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First demonstration of heterogeneous integrated limiter chip with breakdown-enhanced GaN SBDs

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Abstract In this paper, we demonstrated a high power heterogeneous integrated limiter chip with a breakdown-enhanced GaN SBD for the first time. By replacing the conventional thick GaN buffer with a thin AlN buffer layer, the breakdown voltage of the GaN Schottky barrier diode (SBD) was enhanced by a factor of 2.4 without significant degradation of other electrical characteristics. The device achieved a breakdown field strength of 1.2 MV/cm and a Johnson's figure of merit (J-FOM) of 47.2 THz·V. Capitalizing on the superior breakdown performance of this GaN diode, a novel hybrid cascaded self-sensing limiting architecture was proposed, and a heterogeneous integration process was developed to co-fabricate GaN SBDs, Si PIN diodes, on-chip capacitors, and microstrip lines on a GaN-on-SiC substrate. A limiter chip operating from 0.5 to 4.8 GHz is designed and implemented, exhibiting continuous-wave power handling capabilities of 200 W at 2 GHz and 100 W at 4 GHz. These results validate the effectiveness and advancement of the proposed device design, circuit topology, and integration technology, highlighting their strong potential for next-generation electromagnetic protection applications.

Keywords gallium nitride (GaN), Schottky barrier diode (SBD), limiter, heterogeneous integrate

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1 Introduction

Microwave limiters are devices designed to transmit low-power RF signals with low insertion loss while providing sufficient attenuation of high-power signals. These components are critically employed at the front end of RF receiving systems to protect sensitive downstream devices, such as low-noise amplifiers and mixers, from damage or performance degradation caused by high-power microwave injection [1–3]. With the advancement of electronic countermeasures and wireless communications, the electromagnetic spectrum has become increasingly hostile. Receiving systems in communication terminals, radars, and sensing devices are particularly vulnerable to intense electromagnetic interference and intentional jamming, which can lead to operational failures or permanent damage. Hence, the integration of robust limiting protection is indispensable for ensuring system reliability and survivability in these environments.

In contemporary RF receive systems, there is an imperative demand for limiters to enhance power-handling capabilities to address increasingly extreme operational conditions. Concurrently, higher levels of integration are essential to support the ongoing trends in device miniaturization. However, conventional limiter technologies based on silicon (Si) or gallium arsenide (GaAs) are fundamentally impeded by the intrinsic limitations of their material properties, particularly regarding to power tolerance [4–6].

Gallium nitride (GaN), as a wide-bandgap semiconductor, exhibits exceptional advantages, such as a high breakdown electric field and a high-density two-dimensional electron gas with high electron mobility, making it highly suitable for high-frequency and high-power applications [7–9]. Schottky barrier diode (SBD) based on GaN shows considerable promise for realizing high-power and highly integrated limiters. In recent years, notable progress has

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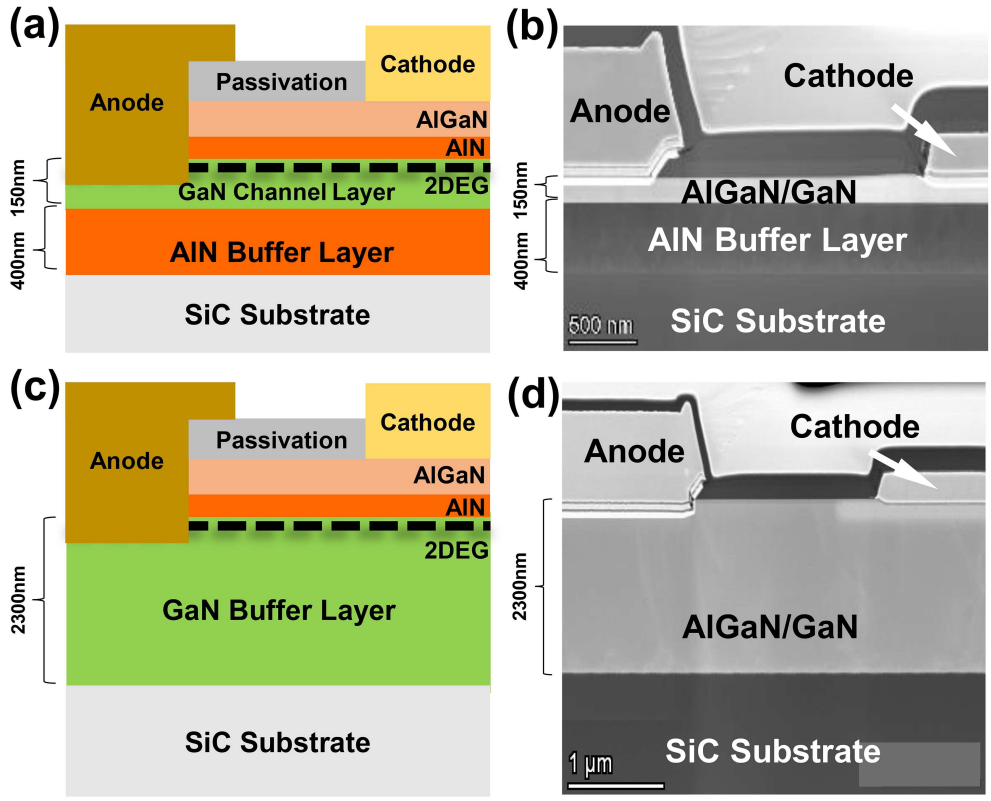

Figure 1 (Color online) (a) Cross-sectional schematic and (b) SEM image of proposed GaN SBD with AlN buffer. For comparison, (c) cross-sectional schematic and (d) SEM image of GaN SBD with GaN buffer.

been made in the power handling capacity of passive limiters utilizing GaN Schottky diodes. However, their performance remains limited by intrinsic operating principles, driving the need for new GaN-based architectures and technical approaches.

This study demonstrates, for the first time, a heterogeneously integrated limiter chip utilizing breakdown-enhanced GaN SBDs, which achieves the highest reported CW power tolerance to the best of our knowledge. At the device level, a novel recessed-anode lateral Schottky diode was implemented, in which a thin AlN buffer layer replaced the conventional thick GaN buffer. Owing to the high breakdown strength and thermal conductivity of AlN, the breakdown voltage increased from 100 to 241 V without significant degradation of other properties. At the circuit level, a self-sensing hybrid cascaded limiting architecture is proposed, which effectively leverages the high breakdown voltage of GaN SBDs and the RF conductance modulation of Si PIN diodes, leading to a significant enhancement in the limiter's power endurance. Furthermore, a heterogeneous integration process was developed to co-fabricate GaN SBDs, Si PIN diodes, microstrip transmission lines, and capacitors on a SiC-based GaN substrate, enabling the chip-scale integration of high-power limiting circuits.

The limiter chip measures only 3.1 mm × 3 mm × 0.1 mm, yet achieves a record continuous-wave power handling capacity of 200 W at 2 GHz. These results validate the effectiveness and advanced performance of the device structure, circuit topology, and integration scheme, demonstrating significant potential for enhancing the electromagnetic protection capabilities of next-generation radio frequency systems.

2 Breakdown voltage enhanced GaN SBDs with AlN buffer

Figure 1(a) illustrates the cross-sectional schematic of the GaN Schottky barrier diode (SBD) incorporating an AlN buffer layer. The epitaxial structure consists of, from bottom to top: a semi-insulating SiC substrate, a 400 nm AlN buffer layer, a 150 nm GaN channel layer, a 1.5 nm AlN insertion layer, and a 22 nm AlGaN barrier layer, with a total thickness under 600 nm. The recessed-anode diode was fabricated following a process consistent with our previous work, with detailed steps available therein [10–12]. A partial cross-sectional scanning electron microscope (SEM) image of the completed device is presented in Figure 1(b), clearly illustrating the material architecture and demonstrating the effectiveness of the fabrication process.

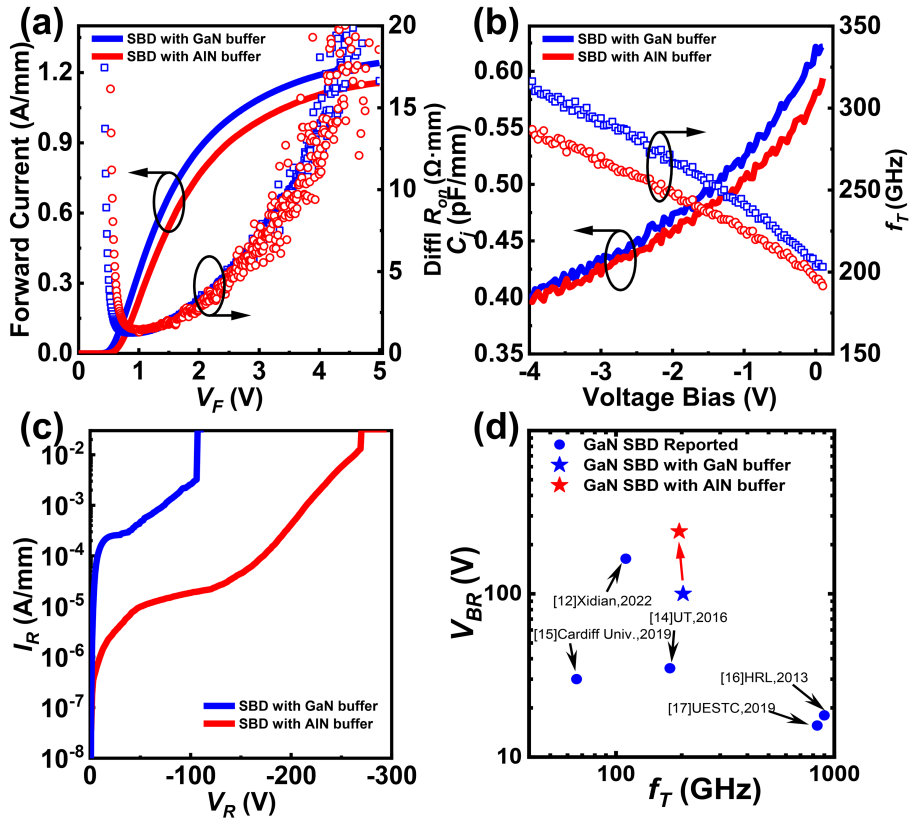

Figure 2 (Color online) (a) Linear-scale I_F-R_{on}-V_F, (b) C_j-f_T-V and (c) I_R-V_R characteristics of SBDs with GaN buffer and AlN buffer. (d) Comparison of f_T and V_{BR} of GaN SBDs.

For comparison, the schematic and cross-sectional SEM image of a conventional recessed-anode GaN diode are presented in Figures 1(c) and (d), respectively. The primary distinction lies in its epitaxial structure: both the buffer and channel layers consist entirely of GaN, with a total thickness of 2.3 μm. This results in an epitaxial thickness four times greater than that of the proposed AlN-buffered device. The cathode-anode spacing (L_{ac}) of both SBDs is 2 μm.

Figure 2(a) compares the forward current-voltage (I_F-V_F) and on-resistance-voltage (R_{on}-V_F) characteristics of GaN SBDs fabricated with AlN buffer layer and conventional GaN buffer layer, plotted in linear coordinates. The conventional GaN-buffered SBD exhibits a saturation current of 1.24 A/mm and an on-resistance of 1.26 Ω·mm. In contrast, the AlN-buffered SBD demonstrates a marginally lower saturation current of 1.16 A/mm and a higher on-resistance of 1.40 Ω·mm. This slight degradation in forward performance is primarily attributed to the thinner channel layer (150 nm) in the AlN-buffered structure, which reduces the two-dimensional electron gas density, thereby leading to decreased current density and increased on-state resistance.

The capacitance-voltage (C_j-V) curve and cutoff frequency versus voltage characteristic (f_T-V) are presented in Figure 2(b). The zero-bias junction capacitance C_{j0} is extracted as 0.58 pF/mm for the AlN-buffered GaN SBD and 0.62 pF/mm for the conventional GaN-buffered device. The cutoff frequencies (defined as $f_T = 1/(2\pi \times R_{on} \times C_{j0})$) for the AlN-buffered and conventional GaN-buffered SBDs are calculated as 196 and 203 GHz, respectively. These closely values demonstrate that both structures exhibit excellent and comparable high-frequency performance.

The reverse current-voltage (I_R-V_R) characteristics are presented in Figure 2(c). A conventional GaN-buffered SBD with a L_{ac} of 2 μm exhibits a breakdown voltage (V_{BR}) of 100 V, significantly surpassing those of typical Si and GaAs SBDs (which typically range from several to tens of volts), and achieves an average breakdown field strength of 0.5 MV/cm. In comparison, the AlN-buffered GaN SBD demonstrates a markedly improved breakdown voltage of 241 V and an average breakdown field strength exceeding 1.2 MV/cm. Moreover, it exhibits a reverse leakage current one to two orders of magnitude lower than that of the conventional GaN-buffered SBD, underscoring the distinct advantages offered by the AlN-buffered structure.

By replacing the conventional GaN buffer with a novel thin AlN buffer layer, the breakdown voltage of the GaN SBD is enhanced by a factor of 2.4. This improvement is attributed primarily to the high breakdown electric field of AlN (>12 MV/cm) [13], which is the highest among III-nitride semiconductors. Furthermore, the AlN buffer

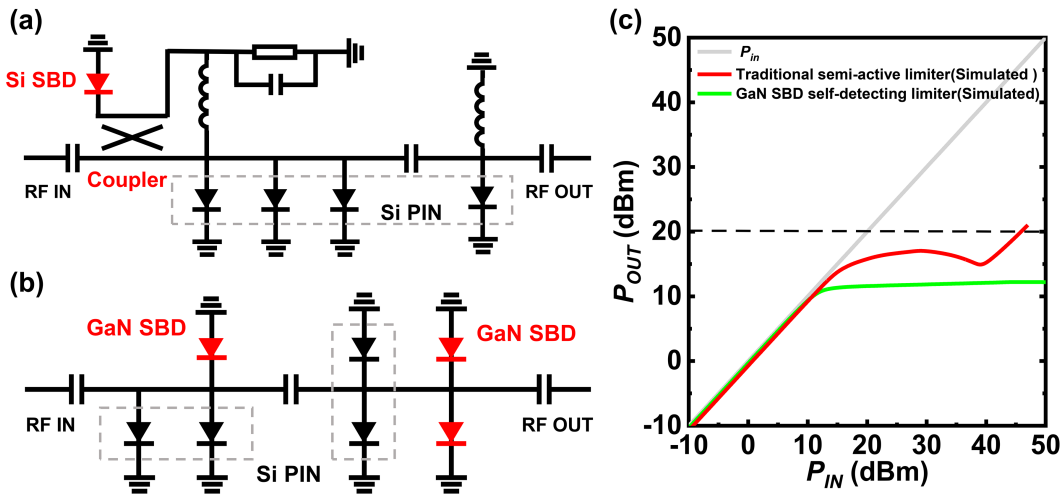

Figure 3 (Color online) (a) Traditional coupled detection semi-active limiting topology; (b) novel hybrid cascaded self-detection limiting topology; (c) comparison of simulated limiting output curves for the two topologies.

serves as a back-barrier that, in conjunction with the AlGaN barrier layer, effectively confines the carriers within the channel, thereby significantly reducing the reverse leakage current of the SBD.

A comparison of the cutoff frequency (f_T) and breakdown voltage (V_{BR}) in this work with previously reported GaN SBDs is summarized in Figure 2(d) [12, 14–17], demonstrating a substantial advancement in breakdown performance. The AlN-buffered GaN SBD exhibits an outstanding Johnson figure of merit (J-FOM = $f_T \times V_{BR}$) of 47.2 THz·V, underscoring its strong potential for high-frequency and high-power applications, particularly in the field of high-power microwave limiting.

3 Heterogeneous integrated limiter chip with GaN SBDs

Conventional high-power limiters typically employ a coupled-detection semi-active architecture, as illustrated in Figure 3(a). When a high-power RF signal is injected, a coupler extracts a small fraction (typically one-thousandth to one-hundredth) of the power to a detection circuit. This signal is then rectified by a Si or GaAs SBD, which generates a DC bias to switch the Si PIN diodes into a low-resistance state. This transition induces an impedance mismatch, thereby reflecting the incident power and achieving limiting functionality. However, due to the relatively low breakdown voltage, limited detection power, and weak driving capability of the Si or GaAs SBD, the activation and limiting performance of the Si PIN diodes are constrained, resulting in unsatisfactory power handling capacity.

The high breakdown voltage of GaN SBDs provides significant flexibility in the design of limiting circuits. This presents a novel hybrid cascaded self-sensing limiting topology, illustrated in Figure 3(b). When high-power microwave signals are injected, the GaN SBD connected in parallel to the main circuit responds first due to its faster reaction speed, initiating the limiting function. Simultaneously, it performs efficient power detection, generating a DC bias that is delivered to the preceding Si PIN diodes. As the input power increases, the driving signal provided by the SBD to the Si PIN diode strengthens, prompting the PIN diode to enter a deeper limiting state. This feedback mechanism stabilizes the power transferred to the GaN SBD, forming an adaptive regulation process. The high breakdown voltage and strong detection capability of the GaN SBD enhance the drive strength for the Si PIN diode, considerably improving the overall power handling capacity of the limiter. Additionally, a pair of GaN SBDs is integrated at the final stage; leveraging their higher power tolerance and ultrafast response characteristics, this configuration further enhances the limiting performance and reduces the residual output power level.

Figure 3(c) shows a comparison of simulation results for the limiting performance of the two topologies. The traditional coupled-detection semi-active limiter exhibits a high threshold power, which is primarily attributed to the presence of its coupling structure. Under high injected power conditions, the PIN diode experiences an abrupt impedance variation, leading to an initial decline followed by a subsequent increase in the output characteristic. This response results in high output power and poor power tolerance of the limiter.

In contrast, the novel hybrid cascaded self-detection limiting topology demonstrates a lower threshold power. Benefiting from an adaptive feedback mechanism, the limiting process yields a smoother and lower output power. Furthermore, leveraging the advantages of GaN SBDs, this topology achieves superior power tolerance. The pro-

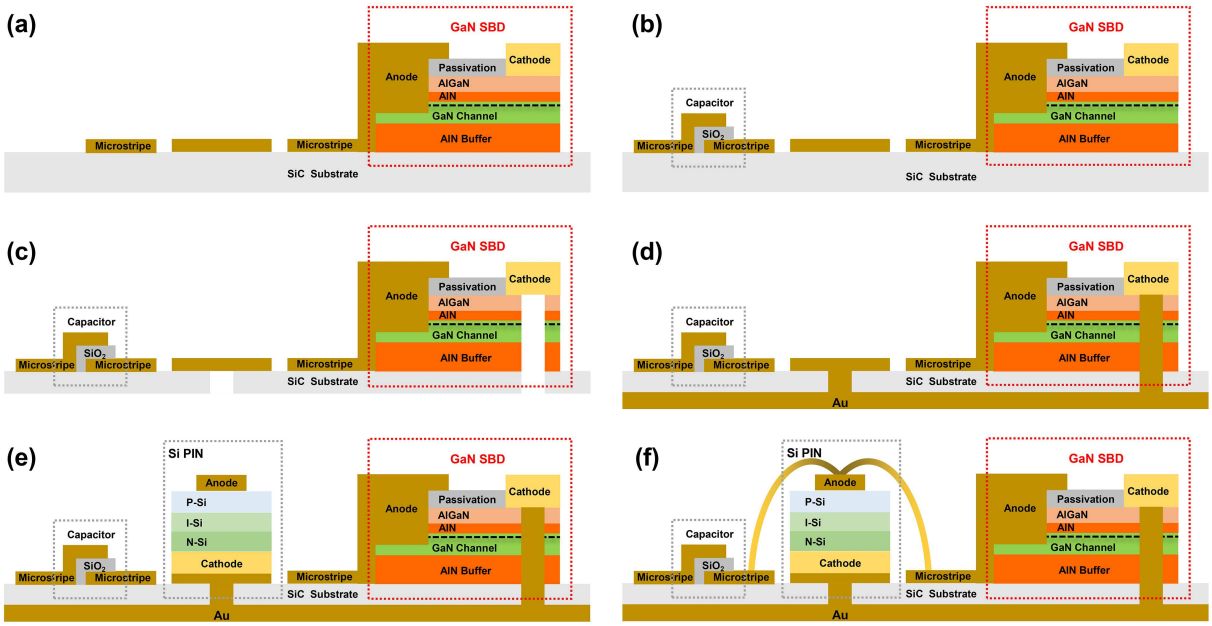

Figure 4 (Color online) GaN heterogeneous integrated limiting chip manufacturing process. (a) SBD interconnect and microstrip wire metallization; (b) on-chip capacitor process (including dielectric deposition, dielectric etching, and metallization); (c) back thinning and backside vias etching; (d) Au electroplating and interconnection on the back; (e) Si PIN sintering; (f) Au wire bonding interconnection.

posed circuit significantly outperforms the conventional architecture in terms of timing logic and power management, offering considerable benefits for advanced radio-frequency protection applications.

To enable the on-chip integration of high-power limiter circuits, a novel heterogeneous integration process was developed to achieve the co-integration of GaN SBDs, Si PIN diodes, capacitors, and transmission lines on a single GaN-on-SiC chip. The fabrication process of the circuit chip following GaN microwave diode is depicted in Figures 4(a)–(f), with key steps including:

(1) Sputtering a Au layer to interconnect the diode anode, form the microstrip transmission lines, and create bonding pads (Figure 4(a));

(2) Growing a dielectric layer, followed by etching and a second Au metallization step to fabricate on-chip capacitors (Figure 4(b));

(3) Thinning the backside of the SiC substrate to 100 μm by polishing, then performing photolithography and etching to form backside vias connecting the GaN SBD cathode and the Si PIN pad (Figure 4(c));

(4) Executing backside Au electroplating to fill the vias and form backside interconnects, followed by dicing the wafer into individual chips (Figure 4(d));

(5) Mounting the Si PIN diode cathode onto the backside Au pad via sintering (Figure 4(e));

(6) Connecting the Si PIN anode to the microstrip line using Au wire bonding to finalize the chip assembly (Figure 4(f)).

By integrating three key technological advances: the novel AlN-buffered GaN SBD device, a hybrid cascaded self-sensing limiting architecture, and heterogeneously integrated chip fabrication techniques, a high-power limiter chip is designed and fabricated, and the photograph is displayed in Figure 5(a). With overall dimensions of 3.1 mm $\times$ 3 mm and a thickness of merely 0.1 mm, the chip combines the benefits of RF conductivity modulation via Si PIN diodes, high-efficiency and high-power detection using GaN SBDs with AlN buffer, and excellent thermal dissipation afforded by the SiC substrate. The measured S-parameters of the limiter are presented in Figure 5(b). The device achieves an insertion loss of less than 2 dB across a broad frequency range from 0.5 to 4.8 GHz, corresponding to a relative operating bandwidth of 162%.

The block diagram of the power testing system for the limiter chip is illustrated in Figure 6(a). A signal generator provides a continuous-wave microwave signal, which is amplified by a power amplifier. The incident power is monitored using a power sensor connected to a coupler port. The signal is then directed through the coupler's output port into the device under test (DUT), where the output power after limiting is measured by a second power sensor. Simultaneously, an infrared thermal camera is positioned above the chip to monitor its real-time thermal distribution during operation.

Figure 6(b) displays the physical configuration of the power test system. Owing to the compact dimensions of

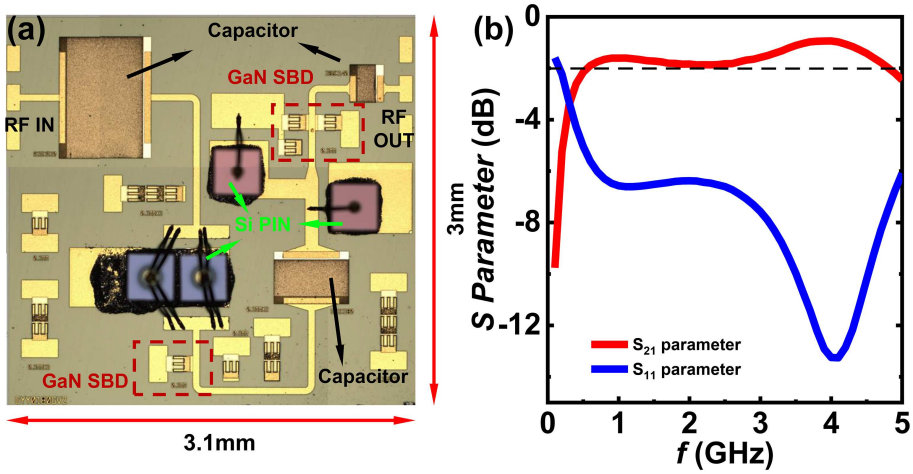

Figure 5 (Color online) (a) The photograph of the fabricated heterogeneous integrated limiter chip; (b) S-parameters of the limiter chip.

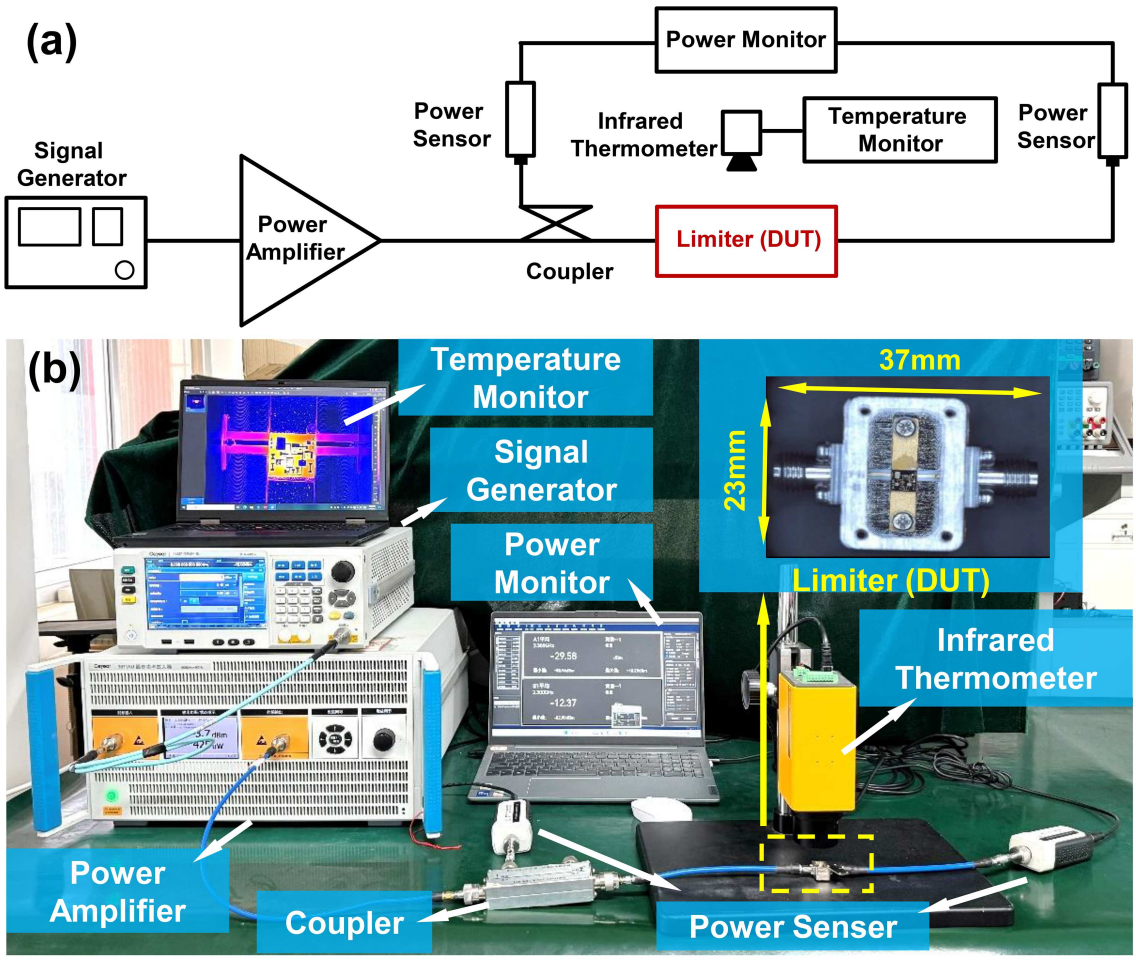

Figure 6 (Color online) (a) Block diagram of the limiting chip power test system; (b) prototype of the limiter chip power test setup and the chip test fixture (inserted picture).

the limiter chip, a custom test fixture was designed and fabricated for this experiment. The chip was mounted using sintering onto a Cu-Diamond heat sink located at the center of the fixture. Input and output connections were established via gold wire bonding to 50 Ω ceramic microstrips, which were subsequently connected to SMA ports. The overall dimensions of the test fixture are 37 mm × 23 mm × 14 mm.

For comparison, a GaN SBD limiter chip with a conventional GaN buffer was co-fabricated and evaluated under

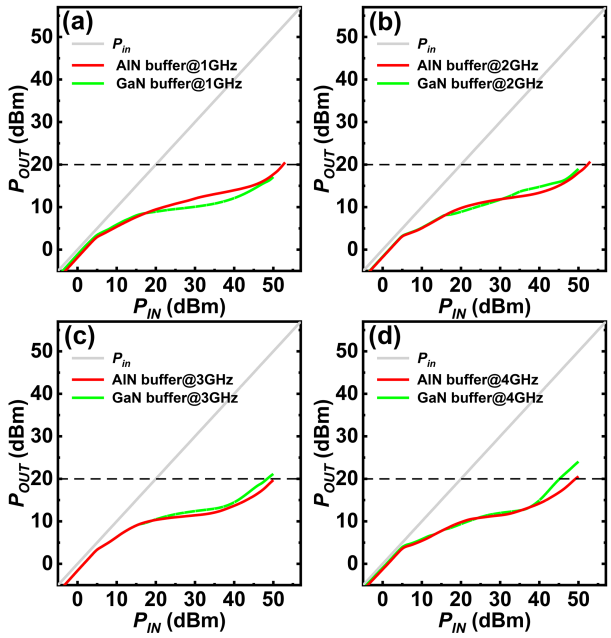

Figure 7 (Color online) Comparison of power test result of limiter chips using GaN buffer layer SBDs and AlN buffer layer SBDs at (a) 1 GHz, (b) 2 GHz, (c) 3 GHz, and (d) 4 GHz.

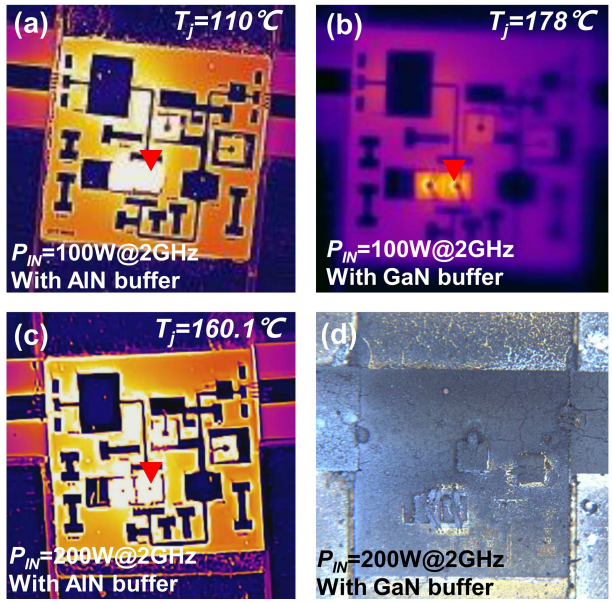

Figure 8 (Color online) The temperature distribution of the limiter chip at 100 W continuous wave input power at 2 GHz using (a) GaN SBDs with AlN buffer; (b) GaN SBDs with GaN buffer. (c) The temperature distribution of the limiter chip using GaN SBDs with AlN buffer at 200 W continuous wave input power at 2 GHz. (d) Photograph of limiter chip using GaN buffered SBDs being completely burned out at 2 GHz 200 W continuous wave input power.

the same test conditions. Both chips were subjected to continuous-wave power injection tests at multiple frequencies, as summarized in Figures 7(a)–(d). Owing to the innovative circuit topology, the proposed limiter chip initiates limiting action at a low input power of 5 dBm. The output power then increases gradually with rising input power, and the rate of increase becomes more obvious beyond 40 dBm (10 W).

At 1 and 2 GHz, the AlN-buffered limiter chip maintained an output power of 20 dBm under 200 W CW input. Limited by the available power amplifier, the maximum input power at 3 and 4 GHz was restricted to 100 W. Even under these conditions, the AlN-buffered limiter chip continued to operate reliably, demonstrating robust limiting performance. In contrast, the conventional GaN-buffered limiter chip exhibited similar trends in output characteristics, yet its maximum tolerable input power reached only 100 W at 1 and 2 GHz. At 3 and 4 GHz, its output power exceeded 20 dBm under 100 W input, indicating comparatively weaker limiting capability.

Figure 8 further presents the temperature distribution of both limiter chips under 2 GHz continuous-wave power injection at 100 and 200 W. Under 100 W injection, the highest temperature is observed at the first-stage PIN diode. As shown in Figure 8(a), the AlN-buffered heterogeneously integrated chip reaches a maximum temperature of only 110°C, while the GaN-buffered counterpart exhibits a PIN diode temperature of 178°C (Figure 8(b)). The elevated temperature in the conventional GaN-buffered limiter chip stems from the restricted detection capacity of the GaN SBD, which operates near its performance boundary. This limitation hinders the complete activation of the Si PIN diode into a low-resistance mode, giving rise to localized thermal accumulation. Moreover, the thick GaN buffer layer exhibits inferior thermal conductivity compared to the thin AlN buffer layer, which additionally contributes to the temperature rise.

Under 200 W continuous-wave injection (Figure 8(c)), the AlN-buffered limiter chip shows a maximum PIN diode temperature of 160°C. Conversely, the GaN-buffered device suffered severe discharge and thermal burnout under the same condition, consequently leading to its complete failure. A micrograph of the chip after thermal failure is presented in Figure 8.

Figure 9 compares the performance of our heterogeneously integrated limiter chip against state-of-the-art published results and commercially available products [2, 7–9, 18–23]. The horizontal and vertical axes denote test frequency and continuous-wave (CW) power handling capacity, respectively. The proposed limiter chip achieves a record CW power handling of 200 W at 2 GHz and 100 W at 4 GHz, demonstrating its leading-edge performance among existing solutions. Furthermore, the full performance potential of the limiter was not fully characterized

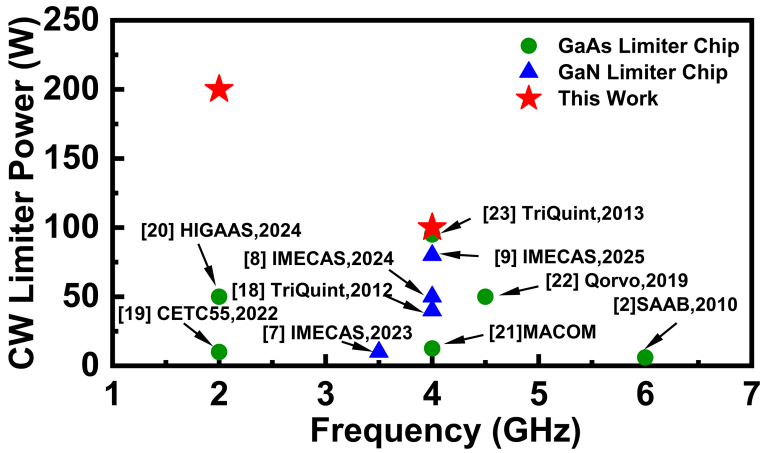

Figure 9 (Color online) Comparison of frequency and CW power capacity of limiter chips in papers and products, this work reports the best continuous wave power results to date.

due to constraints in the available test equipment. It is anticipated that this technical approach offers promising potential for further enhancement.

4 Conclusion

In summary, this study developed a breakdown-enhanced GaN SBD by replacing the traditional thick GaN buffer with a thin AlN buffer. This improvement increased its breakdown voltage by a factor of 2.4, with minimal degradation of other electrical properties. The breakdown field strength reached 1.2 MV/cm, and the Johnson figure of merit (J-FOM) reached 47.2 THz·V. Leveraging this advanced diode, a novel hybrid cascaded self-sensing limiting topology was proposed. A heterogeneous integration process was further established to co-fabricate GaN SBDs, Si PIN diodes, on-chip capacitors, and microstrip lines on a GaN-on-SiC substrate. Ultimately, a limiter chip operating from 0.5 to 4.8 GHz was designed and fabricated, demonstrating exceptional continuous-wave power handling capability-withstanding 200 W at 2 GHz and 100 W at 4 GHz, which are the highest values reported to date for such devices, highlighting its great potential for electromagnetic protection applications.

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