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• REVIEW •
Special Topic: Recent Progress of Fundamental Research on Post-Moore Novel Devices

Memristive dynamics enabled neuromorphic computing systems

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Abstract The slowing down of transistor scaling and explosive growth for intelligence computing power emerge as the two driving factors for the study of novel devices and materials to pursue highly-efficient computing systems. Memristors, incorporating rich intrinsic dynamics, are a promising candidate for constructing efficient and scalable bio-inspired computing systems. In this progress report, we review the latest advances in novel types of memristors as well as their applications in implementing neuromorphic computing systems. This paper not only covers the memristive dynamics-enabled bionic computing systems but also discusses the memristive sensory systems that integrate sensing and computing. Eventually, device-circuit co-optimization methods are given to emphasize the trend of cross-layer co-design in this fast-evolving field. The innovation in memristor devices mainly focuses on specialized computing hardware and yields superior computing and sensing efficiency. At last, we offer our insight into the trend of state-of-the-art research in memristive materials, devices, circuits, and systems.

Keywords memrsitor, memristive dynamics, artificial synapse, artificial neuron, neuromorphic computing

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1 Introduction

The original Moore's law, that is the transistor densities are predicted to double around every 2 years, has dramatically slowed down faced by the difficulty in sub-10 nm CMOS technology nodes [1–4]. Mature von Neumann architecture, previously fueled by the powerful Moore's law to boost performance, yields dominating power consumption and computing latency of transferring data between the processing units and memories [5–10]. This so-called "memory wall" hinders further scale-up of the hardware computing resources [11–16]. However, on the market side, emerging deep-learning-based artificial intelligence applications are recklessly calling for computing resources for limited patterns of multiply-accumulate (MAC) [17–25]. Ironically, around 2017, the predicted computing resource demand growth rate was about twice as large as the practical computing resource growth rate on the earth [26–31]. This disastrous imbalance calls for novel computing paradigms for efficient computing, including smart materials and devices as well as the novel architecture of computers built out of them [32–36].

In this paper, we focus on this track of innovation. We report the latest progress of post-Moore neuromorphic computing systems with innovative materials, devices, and computers built from memristive dynamics. Memristive devices, also known as memristors, refer to a diverse family of nanoscale devices. They include nanoscale devices that change resistivity with external excitations. Specifically, the dynamics of memristors, i.e., how their resistivity is changed over time, have shown differences. The organization of this paper is shown in Figure 1. This progress report not only covers the latest progress on bionic computing systems implemented based on the memristive devices but also memristive sensory computing

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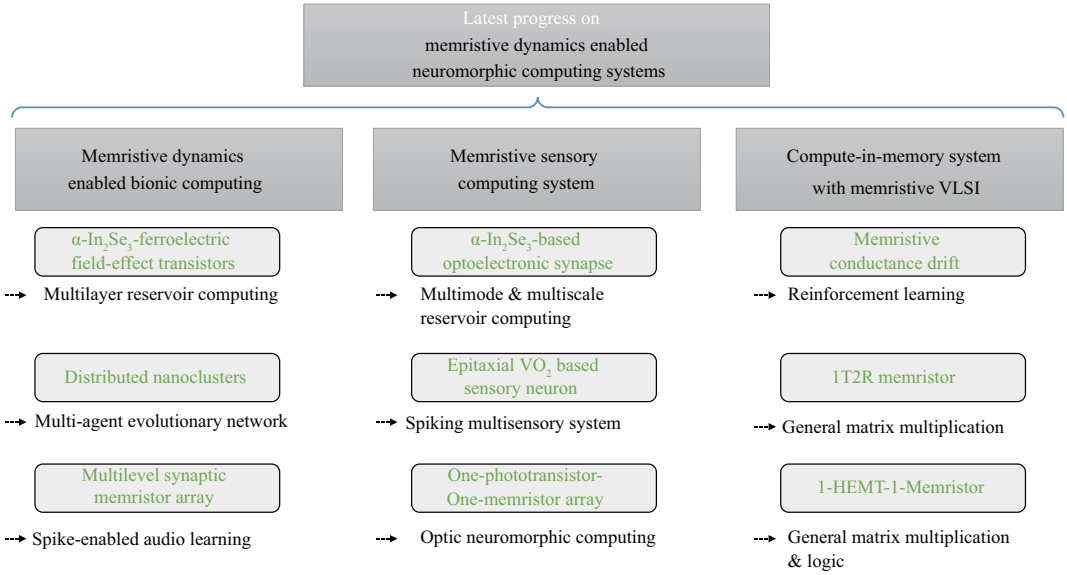

Figure 1 (Color online) Structure of this paper.

systems for multimode signal processing and memristor device very-large-scale integration (VLSI). We report the latest advances in leveraging memristor dynamics to achieve high efficiency and scalable, from devices to circuits and systems, and provide our insight on the trend of exploiting memristor dynamics.

According to different types of applications, the rest of the paper is organized as follows. Section 2 presents the bionic computing paradigms enabled by memristive dynamics; Section 3 elaborates on the memristive device-based sensory computing systems; Section 4 describes the VLSI design for memristor-based compute-in-memory systems. Simultaneously, various neuromorphic computing applications call for different parameters of memristor nanoscale devices. For memristive bionic computing systems, multi-level cell programming and retention are the key enablers for the synaptic and neural properties for precise programming and representation of information [37]; the sensitivity for sensing the external signals is important to the memristive sensory computing systems for the multimodal fusion [38]; as for the memristive VLSI design, uniformity of memristor devices should serve as the prerequisite of large-scale integration and relatively high resistivity would generally improve the computing efficiency [39, 40].

2 Memristive dynamics enabled bionic computing

2.1 Ferroelectric α-In_2Se_3 based multilayer reservoir computing

Reservoir computing refers to a class of recurrent neural networks (RNNs) mapping the inputs into a high-dimensional space [41]. A "reservoir" in reservoir computing can be physically implemented by the memristive devices for enhanced power efficiency with rich dynamics of short-term memory characteristics and the nonlinearity of the synaptic weights. Among various materials, α-In_2Se_3 features both in-plane and out-of-plane ferroelectricity with dipole locking effect even thinned to the monolayer limit [42, 43]. Memristive devices made with α-In_2Se_3 exhibit rich long-term and short-term memory characteristics [44] and are appropriate for implementing reservoir computing hardware. Liu et al. [44] proposed a type of α-In_2Se_3 ferroelectric semiconductor field-effect transistors (FeSFETs).

Figure 2(a) illustrates the device structure of the FeSFET. When sweeping the top gate voltage from -3 to $+3$ V hysterically (drain-to-source voltage is confined to 1 V), the drain-to-source current response versus the gate voltage is shown in Figure 2(b). It reveals a limited gate controllability of the top gate. FeSFET demonstrates a dynamic response with a voltage pulse (-2 V, 100 ms) as the gate voltage excitation, and a low voltage bias of -0.2 V is fed to measure the drain-to-source conductance. The current is observed to decrease upon the arrival of the pulse followed by an increase and a decay toward the initial conductance level. In this process, the decay is limited to a small amplitude and a reasonable part remains after a long time. This compound behavior implies short-term and long-term synaptic plasticity. FeSFET is suitable for implementing synapses (Figure 2(c)). With the help of these rich

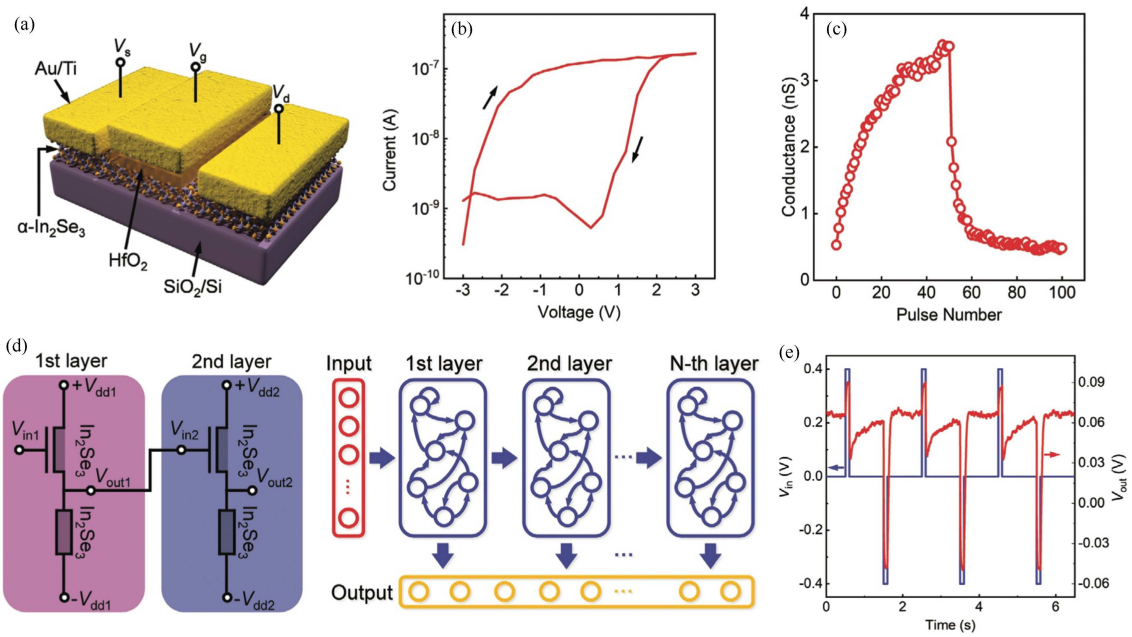

Figure 2 (Color online) (a) Device structure of the FeSFET; (b) transfer curve of the DC sweep; (c) synaptic response of FeSFET; (d) schematic diagram of the FeSFET multilayer reservoir computing; (e) short-term memory characteristics shown in the response of FeSFET to a train of voltage pulses [44] © 2022 Wiley-VCH GmbH.

dynamics, deep reservoir computing hardware can be implemented.

Figure 2(d) depicts a schematic diagram of the deep reservoir computing system with stackable α-In_2Se_3 FeSFETs. The synaptic weights are stored in the α-In_2Se_3 FeSFETs. The aforementioned short-term and long-term memory characteristics help FeSFETs form a high-dimensional space for reservoirs to boost the distance between different features. Figure 2(e) shows a temporal output voltage response to a train of gate voltage pulses (+0.4/−0.4 V, 100 ms), indicating the volatile short-term memory characteristics leveraged in reservoir computing. Liu et al. [44] designed a reservoir computing with FeSFET for a time series prediction task. The input temporal series data are linearly mapped to the gate voltage of FeSFET in the range of (1, 2.5) V. Each reservoir layer outputs 20 data points and the two layers of 40 data points are fed into a 40 × 1 network. One-step-ahead prediction with this network is trained with linear regression. Implemented by only a few FeSFETs, the calculation results of the memristive FeSFET reservoir computing achieve an average absolute percentage error (MAPE) of 4.67%, which is very close to the ideal algorithmic results of MAPE from 4.359% to 7.214%.

2.2 Memristive switching based multi-agent evolutionary network

In order to emulate and solve complex systems, physical networks built with nanoarchitectures (including nanowires, nanoparticles, or random dopants) inspire novel types of bionic computing systems with intrinsic nonlinear dynamics or internal state interactions [45–48]. With this thought, Xu et al. [49] presented a nanoscale, solid-state multi-agent evolutionary network (MAEN) based on the self-organization of distributed Ag nanoclusters. Shown in Figure 3(a), the rich dynamics of Ag-based memristive switching show promising energy efficiency for MAEN computing. The Ag nanoclusters in the MAEN system play a role as de-centralized agents with dynamic evolutions realized by field-driven electrochemical reactions and ion migrations. There exists a positive feedback loop of the alignment of Ag nanoclusters that can emulate the cooperation and competition between the agents in a multi-agent system according to certain principles of optimization. Ag nanoclusters perform self-organized evolution for two kinds of basic modulation units: distance modulation and voltage modulation. These two modulation units together compute the weights of edges in a non-structural graph data form. MAEN system has parallel and serial integration schemes of basic modulation units applied to the solution of varied graph problems.

MAEN system can be used for the emulation of swarm intelligence [50–52] via a physically evolving process (Figure 3(a)). In the MAEN system, self-assembled polyethylene oxide (PEO) with high Ag^+ ion mobility serves as the solid polymer electrolyte. Many Ag nanoclusters with a diameter of ∼10 nm

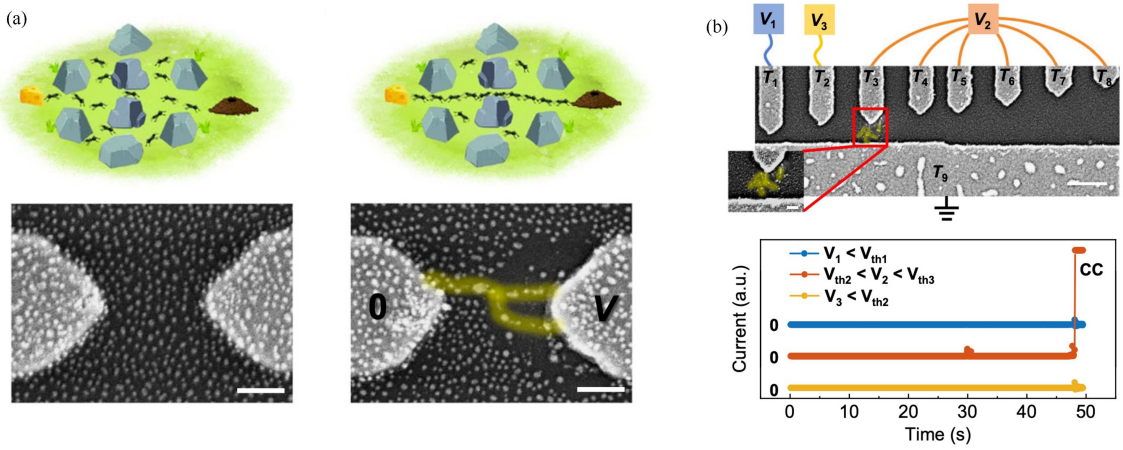

Figure 3 (Color online) (a) Physical networks for swarm intelligence and MAEN-based physical network; (b) MAEN computing microscopic photos with connecting diagrams [49] © 2022 Xu et al.

are randomly distributed in the device, forming bipolar electrodes under an external electric field. Subsequently, the ionization, ion migration, and reduction processes of individual Ag atoms represent the self-organization evolution of the distributed agents. The nanoclusters aggregate by reducing their distances and enhancing the local electric field, resulting in a positive feedback loop mechanism. Conductive filaments are thus generated to induce memristive switching in this device. Through macroscopic electric measurements, evident increases in device currents represent the computational results of such a physical network computing system. Actually, this self-organized evolution of Ag nanoclusters ensembles the process of gradient descent. This is equivalent to the distribution potential function relating to the voltage biases fed to different terminals of the device, as shown in Figure 3(b). MAEN exploits such a physical process for multi-agent interaction emulation without large and complex digital computing circuits. This is an excellent example of leveraging memristive dynamics for high-efficiency computing.

2.3 Spike-enabled audio learning in multilevel synaptic memristor array-based spiking neural network

Nowadays, speech interaction has become an almost standard configuration in ubiquitous controllers, including on vehicles, smart home devices, and wearable devices [53, 54]. Spiking neural network (SNN) features sparse activation and excellent feature extraction capability in speech recognition, making it a promising candidate as a low-power implementation of processing audio signals [55–59]. Wu et al. [60] demonstrated W/MgO/SiO_2/Mo memristor with nonvolatile, analog switching characteristics to store SNN synaptic weights and perform CIM SNN training and inference for speech recognition. Figure 4(a) depicts the W/MgO/SiO_2/Mo memristor device structure and its long-term potentiation and long-term depression behaviors as an SNN synapse. This pulse-based programming scheme is the basis of in situ learning of memristive SNN computing hardware. Figure 4(b) shows the die photo of the schematic illustration of an array configuration of the W/MgO/SiO_2/Mo memristors. In the compute-in-memory (CIM) mode [61], inputs are fed horizontally as voltages and the currents aggregate vertically as the calculation outputs. This operating principle has become the standard of the CIM vector-matrix multiplication (VMM). Figure 4(c) shows small cycle-to-cycle (C2C) and device-to-device (D2D) variations as SNN synapses [62–65], showing a good potential for large integration.

The memristive SNN speed recognition system includes preprocessing components that convert the one-dimensional audio signal into Mel frequency cepstrum (two-dimensional data). With a latency encoding module, it forms spatiotemporal spiking patterns as the inputs into the memristive SNN hardware, which is illustrated in Figure 4(d). SNN is trained to classify different spatiotemporal spike patterns. The inference test of the memristive SNN on the TIDIGITS dataset achieves 94% accuracy with 10 epochs of training [66–69]. This work demonstrates a standard pattern of developing novel memristive devices for specialized bio-inspired computing systems.

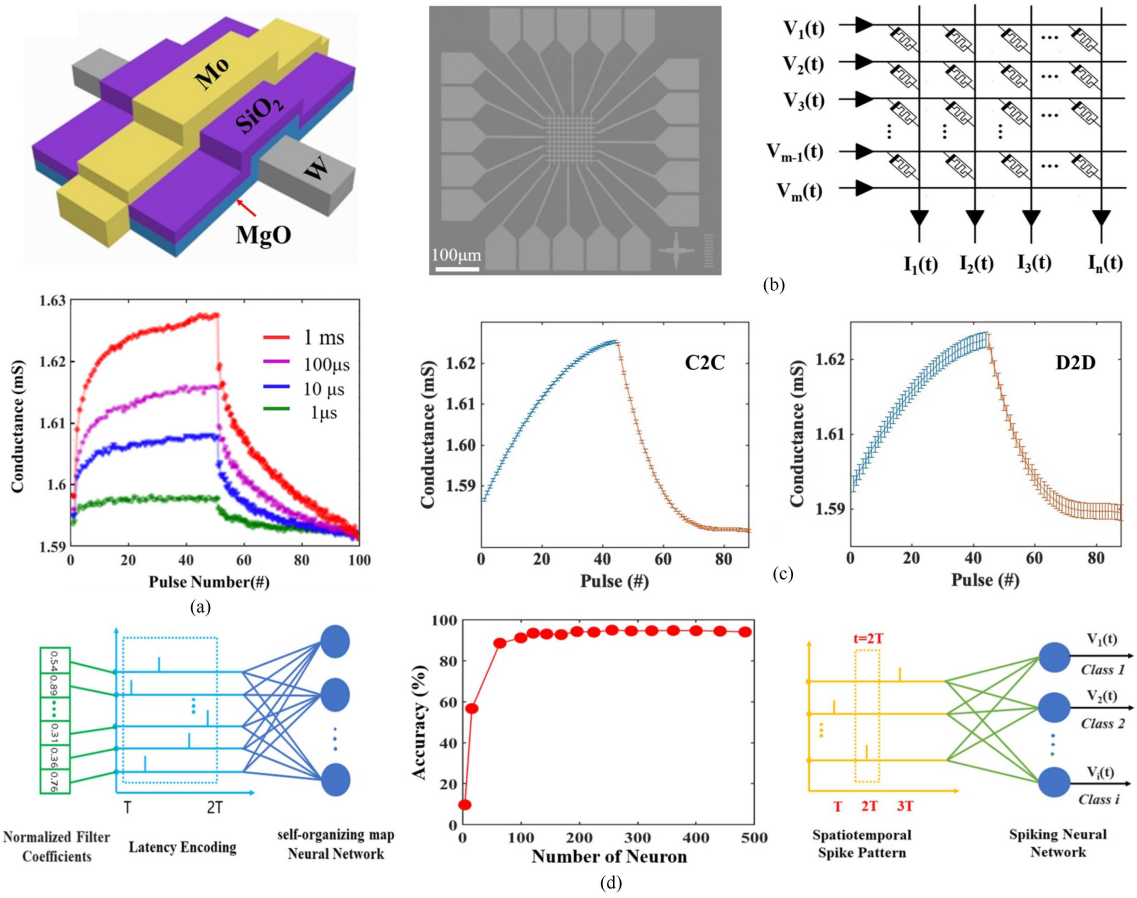

Figure 4 (Color online) (a) Device structure of the W/MgO/SiO_2/Mo memristor and its electrical synaptic properties; (b) array die photo and configuration of the W/MgO/SiO_2/Mo memristor for CIM; (c) C2C and D2D variations of the W/MgO/SiO_2/Mo memristors in an array; (d) signal pre-processing transformation and training results of the memristive SNN for speed recognition [60] © 2022 Wiley-VCH GmbH.

3 Memristive sensory computing system

3.1 α-In_2Se_3-based optoelectronic synapse for reservoir computing

Liu et al. [70] proposed a type of optoelectronic synapses based on α-phase indium selenide (α-In_2Se_3 with controllable temporal dynamics. The devices can be used for multimode and multiscale reservoir computing. The material of α-In_2Se_3 shows intriguing properties. As a type of van der Walls semiconductor material, α-In_2Se_3 has in-plane and out-of-plane ferroelectricity at room temperature even as a thin monolayer [71]. Its dipole-locking effect helps manipulate ferroelectric polarization and subsequently contributes as an effective method to tune device electrical behaviors [71, 72]. Besides, the outstanding optical properties make In_2Se_3 a good material candidate to fabricate photodetectors or optoelectronic memories.

Based on these properties, α-In_2Se_3-based optoelectronic synapse is fabricated for multimode and multiscale signal processing. For the electrical characteristics, the temporal dynamics of α-In_2Se_3-based optoelectronic synapse devices are observed through transient electrical measurements, as shown in Figure 5(a). Postsynaptic current varies following the applied voltages (Figure 5(b)). This demonstrates the possibility of constructing short-term memory with short-term potentiation and short-term depression effects. The short-term memory effects, including short-term potentiation and depression, probably originate from the charge trapping/de-trapping process and ferroelectric switching/relaxation. The long-term depression and long-term potentiation effects can be achieved by applying a train of identical voltage pulses to induce ferroelectric polarization switching in α-In_2Se_3. With these rich bio-realistic dynamics under various electrical stimuli, α-In_2Se_3 makes an excellent candidate to build electrical bionic synapses. The aforementioned short-term memory effects and nonlinearity of the devices are particularly impor-

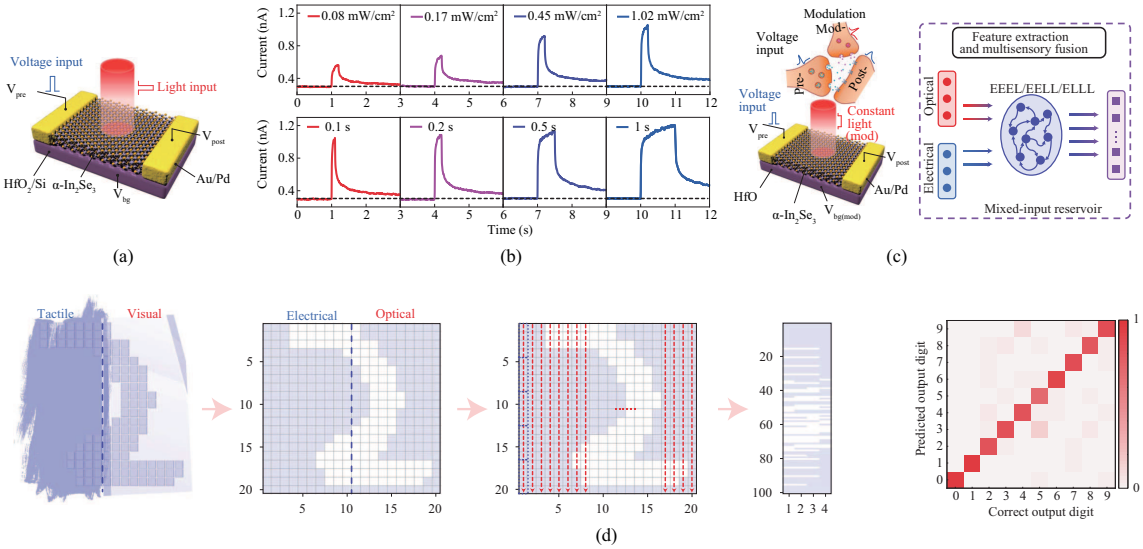

Figure 5 (Color online) (a) The device structure of α-In_2Se_3 memristor; (b) light-induced responses in α-In_2Se_3 memristor; (c) the fused multisensory system with reservoir computing; (d) tactile and visual fused sensory pattern recognition [70] © 2022 Springer Nature.

tant in implementing reservoir computing systems. Moreover, the intrinsic optoelectronic properties of α-In_2Se_3 lead to an interestingly multimodal compound device. The α-In_2Se_3 device also shows the STP effect when illuminated by a 655-nm laser at a small voltage bias (-0.1 V). The resistivity can be altered by the light intensity.

As observed, there exists compound temporal dynamics of α-In_2Se_3 memristor stimulated electrically and optically (Figure 5(c)). This offers an additional degree of freedom to tune the device's characteristics. The simultaneous excitations of light intensity and device back-gate voltage form the "heterosynaptic plasticity" that mixes the ferroelectric and optoelectronic responses of the α-In_2Se_3 memristor. By fusing the multisensory results, α-In_2Se_3 memristors can construct a multimode in-sensor processor. Figure 5(d) shows the multimode recognition system with mixed-input reservoir computing. The visual inputs are direct optical (light) pulses illuminating the device; an external tactile sensor converts the pressure information into electrical pulses and applies to the α-In_2Se_3 memristors electrically. α-In_2Se_3 memristors fuse the multimode signals, which helps improve the performance of the reservoir computing. It conducts a nonlinear transformation on the input and makes the target information linearly separable in a high-dimensional space. α-In_2Se_3 memristors can also help extract features from temporal signals effectively by operating at multiple timescales. This is achieved by tuning the relaxation time with the additional degree of freedom of optical or electrical excitation.

3.2 Epitaxial VO_2 based sensory neuron for spiking neuromorphic multisensory system

For efficient sensing and processing integrated implementation, Yuan et al. [73] presented a calibratable artificial sensory neuron (CASN) developed with an epitaxial VO_2 memristor. Grown by pulsed laser deposition, VO_2 memristor shows boosted C2C uniformity in their neural behaviors thanks to the high crystalline quality of epitaxial VO_2. With the help of an accompanying calibration resistor, D2D variation is also significantly suppressed. Different from the aforementioned sensory synapses, VO_2 memristor serves as the neural unit to generate oscillation (spikes) using the short-term temporal response characteristics. The schematic diagram of the sensory neuron circuit is illustrated in Figure 6(a). R_c is the calibration resistor, S is the sensor, and R_{scaling} scales the sensor output into an appropriate range to be compatible with the VO_2 memristor. Figure 6(b) shows the DC charactersitcs (R_L) of the epitaxial VO_2. memristor and Figure 6(c) presents the spiking frequency responses under different R_L, input voltage V_{in} and the shunt capacitance C_{parallel}. The response frequency is negatively related to R_L and C_{parallel} and positively related to V_{in}.

Various sensors with voltage outputs, such as pressure, light, temperature, and curvature sensors, can be integrated into this generic VO_2-memristor-based sensing and processing scheme. Figure 6(d) shows an implementation of a curvature sensory computing system to recognize different gestures. The

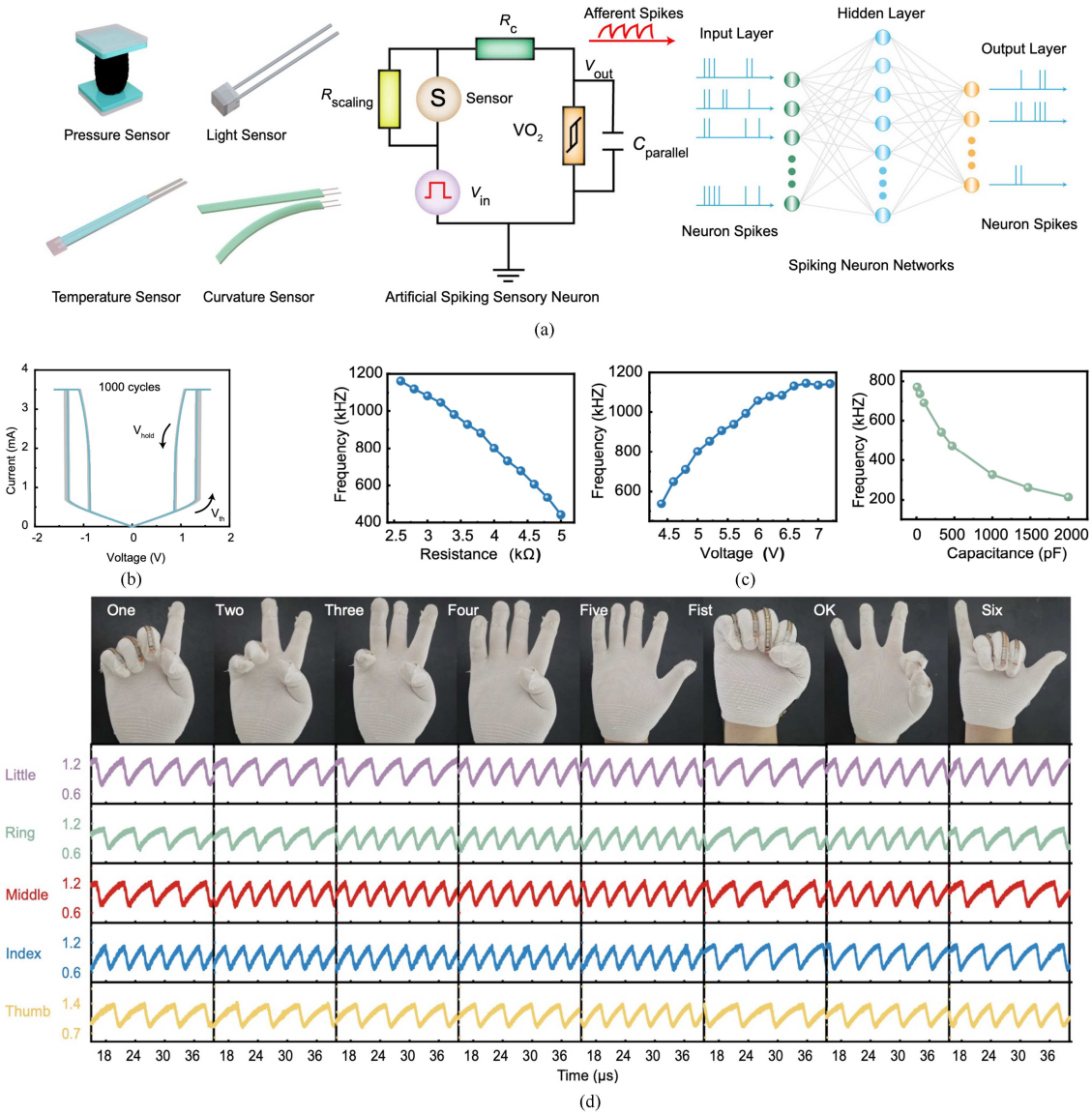

Figure 6 (Color online) (a) Artificial spiking sensory neuron with VO_2 memristor; (b) DC I-V curve of the VO_2 memristor; (c) spiking frequency modulation of the artificial spiking sensory neuron with VO_2 memristor; (d) gesture sensing and recognition system [73] © 2022 Yuan et al.

VO_2-memristor-based artificial spiking sensory neurons attach to each finger and the output spiking frequencies of the five neurons directly encode the output that implies a certain gesture. On average, each spike costs only around 2.9 nJ of energy. The energy consumption is promising to significantly scale down in around 3 orders of magnitude in this scheme because the VO_2 memristor resistance can easily scale up by controlling the growth conditions of the VO_2 film and the threshold voltage of the spiking generation may decrease with the help of reduced channel length of the VO_2 memristor.

3.3 One-phototransistor-one-memristor array for optic neuromorphic computing

By mimicking the human visual system, optic neuromorphic devices center on specific visual processing and cognitive tasks, including image enhancement, noise reduction, pattern recognition, and other low-level visual signal processing tasks [74]. The major challenge lies in the fundamental devices to build optic artificial neural networks (OANN). Bitcell selectors to avoid sneak paths and silicon compatibility are the two key requirements for implementing large-scale OANN computing systems. Dang et al. [75] fabricated a one-phototransistor-one-memristor (1PT1R) optic neuromorphic device presenting light-tunable plasticity for in-sensor computing.

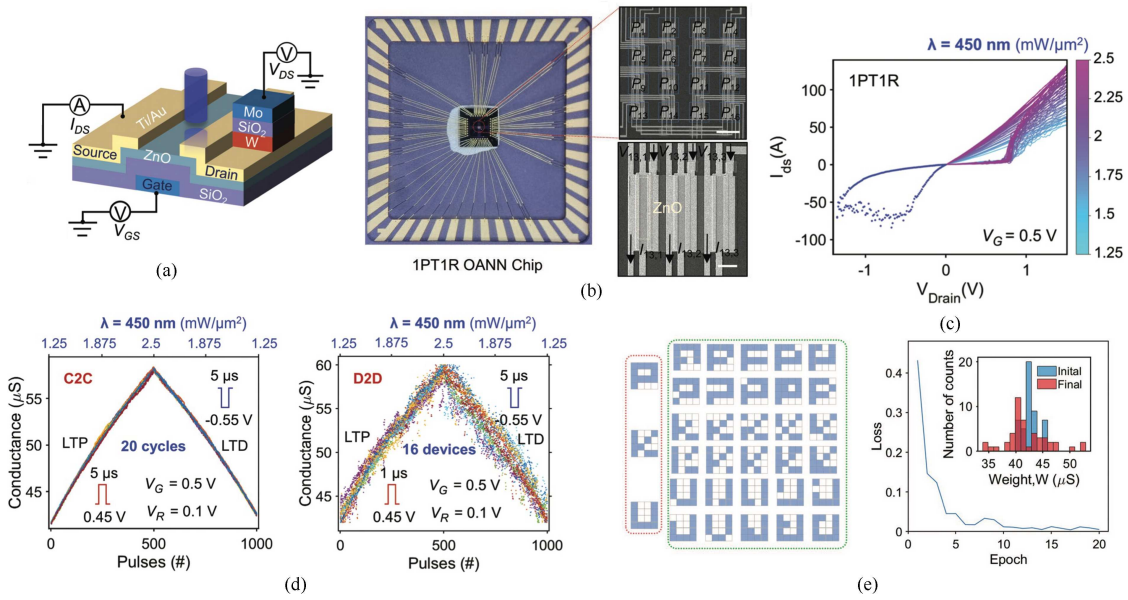

Figure 7 (Color online) (a) Structure diagram for the 1PT1R device; (b) die photo for 1PT1R array for OANN; (c) DC characteristics of 1PT1R bitcell; (d) light intensity sensing characteristics of 1PT1R bitcell; (e) OANN to classify "P", "K", and "U" patterns [75] © 2022 Wiley-VCH GmbH.

The 1PT1R device is composed of a ZnO thin-film transistor (TFT) and a nonvolatile $Mo/SiO_2/W$ memristor, as illustrated in Figures 7(a) and (b). The DC characteristics of the 1PT1R device are shown in Figure 7(c). The memristor demonstrates a highly linear programming curve. $Mo/SiO_2/W$ memristor is serially connected to the drain of the ZnO TFT. The ZnO TFT can be controlled by the light, introducing the interface to a light sensor. A bias voltage is applied to the gate and the drain terminals of the ZnO TFT to receive different light intensities of the laser source (with a wavelength of 450 nm). The light intensity sensing behavior is shown in Figure 7(d). The threshold voltage is about 0.7 V with an on/off ratio over 10^7. The linearity of the conductance programming means it is convenient to the in situ learning in constructing the OANN.

This 1PT1R array can implement a highly-efficient OANN. Dang et al. [75] implemented an in-sensor computing recognition system based on a 16 × 3 1PT1R array to sense and classify 4 × 4 resolution pictures containing "P", "K", and "U" (Figure 7(e)). Training is done in 20 epochs, showing a recognition accuracy of 99.3%.

4 Compute-in-memory system with memristive VLSI

4.1 Conductance drift based eligibility traces computing for reinforcement learning

Reinforcement learning algorithms derive knowledge by gaining rewards from the environment and completing complex tasks such as chess games or control problems without supervision from humans [76–79]. The outcome, i.e., a "policy", of the reinforcement learning system is comprised of state-action pairs that lead the agent to obtain a maximum reward. This policy can be achieved by machine learning methods, including SARSA and deep Q networks. Throughout the learning process, eligibility trace (ET) is introduced to accelerate convergence. It records a state trace of the agent with decay over time. Once a high-level reward is received, the policy of all states will be updated with the amplitudes proportional to the corresponding ET. Hence, in the next training epoch, ET will rapidly lead the agent to those states with high rewards as well as avoid states with a penalty. However, the performance of ET algorithms implemented on the conventional platforms is restricted by the memory wall as ET size increases. To address these challenges, Lu et al. [80] leveraged the conductance drift (CD) effect in memristor nanoscale devices for efficient ET computing for reinforcement learning.

CD effect exists widely in memristor devices [81,82]. It refers to the phenomenon of passive conductance (resistivity) drifting from the programmed values over time without external electrical excitations [83]. Taking amorphous $Ge_2Sb_2Te_5$ (GST) phase change memory (PCM) [84–87] as an example, the CD effect

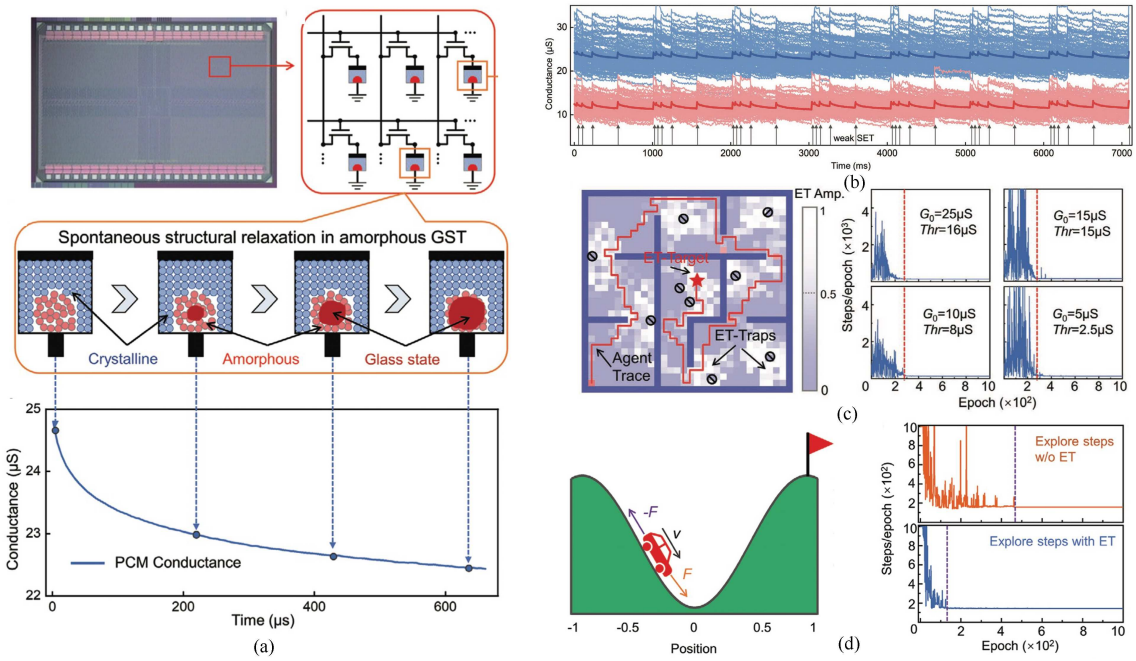

Figure 8 (Color online) (a) 4 Mb memristors with intrinsic CD effect; (b) ET evolution with mapped to memristive conductance with CD effect; (c) Task I using the memristive CD for reinforcement learning ET; (d) Task II using the memristive CD for reinforcement learning ET [80] © 2021 Wiley-VCH GmbH.

is caused by spontaneous structural relaxation. It results in a stable conductance decay over time after SET operations (program devices from high to low resistance states) without any energy consumption. This in-memory electrical-excitation-free decay is exploited to emulate the similar decay in ET for higher computing efficiency. Here, a 4 Mb carbon-doped GST (C-GST) PCM chip stores ET data and execute the in-memory decay computing to implement ET. The convergence of the SARSA (λ) reinforcement learning training algorithm is accelerated by the PCM-ET, and the agent achieves outstanding performance in 30 $\times$ 30-state maze navigation and 220-state mountain car game. In addition, the multi-level PCM cells used to save ET during reinforcement learning training are reused to save the final policy, which is represented by 1 of 4 conductance states, with high storage density and long retention so that system hardware cost is also greatly reduced.

The PCM CD effect is systematically investigated experimentally. 9 groups (about 1000 devices in each group) of PCM devices are programmed to 9 resistance states (1–25 μS) by several SET, RESET, and verify operations. All devices in different states show stable and obvious CD in only 600 ms after programming. Relative conductance attenuation amplitude at 6 ms after programming distributes within 2% in all states. The drift is more stable in high conductance states. Figure 8(a) shows the conductance changes in various states over time, the test data (dots) can be well fitted by the model (lines) $G = G_0 \cdot (t/t_0)^{-\nu}$, where ν is the drift coefficient. ν is experimentally extracted from the slopes of the lines. ν follows a normal distribution with stable means of 0.01–0.02 in all states. Its standard deviation is lower in higher conductance states. After consecutive partial SET operations with different time intervals, the device conductance undulates in a certain range due to the reverse effects of CD and the SET operations. Based on the CD and partial set stimulation, ET can be implemented with low energy consumption. Such programming techniques help obtain a deliberate CD effect to emulate the decay in ET without external excitation.

Figure 8(b) shows ET waveforms in two levels implemented by about 100 PCM devices in the 2 selected states within a micro-second time scale, this speed can well match the processing speed in conventional platforms. In addition, the mean conductance after every set operation is well maintained for more than 40 periods, this indicates the replacing ET which results in faster and more reliable reinforcement learning training than the conventional accumulating ET. PCM-ET is evaluated in the two types of reinforcement learning tasks: discrete (Task I) and continuous (Task II) state reinforcement learning tasks.

• Task I: maze navigation. The effect of PCM-ET is demonstrated in the maze navigation task. The reinforcement learning agent needs to learn a strategy from the 30 $\times$ 30 maze with traps, guidance, and

target (with reward −10, 1, 100, respectively) through SARSA(λ) and ϵ-greedy algorithms. For each step, the agent should select a move directly from "up", "down", "left", and "right". One training epoch ends whenever the agent reaches a trap or the target. Figure 8(c) shows the efficacy of ET (with exponential decay) in reinforcement learning training. The total reward received per epoch in ET training converges rapidly to as high as 100 in about 250 epochs, implying the fast formation of correct policy to reach the target and avoid traps. Explore steps (steps that cause extra computing overheads) per epoch also reduces to a very low level after the agent fully explores the maze and finds a proper way to the target in ET training, while the steps without ET are still lingering over the exploration of the maze. The training performance varies with different decay rates. Parametric calibration is required in that larger a (slow decay) causes more explore steps while smaller a results in many epochs before convergence, therefore optimal ET decay rate for the maze task is about 0.8–0.9 given the task and reward configuration.

Compared with this appropriate range of decay rate, the PCM-CD with $0.01 < \nu < 0.03$ is too slow for reinforcement learning training. Thus, a linear transformation is used to amplify the decay amplitude of PCM-CD to be comparable to ET. With such linear transformation, PCM-ET can achieve the wanted similar decay as ET in all 1000 epochs. The distributions of the effective memory length, which is the count of states with ET > 0.5, shift to a low level with an increase of threshold (Thr) in the transformation for a given conductance state. Thus, by modifying the Thr in each conductance state, memory length can be adjusted to the proper range, corresponding to decay within the range of (0.8, 0.9). According to the ET, the final policy will guide the agent to avoid the regions around the traps or follow the traces to the target in advance. With too long memory, there will be too many regions to avoid and it is hard to find a correct way out; while too short memory may reduce suppression ET thus training convergence arrives late.

The policy map transferred from Q-table after reinforcement learning training is picked with the optimal actions for maximum Q values in every state. From any initial position in the valid region, the policy map can guide the agent to reach the target. The multi-level PCM used for ET during training can be reused to save the policy map for reinforcement learning inference to further reduce hardware costs. The conductance distributions of 4 states (1000 d./state) are without any overlap between any 2 states for more than 11 h, therefore the policy at one position can be mapped to 1 conductance state in a PCM cell. Even with no overlap in the resistance distribution, fixed thresholds may still fail to distinguish these 4 states due to CD, especially within the time range of 0.5 h right after programming. As a result, faults in the stored policy map may cause the failure of the navigation. To avoid such storage faults, the global drift compensation is taken by sampling 10% devices to estimate the mean change factor and correct the conductance of the whole table. Distribution shift is well inhibited subsequently; the storage faults vanish even in larger time scales ($\sim$11 h).

• Task II: mountain car. In order to demonstrate the generalization capability of the PCM-ET method in different reinforcement learning tasks, Task II is representative of the continuous state reinforcement learning problems (Figure 8(d)). In this task, a car with weak power needs to climb up the hill to arrive position of the red flag. The motor of the car is so weak that the driver must learn to accumulate adequate gravitational potential energy from limited traction gradually instead of direct drive to the flag. One epoch of training ends once the traction count is over 1000 with a reward of 1/step or the car reaches the flag with a reward of 100. The state of the car is discretized to train the agent by SARSA (λ) and ϵ-greedy algorithms. Simulation results show that the ET also leads to an earlier convergence. Considering the convergence speed and quality of policy (the fewer steps the better), the optimal decay factor is in the range of 0.9–0.95. PCM-CD can directly implement this slow decay without amplification and reach excellent training performance (12.5–25 μS). The well-trained policy map can guide the car to swing back and forth to get enough velocity to escape the valley and reach the flag position based on the discretized car states. Besides, this policy map can also be saved in PCM with high density and long retention as aforementioned in Task I.

PCM-ET requires no external excites (no energy consumption) except for the partial SET operation during ET update. The proposed scheme yields 201× lower energy consumption compared with the decay calculation in NVIDIA A100 GPU. Moreover, the energy cost can be further reduced by about 3 orders due to the in-memory decay of PCM-ET compared to the conventional methods with frequent data moving.

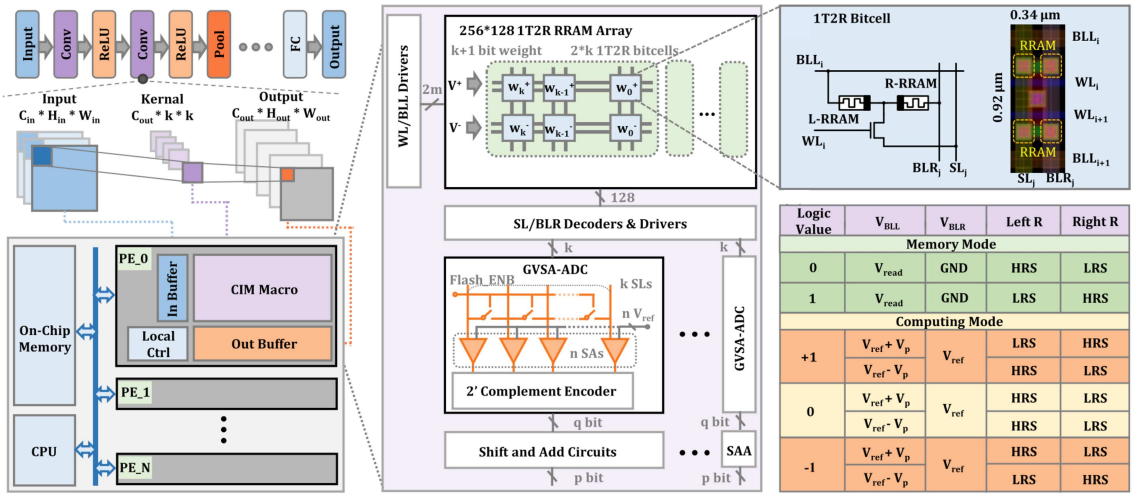

Figure 9 (Color online) System diagram of the 1T2R voltage sensing CIM accelerator [97] © 2022 IEEE.

4.2 A voltage sensing 1T2R memristor array architecture for CIM accelerators

Besides device-level innovation, device-circuit codesign are necessary to build large-scale memristive computing systems [88–92]. There are three major challenging aspects for the CIM accelerators to execute highly-parallel VMM. (a) Device uniformity. The process variation of memristor bitcells inflicts vast accuracy loss in the form of adding the noise to the stored synaptic weights, which necessitates the process and circuit techniques to improve the device uniformity. (b) Minimized power consumption at fast computing speed. The current sensing scheme of CIM applies constant electrical excitations upon the devices amid computation, subsequently causing large power consumption heavily depending on the memristor resistivity. (c) Circuit flexibility. There exists a scaling coefficient between the CIM input signals and the output signals, which makes it very difficult to alter CIM circuits for different computing range [93–96].

To ameliorate these problems, Jing et al. [97] proposed a 1-transistor-2-memristor (1T2R) bitcell structure suitable for voltage sensing to perform CIM VMM with boosted efficiency and flexibility. Figure 9 shows the circuit scheme and the 1T2R bitcell structure. Two memristor devices are connected in a "head-to-tail" manner and a transistor connects the joint node of the two memristors. The proposed 1T2R bitcell shows an area of $97.8F^2$ ("F" is the feature size), which is slightly larger than the common 1T1R design (60–80 F^2). Nevertheless, this 1T2R bitcell is sensed to obtain the relative voltage of the joint node between two memristors. Because of the locality of the process variation distribution, this voltage sensing scheme does not rely solely on the absolute value of the resistance value of the memristor devices. Therefore, the uniformity is enhanced. During computation, both positive and negative pulses are given into different bit lines, which are statistically complementary to neutralize the constant DC current within the source lines. In this way, the CIM power consumption with high input parallelism can be largely saved. This work is benchmarked with widely used deep neural networks for the recognition tasks on CIFAR10 dataset [22]. It yields an energy efficiency as high as 39.52 TOPS/W with simulated verification at 40 nm CMOS technology node.

4.3 1-HEMT-1-memristor CIM and logic technology

Modern semiconductor process platforms for implementing Turing-complete computers should not only embrace neural networks but also support logic and stochastic operators [98–103]. Dang et al. [104] demonstrated a fabrication process with AlGaN/GaN high-electron-mobility transistor (HEMT) and Au/NbO_x/ HfO_2/Pt memristors toward homomorphic encryption computation tasks. A typical application scenario of homomorphic encryption is processing the encrypted data on artificial intelligence and Internet of Things (AIoT) devices, where power and energy are essential factors for the implementation. There are mainly three key components in the homomorphic encryption and processing of secure data: convolutional neural network (CNN), encryption implemented by XOR logic gates, and random number generator. Such a compound function can be achieved by the combination of memristive devices: one-AlGaN/GaN-HEMT one-Au/NbO_x/HfO_2/Pt-memristor (1HT1R) bitcell arrays for CNN, HEMT-based circuits for XOR logic gates, and Pt/SiO_x:Ag/Pt memristors for true random number generator

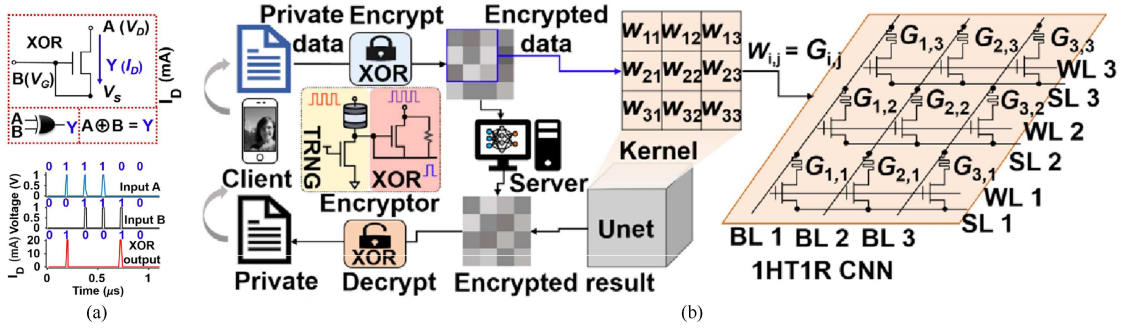

Figure 10 (Color online) (a) HEMT XOR logic gate; (b) privacy-reserved memristive processing system [104] © 2022 IEEE.

(TRNG). In a 1HT1R bitcell, one of the two terminals of the memristor connects to the drain terminal of the HEMT. The HEMT serves as the selecting device to avoid sneak paths in the array configuration. The 1HT1R bitcell yields <8 ns resistance switching latency. And it only takes an average energy cost of 96 fJ/bit for the programming. The 1HT1R performs CIM VMM [104] with fast switch-on/off latency thanks to the HEMT selector. For the XOR logic gate implementation, a single HEMT is leveraged with shorted gate and source terminals, as shown in Figure 10(a).

Dang et al. [104] built a hardware encryptor for privacy data processing with the aforementioned combination of HEMT and memristive devices. As shown in Figure 10(b), the exemplary privacy-reserved processing system can perform pixel-level XOR with a private key (i.e., a random noise image generated by TRNG with the same resolution as the target image). Then low-power 1HT1R-based CIM component conducts cognitive processing with CNN for the image segmentation [105, 106].

This HEMT/memristor hybrid process opens up the possibility of implementing high-performance AIoT secure processing with limited power and energy budgets. From the application perspective, HEMT/memristor integration offers an alternative solution to the implementation in designing domain-specific logic operations. State-of-the-art CIM accelerator designs use memristor logic-in-memory [107–110]. However, there lie concerns about memristor device endurance and relatively long operational latency (∼nanoseconds) in such designs. Instead, transistor-based digital logic within or aside bitcell arrays would be mature to achieve fast and repetitive logic operations [61]. Following this approach, HEMT showcases better performance than conventional silicon-based transistors in realizing logic circuits.

5 Conclusion and perspective

We have reviewed the representative studies in the field of memristive dynamics-enabled bionic computing systems as well as memristive sensory computing systems. Memristive devices have illuminated the way for highly efficient computing paradigms. Even though the demonstration is limited by small-scale demonstration, the dynamics have showcased an intricated analogy of the memristive device to the biological neuron and synapses in various forms to construct neuromorphic computing systems.

Note that, introducing memristive dynamics and adaptability into bio-inspired computing is never to replace all conventional architectures of computers. Rather, the novel memristive dynamics pave a new path to realize specialized computing hardware. As can be observed, the example applications shown in this paper mostly center on pattern recognition and image (two-dimensional)/speed (one-dimensional) signal processing. In that specialized hardware, the fusion of computing, storage, and sensory units endows the neuromorphic computing systems with high power and energy efficiency, and scalability in the device form factors. They are basically a response to the fast-growing AIoT markets. Besides, the reviewed memristor-based computing systems are able to scale up and down for various computing workloads.

Neuromorphic computing system naturally mimics the biological neural system to fulfill emerging cognitive computing jobs. Admittedly, bio-inspired computing hardware, for the moment, will be well-matched to perform large-scale perceivable signal processing, especially those that can be converted and solved by spiking or deep neural networks. Beyond this, with the help of complex memristive dynamics, we are expecting to solve the most difficult computing problems today by mimicking the human brain, for example, chaotic systems, and combinatory problems with transcendentally large search space.

To address these perspectives, future research on memristive-dynamics-based neuromorphic computing systems should focus on (a) discovering more dynamics with the help of material and device engineering; (b) matching the novel dynamics of nanoscale electron devices to the advanced neuromorphic computing models; (c) develop fabrication technologies that are appropriate for VLSI circuit implementation, especially developing the processes to be compatible with mature silicon CMOS platforms. Potential solutions root in the interdisciplinary investigations on semiconductor process engineering, neuromorphic computing algorithms, and in-memory computing system design.

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