SCIENCE CHINA
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• Supplementary File •

# GaN-based artificial optoelectronic neural circuit with multilevel synapses cascade for neuromorphic computing

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## Appendix A The fabrication process, morphology characterization, and energy band structure of the proposed devices

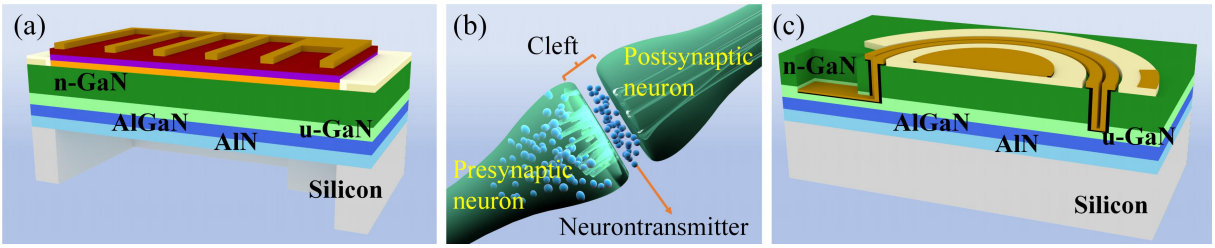



**Figure A1** (a) Cross-sectional schematic diagram of the synaptic diode. (b) Schematic diagram of a biological synapse. (c) Cross-sectional view of the synaptic MOSFET.

The synapses within the biological nervous system are depicted in Figure 1(b). Upon stimulation of neurons, presynaptic neurons generate action potentials, which propagate to the presynaptic membrane and get encapsulated by vesicles. Subsequently, the presynaptic membrane channels open, allowing vesicles laden with neurotransmitters to detach from the presynaptic membrane and discharge their contents into the synaptic cleft. When these neurotransmitters bind to receptors on the postsynaptic membrane, channels on the latter open, decreasing the membrane potential of the postsynaptic membrane. This leads to local polarization and elicits a postsynaptic potential. Figure 1(a) and 1(b) respectively show the cross-sectional schematic diagrams of the GaN-based synaptic diode as the IS and the GaN-based synaptic MOSFET as the OS. Specifically, the Si substrate at the bottom of the synaptic diode is graphically etched to form a large thin film. This enables light to be irradiated onto the synaptic diode from the backside and prevents the light from being absorbed by the Si substrate. The material of the drain and source of the synaptic MOSFET is n-GaN, and the u-GaN layer is chosen as the gate channel, resulting in the formation of an N-channel enhancement-mode MOSFET.

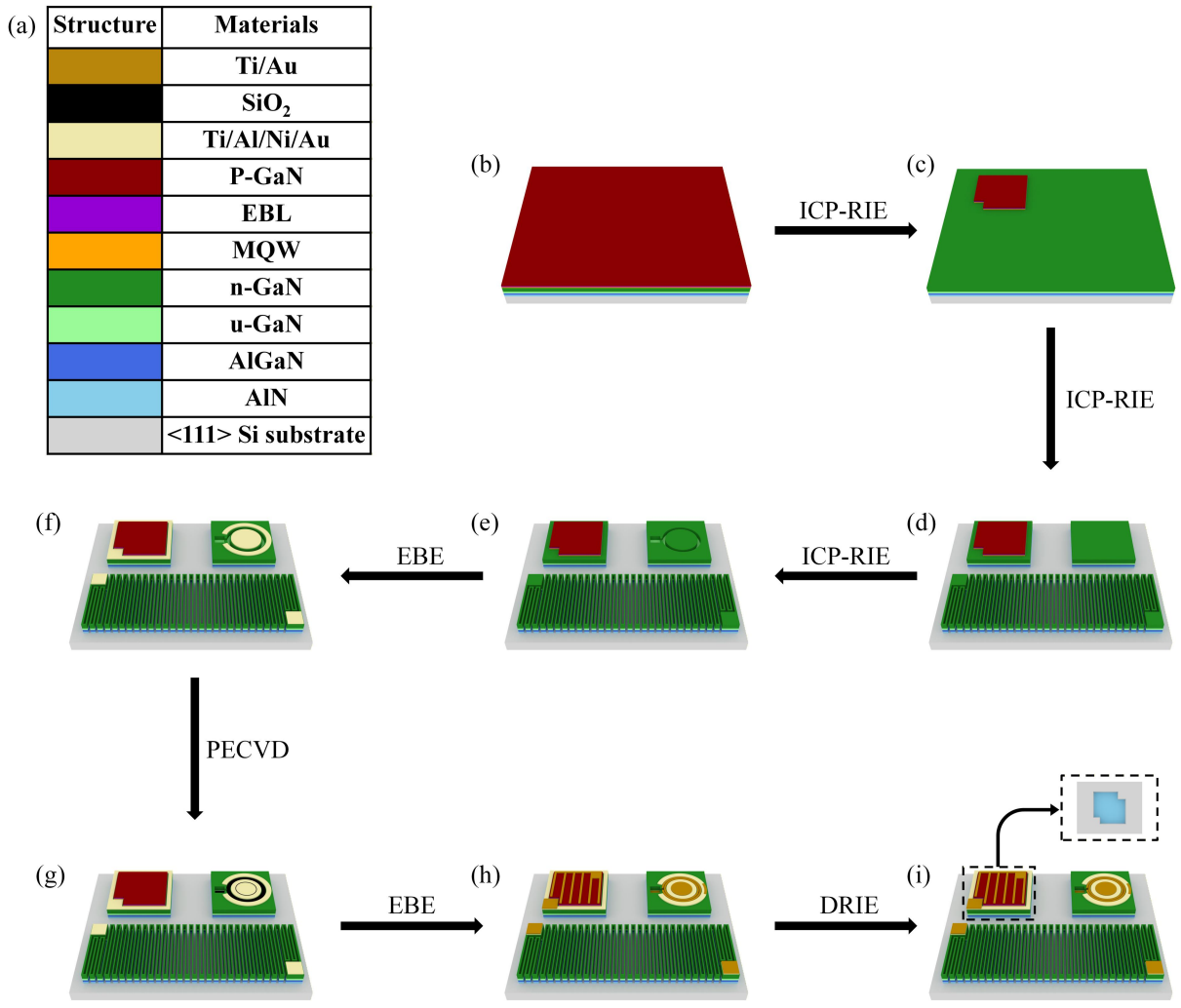



**Figure A2** (a) Epitaxial layer structure of the proposed device. (b) ∼ (i) Fabrication process flow of the proposed device.

The fabrication process of the proposed cascaded synaptic device structure is illustrated in Figure A1, with Figure A2(a) showing the final layer architecture after processing. The epitaxial structure was grown by metal-organic chemical vapor deposition (MOCVD), consisting of a 265 nm AlN layer, a 670 nm AlGaN layer, a 800 nm undoped GaN layer (u-GaN, referring to GaN without intentional doping, typically regarded as intrinsic or near-intrinsic GaN), a 2800 nm n-doped GaN layer (n-GaN, referring to GaN intentionally doped with donor impurities, where Si is used as the n-type dopant), 9 pairs of InGaN (quantum well)/GaN (quantum barrier) multiple quantum well (MQW) with thickness of 100 nm, a 25 nm electron blocking layer (EBL), and a 90 nm p-doped GaN layer (Mg was used as the p-type dopant). The detailed fabrication process, as shown in Figure A2(b-i), begins with inductively coupled plasma reactive ion etching (ICP-RIE) to pattern the active region of the synaptic diode by etching from the p-GaN down to the n-GaN layer. Subsequent ICP-RIE etching creates isolation trenches reaching the silicon substrate to separate individual devices while simultaneously forming folded resistor structures. Additionally, ICP-RIE etching exposes the u-GaN channel layer to define the gate channel for the synaptic MOSFET. Ohmic contacts are then formed through electron beam evaporation (EBE) of Ti/Al/Ni/Au (20/200/20/160 nm) stacks for source/drain electrodes of the synaptic MOSFET, cathode contacts for the synaptic diode, and the resistor electrodes, followed by rapid thermal annealing (RTA) to improve contact properties. A 120 nm $SiO_2$ dielectric layer is deposited via plasma enhanced chemical vapor deposition (PECVD) and patterned using buffered oxide etchant (BOE) wet etching. Gate electrodes for the synaptic MOSFET, anode contacts for the synaptic diode, and remaining test pads are formed by EBE deposition and patterning of Ni/Au (20/200 nm). Finally, deep reactive ion etching (DRIE) removes the Si substrate beneath the patterned p-GaN regions of the synaptic diode to enable backside optical illumination.

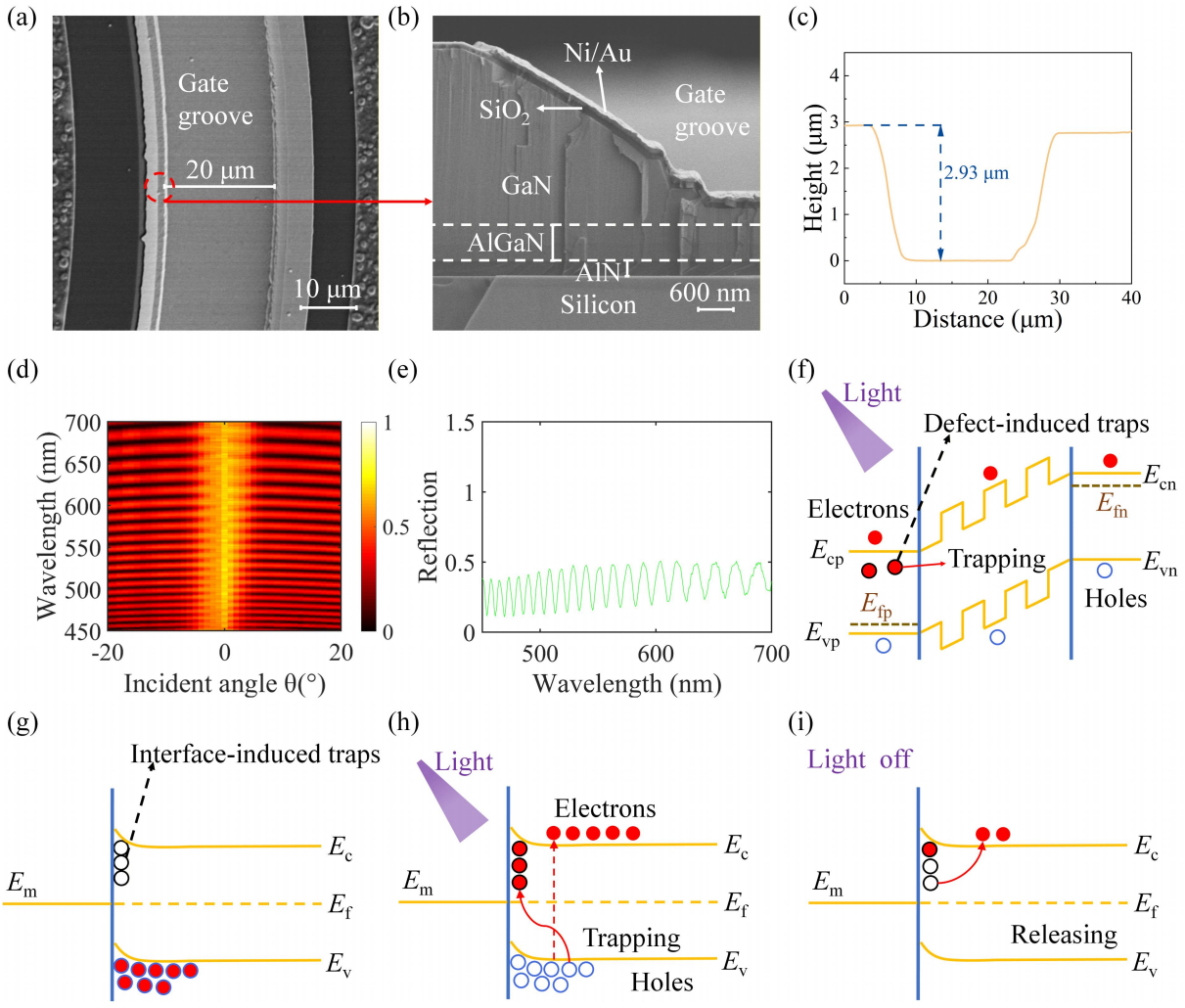



**Figure A3** (a) SEM image of the gate groove in the synaptic MOSFET. (b) Cross-sectional SEM image of the left side wall of the gate groove in the synaptic MOSFET. (c) Etching depth of the gate groove in the synaptic MOSFET. (d) Angular resolution reflection spectra of the 4.846 μm thick thin film of the synaptic diode. (e) Resonance peak of the synaptic diode (lines drawn under the vertical condition of reflection spectrum). (f) Energy band diagram showing carriers trapping behavior in the synaptic diode under UV illumination. (g) Energy band diagram showing carriers distribution in the synaptic MOSFET under dark conditions. (h) Energy band diagram showing carriers trapping behavior under UV illumination. (i) Energy band diagram showing carriers releasing behavior upon returning to dark conditions.

The scanning electron microscopy (SEM) image of the gate groove in the synaptic MOSFET is presented in Figure A3(a), with an etched groove width of 20 μm. Figure A3(b) displays a cross-sectional SEM image of the employed epitaxial layers (GaN/AlGaN/AlN), where distinct stratification is observable, with the u-GaN layer serving as the gate channel. The corresponding horizontal profile along the channel is shown in Figure A3(c), revealing a measured gate groove height of 2.93 μm. Figure A3(d) provides an angular resolution reflection spectra of the synaptic diode, demonstrating the thin film thickness after DRIE of the Si substrate, which facilitates backside illumination of the device. Resonance peak of the synaptic diode is shown in Figure A3(e). The synaptic diode after DIRE etching exhibits 21 resonance modes under incident light wavelengths ranging from 450 to 700 nm, and the thin film thickness of the synaptic diode is calculated to be 4.846 μm based on the formulated methodology. The formula for calculation is as follows:

$$L = \frac{m\lambda}{2\mathrm{n}}, \tag{A1}$$

where the integer $m$ represents the order of the resonant mode, $\lambda$ denotes the wavelength of the incident light, n is the refractive index of the thin film, and $L$ corresponds to the thickness of the thin film. The synaptic functionality of the device fundamentally arises from its charge storage effect, which is the dynamic characteristics caused by the accumulation and release of charge carriers in the channel. Figure A3(f) shows the energy band diagram of the synaptic diode under ultraviolet (UV) illumination. Defects introduced during material growth, device fabrication, and ion bombardment in the ICP etching process, which damages the etched interface, inevitably generate deep-level states in the top p-type region and near the etched surface. These defects create trap levels within the bandgap and act as charge storage centers. Under UV illumination, photons with energies equal to or greater than the semiconductor bandgap excite electrons from the

valence band to the conduction band, generating electron-hole pairs. Since the defect levels are typically located below the conduction band edge, photogenerated electrons can be captured and stored in these trap states. After the illumination is removed, the trapped electrons are gradually released by thermal activation over the energy barrier associated with the trap levels. This slow trapping and releasing process results in persistent photoconductivity (PPC) effect. Figures A3(g-i) illustrate the energy band diagrams of the synaptic MOSFET under different operating conditions. As shown in Figure A3(g), trap states are formed at the gate dielectric/channel interface due to defects introduced during the $SiO_2$ deposition process. Under UV illumination (Figure A3(h)), photogenerated electrons drift toward the channel region and are captured by these interface trap states. When the illumination is turned off (Figure A3(i)), the photogenerated carriers recombine while the trapped electrons are gradually released. The delayed release of electrons leads to a slow decay of the channel current, producing a PPC effect and enabling the synaptic behavior of the device.

## Appendix B The optoelectronic and synaptic characteristics of the proposed devices

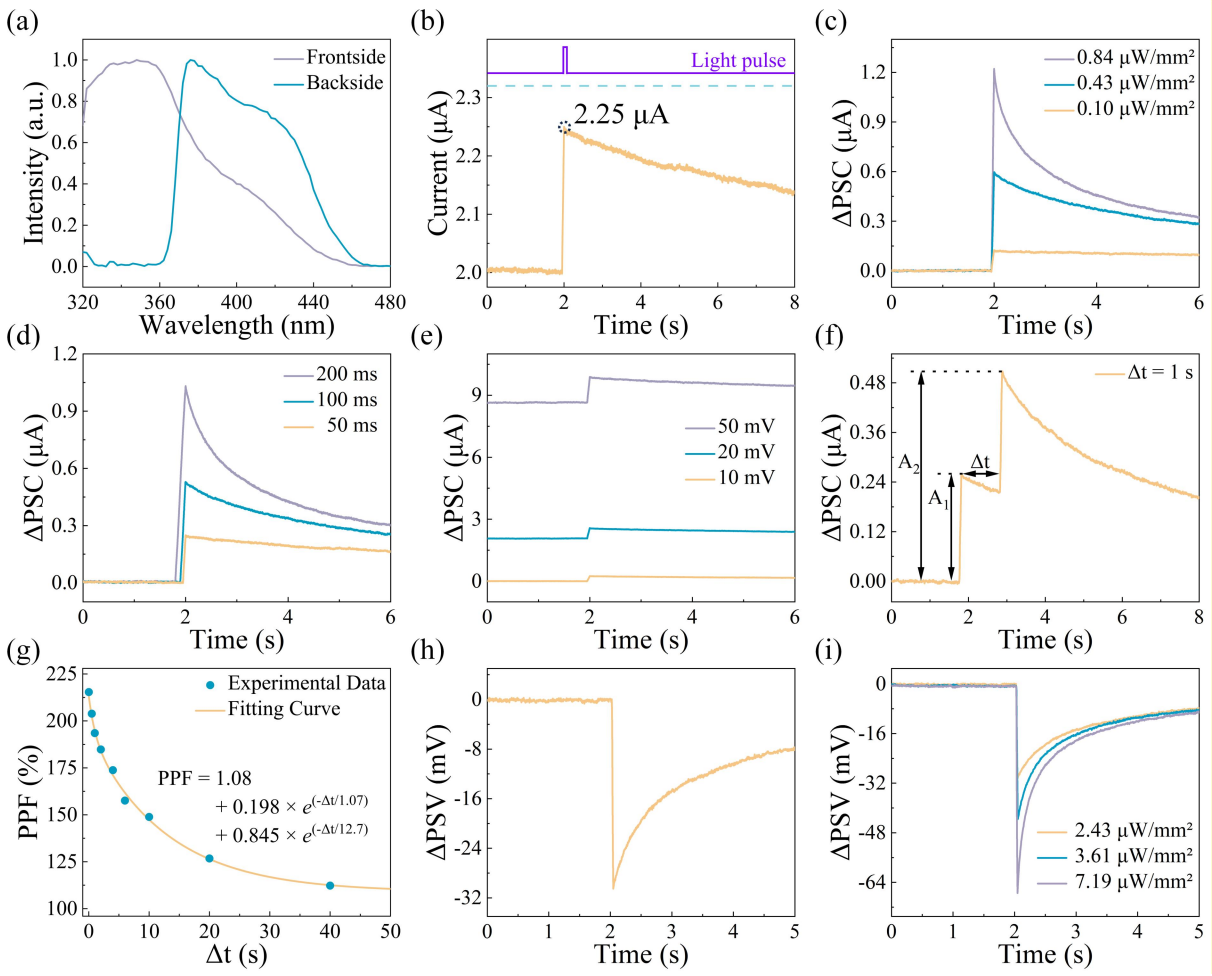



**Figure B1** (a) Spectral response of the synaptic diode's frontside and backside. (b) Raw EPSC of the synaptic diode induced by a light pulse before data processing (375 nm wavelength, 50 ms pulse width, 0.26 μW/mm$^2$ light intensity, and 10 mV bias). (c) EPSCs under different light intensities (375 nm wavelength, 50 ms pulse width, and 10 mV bias). (d) EPSCs induced in the synaptic diode under different pulse width conditions (375 nm wavelength, 0.26 μW/mm$^2$ light intensity, and 10 mV bias). (e) EPSCs induced in the synaptic diode under different bias conditions (375 nm wavelength, 50 ms pulse width, and 0.26 μW/mm$^2$ light intensity). (f) PPF behavior induced by two consecutive light pulses (375 nm wavelength, 50 ms pulse width, 0.26 μW/mm$^2$ light intensity, 10 mV bias, and 1 s pulse interval). (g) PPF index as a function of pulse interval. (h) PSV output from the synaptic diode in series with a resistor for voltage division (375 nm wavelength, 20 ms pulse width, 2.43 μW/mm$^2$ light intensity, and -5 V bias). (i) PSV induced by different light intensities (375 nm wavelength, 20 ms pulse width, and -5 V bias).

Figure B1(a) displays the spectral responses of the synaptic diode's frontside and backside, reflecting the device's light absorption characteristics. It can be observed that the two sides exhibit different spectral responses. This difference in spectral response originates from the different optical absorption paths within the device structure. When light is incident from the backside, it first propagates through the buffer layer. Photons with shorter wavelengths are partially absorbed in the buffer layer because their photon energies exceed the effective bandgap of the layer. In contrast, photons with longer wavelengths can penetrate through the buffer layer and are subsequently absorbed by the GaN and MQW layers, leading to a dominant photoresponse around 376 nm. Under frontside illumination, the incident light directly reaches the GaN and MQW layers without passing through the buffer layer. As a result, high-energy photons in the shorter wavelength region can be more effectively absorbed, leading to an enhanced photoresponse at shorter wavelengths. Figure B1(b) present the raw EPSC signals of the synaptic diode induced by a light pulse. Upon illumination, the diode generates a high density of photogenerated carriers, causing a rapid current increase. Concurrently, defects in the p-type region become populated by these carriers, as shown in Figure A3(f). When illumination ceases, photogenerated electrons and holes recombine, leading to current decay. However, the gradual release of carriers from defects slows the decay rate, producing synaptic behavior. This transient current is thus termed the PSC. The peak EPSC current of the synaptic diode is 2.25 μA. The energy consumption is calculated using the following equation:

$$E = I_{\text{peak}} \times t \times V_{\text{bias}}, \tag{B1}$$

where $I_{\text{peak}}$ represents the peak current of the EPSC and t denotes the optical pulse width. Based on this equation, the energy consumption of the EPSC induced by a light pulse is calculated to be 1.125 nJ for the synaptic diode. Figures B1(c-e) show the light induced EPSCs under different light intensities, pulse widths, and bias conditions. paired-pulse facilitation (PPF) is a critical phenomenon in neuromorphic computing and synaptic plasticity research, and serves as a fundamental mechanism for diverse synaptic activities. The PPF index can be defined as:

$$\text{PPF} = \frac{A_2}{A_1}, \tag{B2}$$

where $A_1$ and $A_2$ represent the amplitudes of the first and second EPSCs, respectively. Figure B1(f) demonstrates the typical PPF behavior under two consecutive optical pulses. Figure B1(g) reveals that the amplitude of the second response decreases as the pulse interval ($\Delta t$) increases. This decay behavior can be mathematically described by:

$$\text{PPF} = C_0 + C_1 \times \exp(-\frac{\Delta t}{\tau_1}) + C_2 \times \exp(-\frac{\Delta t}{\tau_2}), \tag{B3}$$

where $C_1$, $C_2$, $\tau_1$, and $\tau_2$ represent the initial magnitude and characteristic relaxation time of the fast and slow phase. The relaxation times of the synaptic diode obtained from Figure 3(e) are $\tau_1 = 1.07$ s and $\tau_2 = 12.7$ s.

The synaptic diode was connected in series with a resistor to form a voltage divider circuit, with its output designated as the postsynaptic voltage (PSV). As shown in Figure B1(h), the PSV output from the voltage divider circuit was obtained when the synaptic diode was stimulated by a light pulse. It can be seen that under -5 V bias, PSV, like inhibitory post-synaptic current (IPSC), also has synaptic curves and depression ability. Figure B1(i) demonstrates PSV variations under light pulses of different light intensities. The PSV output effectively modulated the MOSFET's operational characteristics when applied to the gate terminal of the synaptic MOSFET.

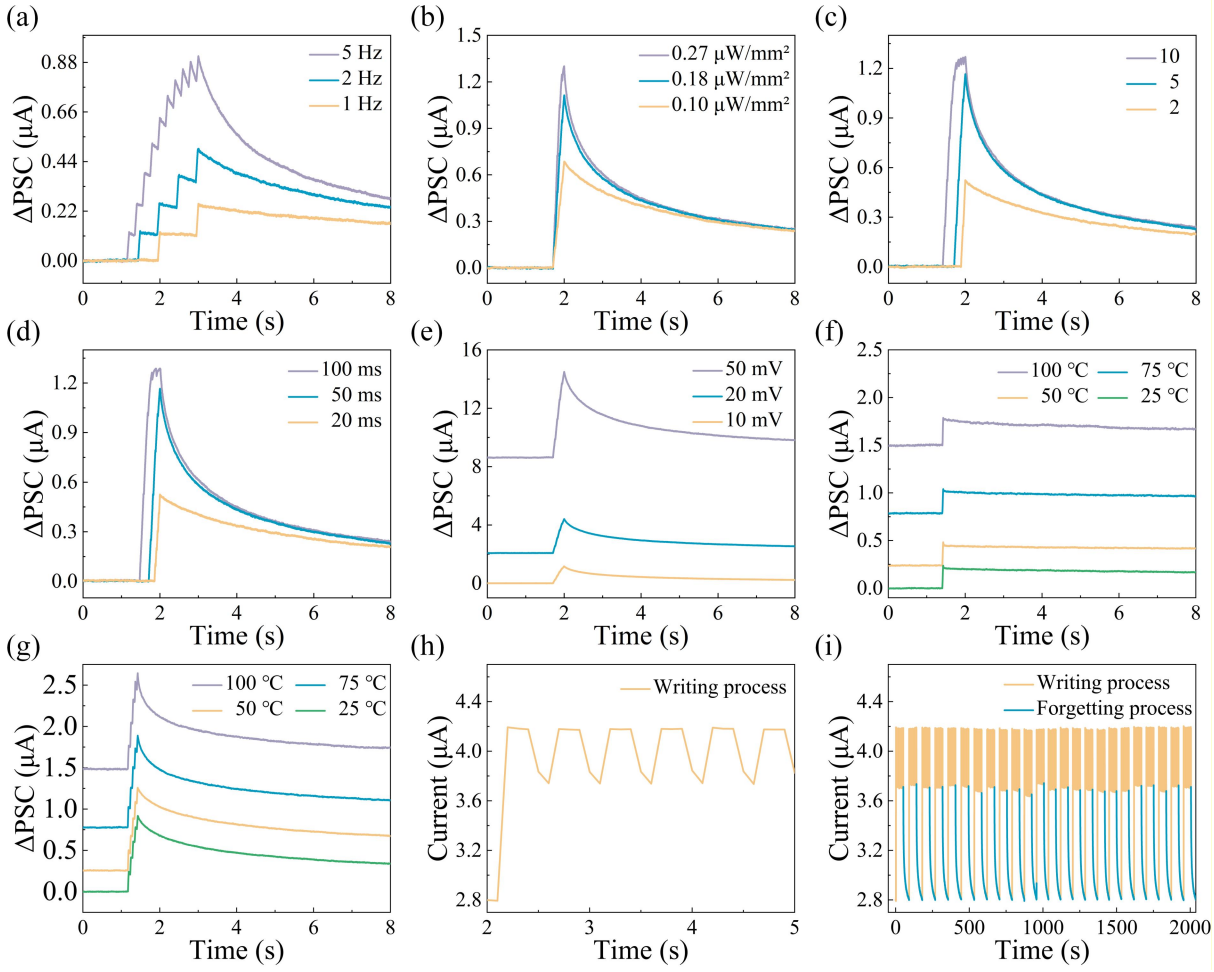



**Figure B2** (a) STP to LTP transition induced by frequency-varied light pulses (375 nm wavelength, 50 ms pulse width, 0.10 μW/mm$^2$ light intensity, 10 mV bias, and 2 s duration). (b) STP to LTP transition induced by different light intensities (375 nm wavelength, 50 ms pulse width, 10 mV bias, 10 ms pulse interval, and 5 pulses). (c) Transition from STP to LTP achieved in the synaptic diode under varying numbers of light pulses (375 nm wavelength, 0.26 μW/mm$^2$ light intensity, 50 ms pulse width, 10 mV bias, and 10 ms pulse interval). (d) STP to LTP transition under different pulse widths (375 nm wavelength, 0.26 μW/mm$^2$ light intensity, 5 light pulses, 10 mV bias, and 10 ms pulse interval). (e) STP to LTP transition under different bias conditions (375 nm wavelength, 0.26 μW/mm$^2$ light intensity, 50 ms pulse width, 5 light pulses, and 10 ms pulse interval). (f) EPSCs of the synaptic diode induced by a light pulse under different temperatures (375 nm wavelength, 50 ms pulse width, 5.83 μW/mm$^2$ light intensity, and 10 mV bias). (g) Transition from STP to LTP of the synaptic diode under different temperatures (375 nm wavelength, 50 ms pulse width, 5.83 μW/mm$^2$ light intensity, 10 mV bias, 10 ms pulse interval, and 5 light pulses). (h) Light writing process of the synaptic diode (375 nm wavelength, 250 ms pulse width, 250 ms pulse interval, 4.97 μW/mm$^2$ light intensity and 10 mV bias). (i) Repeated cycles of 100 light pulses for writing followed by natural forgetting over a total duration of 2000 s.

The key to biological neural learning lies in long-term plasticity (LTP), which can be achieved through repetitive training with multiple consecutive pulses that drive the transition from short-term plasticity (STP) to LTP. As shown in Figure B2(a), the STP to LTP transition was induced by optical pulses of varying frequencies. The PSC amplitude exhibited frequency-dependent enhancement, reaching saturation at 5 Hz stimulation. This saturation likely reflects an equilibrium between the photogenerated carriers generation and recombination processes. Figure B2(b-e) shows the STP to LTP conversion under different light intensities, numbers of light pulses, pulse widths, and bias conditions. To investigate the operational performance of the synaptic diode at different temperatures, EPSCs and the transition from STP to LTP were measured in the temperature range from 25 °C to 100 °C, as shown in Figure B2(f) and B2(g). As the temperature increases, the baseline current of the synaptic diode shows a noticeable rise. This behavior is mainly attributed to the enhanced thermal excitation effect in the device under elevated temperatures, which increases defect-assisted carrier transport and consequently raises the dark current. In contrast, the photocurrent increment induced by the light pulse remains nearly unchanged, indicating that under low-bias conditions the photogenerated carrier generation process is relatively insensitive to temperature. In addition, the stability of the device under repeated optical pulse stimulation was also characterized, as presented in Figure B2(h) and B2(i). Figure B2(h) presents the optical writing process of the synaptic diode, while Figure B2(i) shows the repeated experiment in which 100 light pulses were applied for writing, followed by a natural forgetting process, with a total duration of 2000 s. These results demonstrate that the device exhibits good stability.

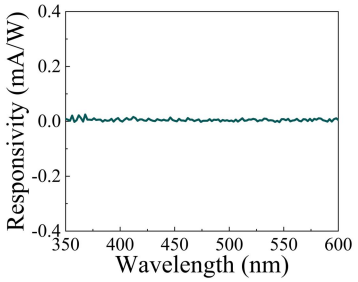



**Figure B3** Spectral response of the resistor.

Figure B3 shows the spectral response of the resistor, which confirms that the resistor does not generate photocurrent under illumination and therefore does not affect the output of the circuit.

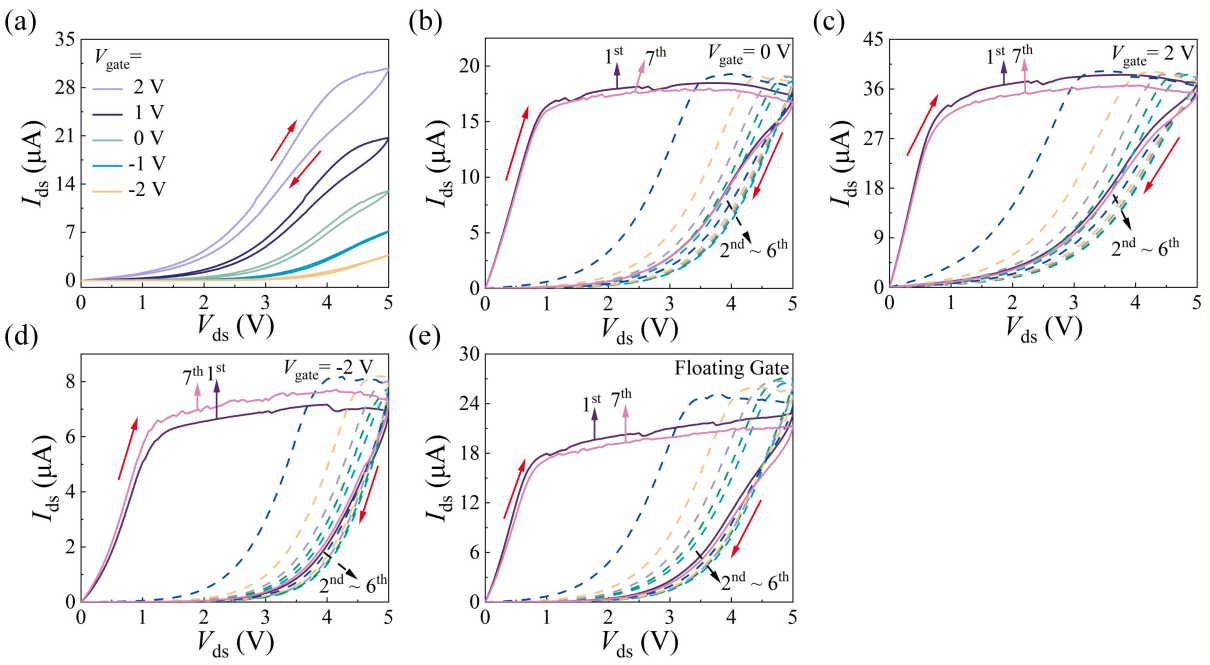



**Figure B4** (a) Output characteristic curves with bidirectional scanning under various $V_{gate}$ of the synaptic MOSFET. (b) Hysteresis behavior of the transistor output at 0 V $V_{gate}$. (c) Hysteresis in the output characteristics of the synaptic MOSFET at $V_{gate}$ = 2 V. (d) Hysteresis in the output characteristics at $V_{gate}$ = -2 V. (e) Hysteresis in the output characteristics at floating gate state.

Figure B4(a) illustrates the output characteristic curve with bidirectional sweeps under various gate voltages ($V_{gate}$). Increasing $V_{gate}$ significantly enhances $V_{ds}$. A pronounced hysteresis emerges between forward and backward sweeps at higher $V_{gate}$, suggesting charge storage effect. To investigate whether the device has a stronger charge storage effect under illumination, the output characteristic curve was measured after prolonged light exposure. Figure B4(b-e) displays the hysteresis in the output characteristic curves of the device at varying $V_{gate}$. The $1^{st}$ curve represents the initial bidirectional sweep after 30 s of 375nm UV illumination, showing a clear hysteresis response. The $2^{nd} \sim 6^{th}$ and $7^{th}$ curves correspond to the second to sixth bidirectional sweeps in the dark and the seventh sweep after re-illumination for 30 s, respectively. The hysteresis gradually diminishes during consecutive measurements in the dark, but reappears distinctly after re-exposure to 30 s of illumination. This confirms that the device retains a substantial amount of photogenerated carriers, demonstrating its light-induced charge storage capability. The mechanism underlying the hysteresis in the synaptic MOSFET aligns with the energy band diagrams illustrated in Figure A3(g-i).

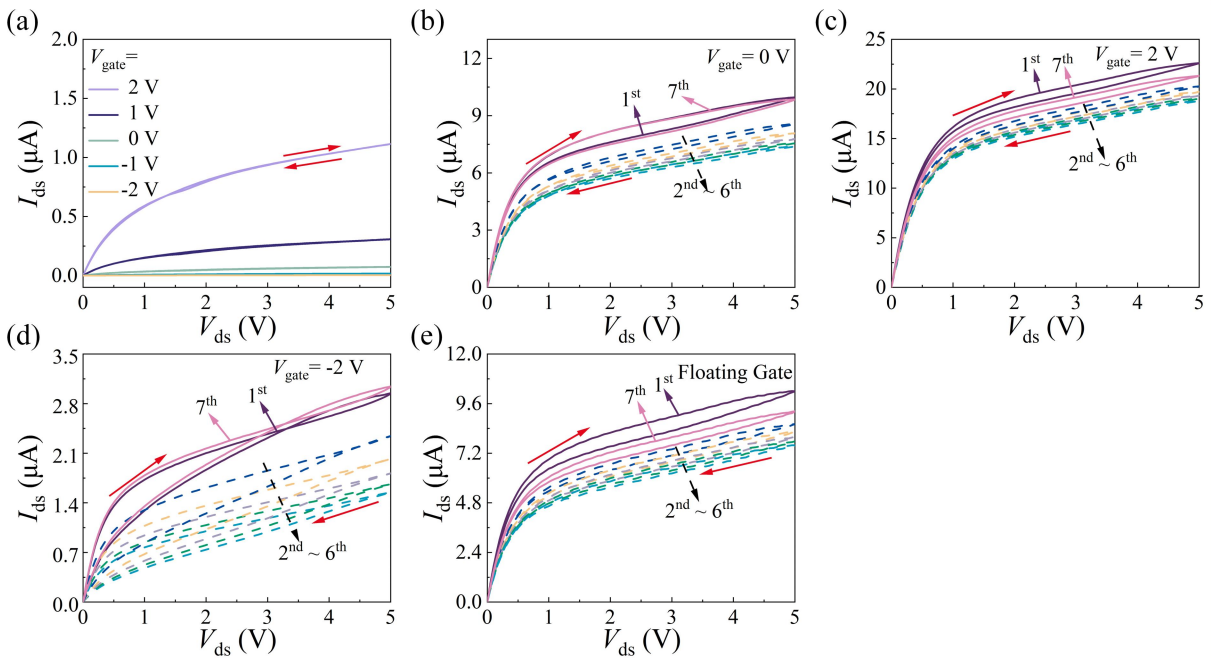



**Figure B5** (a) The bidirectional output characteristics of the synaptic MOSFET under source and drain terminals swapping test at varying $V_{\mathrm{gate}}$. (b) Hysteresis in the output characteristics under source and drain terminals swapping test at $V_{\mathrm{gate}}$ = 0 V. (c) Hysteresis in the output characteristics under source and drain terminals swapping test at $V_{\mathrm{gate}}$ = 2 V. (d) Hysteresis in the output characteristics under source and drain terminals swapping test at $V_{\mathrm{gate}}$ = -2 V. (e) Hysteresis in the output characteristics under source and drain terminals swapping test at floating gate state.

Notably, due to the ring structure of the synaptic MOSFET, the source and drain terminals are asymmetric, and distinct behaviors can be observed by swapping the source and drain terminals. The output characteristic curve of reverse testing is shown in Figure B5(a). Figure B5(b-e) displays the hysteresis in the output characteristic curves of reverse testing of the device at varying $V_{\mathrm{gate}}$.

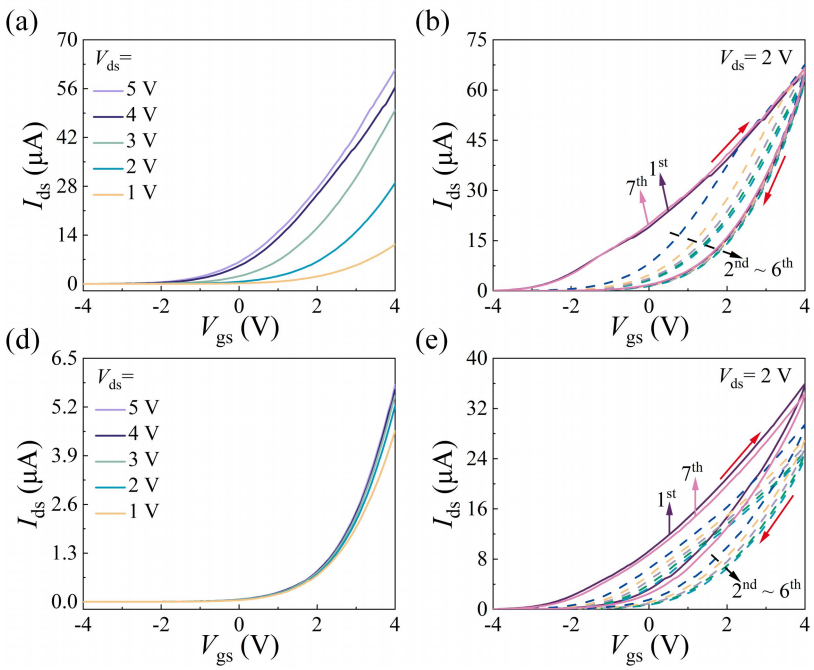



**Figure B6** (a) Transfer characteristics of the synaptic MOSFET at varying $V_{\mathrm{ds}}$. (b) Hysteresis in the transfer characteristics at $V_{\mathrm{ds}} = 2$ V. (c) Transfer characteristics under source and drain terminals swapping test at varying $V_{\mathrm{ds}}$. (d) Hysteresis in the transfer characteristics under source and drain terminals swapping test at $V_{\mathrm{ds}} = 2$ V.

Hysteresis is also observed in the transfer characteristic curve. The transfer characteristic curve of the synaptic MOSFET is shown in Figure B6(a). Figure B6(b) displays the hysteresis in the transfer characteristic curve at 2 V $V_{\mathrm{ds}}$. The transfer characteristic curve of reverse testing is shown in Figure B6(c). Figure B6(d) presents the hysteresis in the transfer characteristic curves of reverse testing at 2 V $V_{\mathrm{ds}}$.

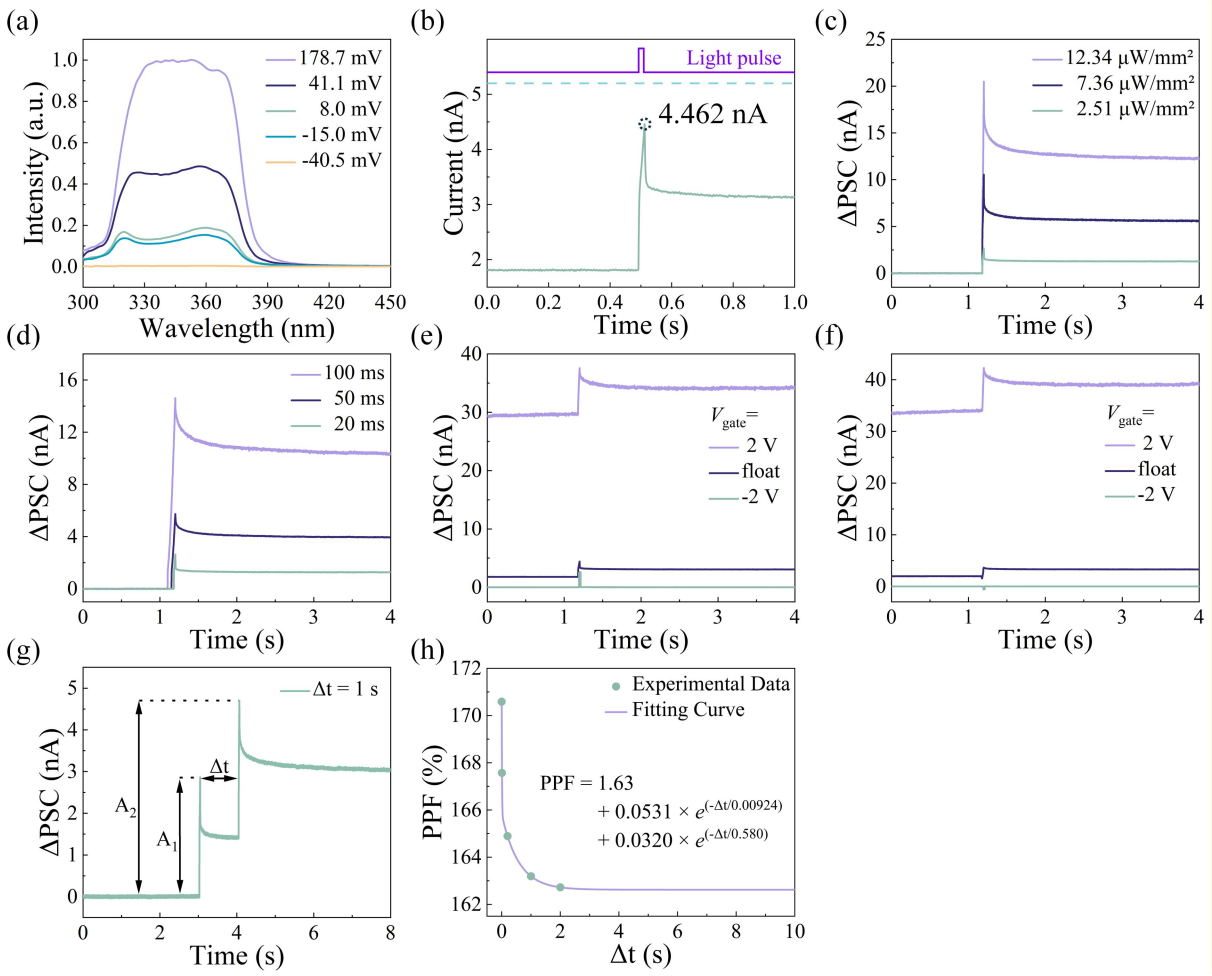



**Figure B7** (a) Spectral response of the synaptic MOSFET under different $V_{ds}$. (b) Raw EPSC of the synaptic MOSFET induced by a light pulse before data processing (375 nm wavelength, 0.26 μW/mm$^2$ light intensity, and 10 mV bias). (c) EPSC modulation under different light intensities (375 nm wavelength, 20 ms pulse width, float gate state, and 1 mV $V_{ds}$). (d) EPSCs induced in the synaptic MOSFET under varying pulse widths (375 nm wavelength, 2.51 μW/mm$^2$ light intensity, floating gate state, and 1 mV $V_{ds}$). (e) EPSCs induced at different $V_{gate}$ (375 nm wavelength, 20 ms pulse width, 2.51 μW/mm$^2$ light intensity, and 1 mV $V_{ds}$). (f) EPSCs induced under source and drain terminals reverse testing at different $V_{gate}$ (375 nm wavelength, 20 ms pulse width, 2.51 μW/mm$^2$ light intensity, and 1 mV $V_{ds}$). (g) PPF behavior induced by two consecutive light pulses (375 nm wavelength, 20 ms pulse width, 2.75 μW/mm$^2$ light intensity, float gate state, 1 mV $V_{ds}$, and 1 s pulse interval). (h) PPF index as a function of pulse interval.

Figure B7(a) shows the spectral response under different drain-source bias voltages ($V_{ds}$). The photoresponse intensity increases with higher $V_{ds}$, attributed to enhanced separation efficiency of photogenerated carriers under stronger electric fields. The device exhibits broad spectral responsivity, indicating excellent wavelength selectivity for multi-band optical detection. Figure B7(b) present the raw EPSC signals of the synaptic MOSFET induced by a light pulse. Specifically, the peak EPSC current of the synaptic MOSFET is 4.462 nA. According to Equation (B1), the energy consumption of the EPSC induced by a light pulse is calculated to be 89.24 fJ for the synaptic MOSFET. Figures B7(c-e) show the light induced EPSCs under different light intensities, pulse widths, and $V_{gate}$ conditions. Figures B7(f) presents the EPSCs induced under source and drain terminals reverse testing at different $V_{gate}$. Figure B7(g) illustrates the PPF behavior under two consecutive light pulses. Figure B7(h) displays that the amplitude of the second response decreases as the $\Delta t$ increases. The relaxation times of the synaptic MOSFET obtained from Figure B7(h) are $\tau_1 = 0.00924$ s and $\tau_2 = 0.580$ s.

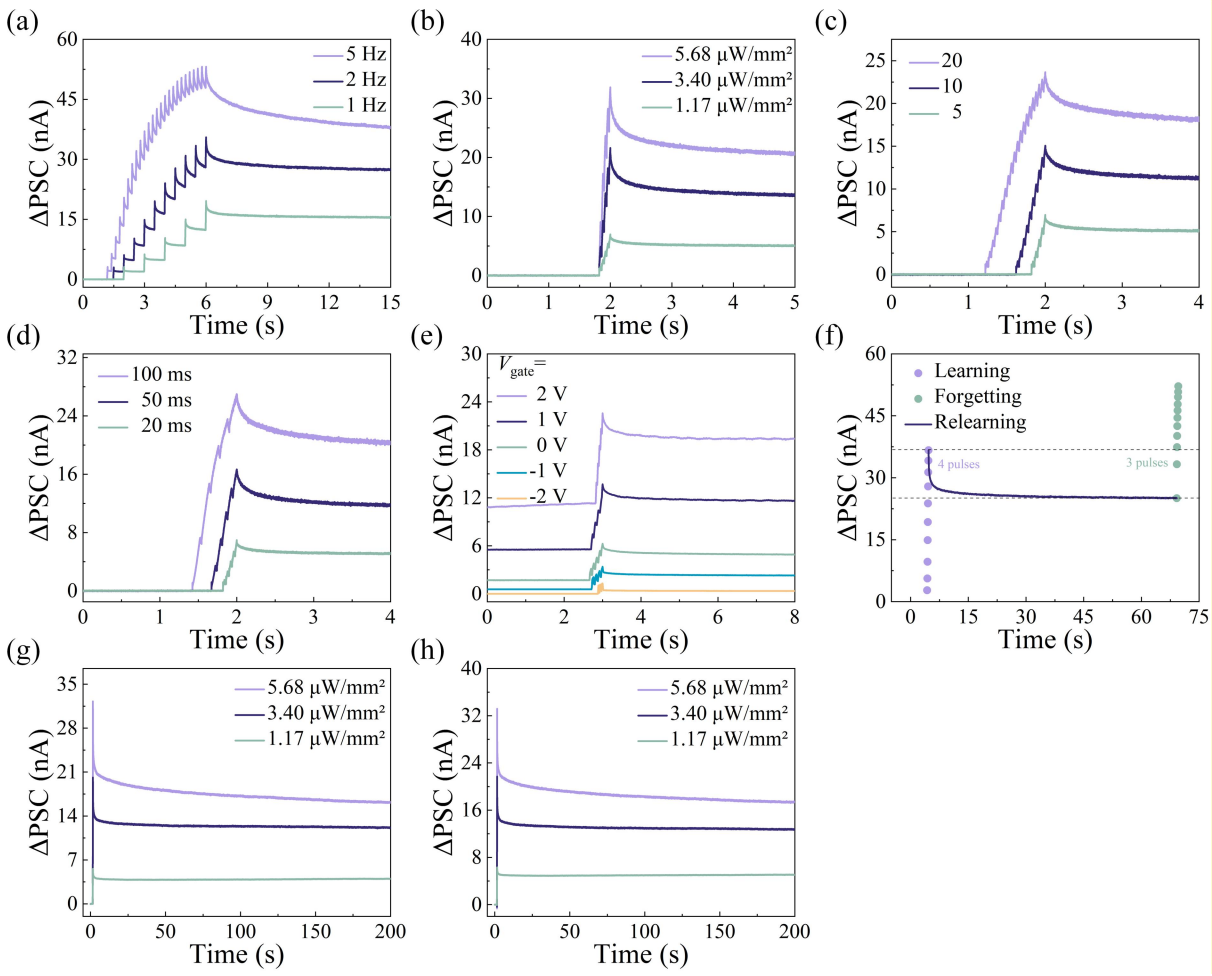



**Figure B8** (a) STP to LTP transition induced by frequency-varied light pulses(375 nm wavelength, 20 ms pulse width, 3.22 μW/mm$^2$ light intensity, float gate state, 10 mV $V_{ds}$, and 5 s duration). (b) STP to LTP transition under different light intensities (375 nm wavelength, 20 ms pulse width, float gate state, 10 mV $V_{ds}$, 20 ms pulse interval, and 5 pulses). (c) STP to LTP transition in the synaptic MOSFET under varying numbers of light pulses (375 nm wavelength, 3.22 μW/mm$^2$ light intensity, 20 ms pulse width, floating gate state, 10 mV $V_{ds}$, and 20 ms pulse interval). (d) STP to LTP transition under different pulse widths (375 nm wavelength, 3.22 μW/mm$^2$ light intensity, 5 light pulses, floating gate state, 10 mV $V_{ds}$, and 20 ms pulse interval). (e) STP to LTP transition at different $V_{gate}$ (375 nm wavelength, 3.22 μW/mm$^2$ light intensity, 20 ms pulse width, 5 light pulses, 10 mV $V_{ds}$, and 20 ms pulse interval). (f) Learning-forgetting-relearning curve (375 nm wavelength, 3.22 μW/mm$^2$ light intensity, 20 ms pulse width, floating gate state, 10 mV $V_{ds}$, and 20 ms pulse interval). (g) Decay curves of STP to LTP transition measured under different light intensities over 200 s in the synaptic MOSFET (375 nm wavelength, 20 ms pulse width, floating gate state, 10 mV $V_{ds}$, 20 ms pulse interval, and 5 pulses). (h) Decay curves of STP to LTP transition measured under source and drain terminals reverse testing with different light intensities over 200 s (375 nm wavelength, 20 ms pulse width, floating gate state, 10 mV $V_{ds}$, 20 ms pulse interval, and 5 pulses).

Figure B8(a-e) depicts the transition from STP to LTP by light pulses of different frequencies, light intensities, numbers of light pulses, pulse widths, and $V_{gate}$ conditions. Figure B8(f) presents the device's learning-forgetting-relearning behavior. The first stimulation process required four light pulses to achieve an EPSC amplitude of 36.65 nA, whereas only three light pulses were needed to attain the same EPSC level during the second stimulation process. Analogous to human cognitive processes, the initial learning phase requires stronger stimulation, whereas relearning after a forgetting period achieves the same synaptic current level with fewer stimuli. The long-term decay curves of STP to LTP transitions under different light intensities, as shown in Figure B8(g) and B8(h), further confirm the device's robust memory retention capability.

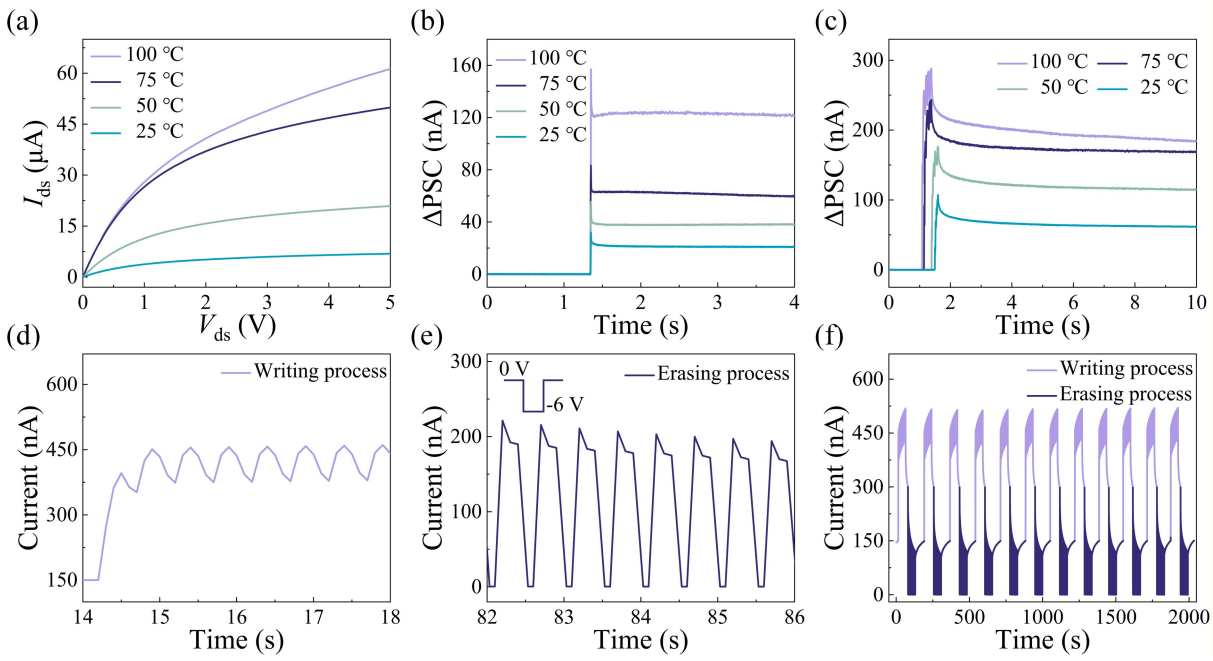



**Figure B9** (a) Output characteristic curves of the synaptic MOSFET under different temperatures with $V_{\mathrm{gate}} = 2$ V. (b) EPSCs of the synaptic MOSFET induced by a light pulse under different temperatures (375 nm wavelength, 20 ms pulse width, 722.36 μW/mm$^2$ light intensity, float gate state, and 1 mV $V_{\mathrm{ds}}$). (c) Transition from STP to LTP of the synaptic MOSFET under different temperatures (375 nm wavelength, 20 ms pulse width, 722.36 μW/mm$^2$ light intensity, float gate state, 10 mV $V_{\mathrm{ds}}$, 20 ms pulse interval, and 5 light pulses). (d) Light writing process of the synaptic MOSFET (375 nm wavelength, 250 ms pulse width, 250 ms pulse interval, 79.61 μW/mm$^2$ light intensity, float gate state, and 10 mV $V_{\mathrm{ds}}$). (e) Gate voltage induced electrical erasing process of the synaptic MOSFET (0 V high level, -6 V low level, 250 ms pulse width, 250 ms pulse interval and 10 mV $V_{\mathrm{ds}}$). (f) Repeated cycles of 100 light pulses writing followed by 100 electrical pulses erasing over a total duration of 2000 s.

Figure B9(a-c) show the device performance of the synaptic MOSFET under different temperatures. It can be observed that both the output current of the synaptic MOSFET and the current variation induced by the light pulse increase with increasing temperature. These phenomena are mainly attributed to the enhanced thermal excitation of carriers in the material under higher temperatures, which significantly increases the concentration and transport efficiency of photogenerated carriers, thereby strengthening the photoresponse and memory behavior of the device. Figure B9(d) illustrates the optical writing process of the synaptic MOSFET, and Figure B9(e) shows the electrical erasing process of the gate under -6 V gate pulses. It can be seen that with repeated gate pulse modulation, the peak current gradually decreases, indicating that appropriate gate modulation can accelerate the "forgetting" process. Meanwhile, a noticeable spike appears when the electrical pulse switches from the low level back to the high level. This phenomenon is attributed to the impedance mismatch between the synaptic MOSFET and the signal generator. Figure B9(f) presents repeated cycles of 100 light pulses for writing followed by 100 electrical pulses for erasing over a total duration of 2000 s, demonstrating that the device maintains good stability during the repeated operation.

## Appendix C The detailed process of neuromorphic computing based on the synaptic cascade structure

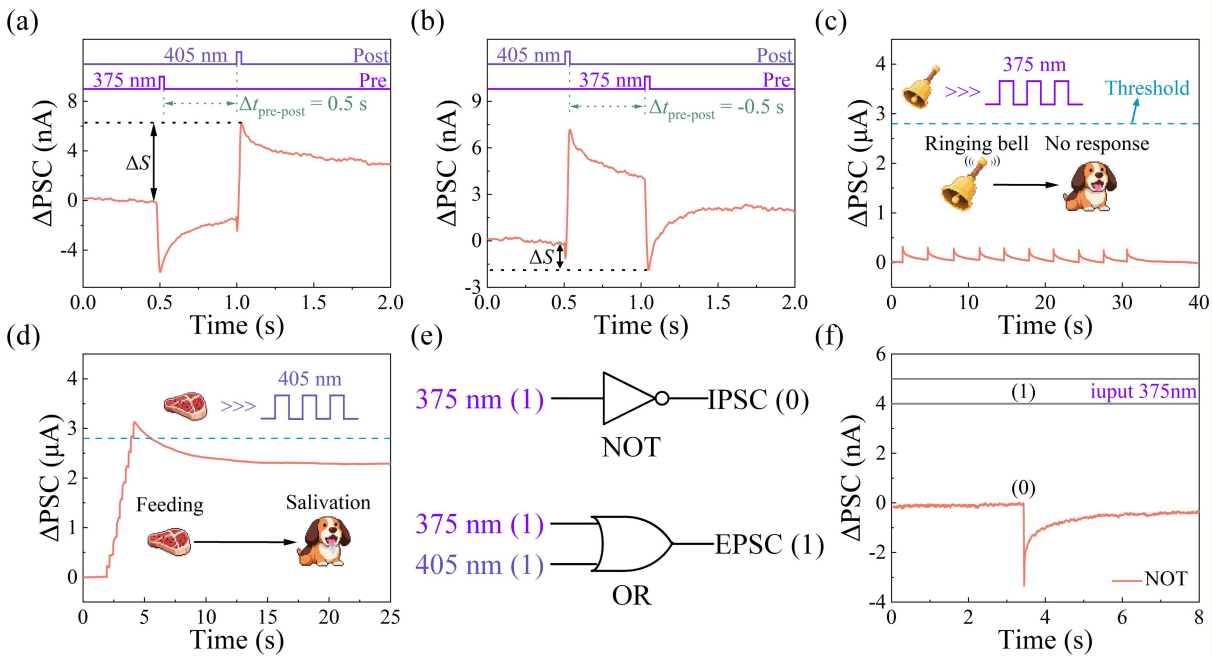



**Figure C1** (a) PSC changes induced by 375 nm light stimuli synaptic diode (20 ms pulse width, 4.73 μW/mm$^2$ light intensity, and -5 V bias) and 405 nm light stimuli synaptic MOSFET (20 ms pulse width, 31.70 μW/mm$^2$ light intensity, and 2 V $V_{ds}$) with $\Delta t_{pre\text{-}post}$ = 0.5 s. (b) PSC changes with $\Delta t_{pre\text{-}post}$ = -0.5 s. (c) Synaptic diodes were used as a bell, and the threshold of PSC induced by ten 375nm light pulses did not exceed 2.8 μA. The dog did not respond to the stimulation of the bell (20 ms pulse width, 16.74 μW/mm$^2$ light intensity, 2 V bias, and 3 s pulse interval). (d) Synaptic MOSFET as food, and the threshold of PSC induced by ten 405nm light pulses exceeding 2.8 μA, induces salivation of the dog (20 ms pulse width, 29.29 μW/mm$^2$ light intensity, 3.5 V $V_{ds}$, and 200 ms pulse interval). (e) Corresponding circuit symbols for NOT and OR logic gates. (f) The logical operation of NOT (the synaptic diode's test condition is 20 ms pulse width, 25.97 μW/mm$^2$ light intensity, and -3 V bias; the synaptic MOSFET's test condition is 20 ms pulse width, 50.73 μW/mm$^2$ light intensity, and 2 V $V_{ds}$).

Figure C1(a) and C1(b) show the change in PSC under different $\Delta t_{pre\text{-}post}$. If the presynaptic spike precedes the postsynaptic spike ($\Delta t_{pre\text{-}post} > 0$), synaptic weight increases and induces LTP, whereas if the postsynaptic spike arrives before the presynaptic spike ($\Delta t_{pre\text{-}post} < 0$), synaptic weight decreases and long-term depression takes place. Based on the spectral responses of the devices, as shown in Figure B1(a) and B7(a), we selected a 375 nm light to stimulate the IS and a 405 nm light to stimulate the OS. Figure C1(a) illustrates the scenario where the IS is stimulated first ($\Delta t_{pre\text{-}post} > 0$). Upon 375 nm light excitation, the IS generates an IPSC, which is converted into PSV via the voltage divider and then applied to the OS, inducing an IPSC. After $\Delta t_{pre\text{-}post}$ of 0.5 s, the OS is activated by the 405 nm light, producing an EPSC. The difference between the second PSC and the baseline current corresponds to the synaptic weight ($\Delta S$). Conversely, when the OS is stimulated first ($\Delta t_{pre\text{-}post} < 0$), as shown in Figure C1(b), the 405 nm light triggers an EPSC in the OS. After $\Delta t_{pre\text{-}post}$ of -0.5 s, the IS is activated by the 375 nm light, generating an IPSC that, after voltage division, induces an IPSC in the OS. The fitted curve of STDP as a function of $\Delta t_{pre\text{-}post}$ is shown in Figure 1(d). This antisymmetry arises from the fact that the first stimulus induces a corresponding IPSC (or EPSC) in the OS, leading to a decrease (or increase) in its conductance. When the second stimulus subsequently excites the OS in the opposite direction, the altered conductance exerts an inhibitory effect on the resultant response. As the absolute value of $\Delta t_{pre\text{-}post}$ increases, the conductance change (in absolute terms) induced by the first stimulus gradually decays, thereby reducing its suppressive influence on the second stimulus.

Figure C1(c) and C1(d) present the details of artificial Pavlov's dog experiment. In conventional experiments, initially, ringing a bell does not elicit salivation. However, after repeatedly pairing the bell with food presentation, the dog eventually associates the two stimuli, leading to salivation upon hearing the bell alone. In Figure C1(c), the 375 nm light serves as the "bell". Based on the SNS structure, when ten consecutive 375 nm light pulses are applied to the IS (ringing bell) induces PSC below the 2.8 μA threshold, analogous to the dog not salivating in response to the bell alone. Conversely, the 405 nm light represents "food", as shown in Figure C1(d). When ten consecutive 405 nm light pulses stimulate the OS (feeding), the PSC exceeds the 2.8 μA threshold, mimicking the dog's salivation. Figure 1(e) shows the phenomenon after modulation by two simultaneous stimuli.

Figure C1(e) illustrates the corresponding circuit symbols for both NOT and OR gates. As previously detailed, the 375 nm light stimulates the IS, while a 405 nm light illuminates the OS. Figure C1(f) illustrates that when the 375 nm optical output signal equals "1", the OS outputs an IPSC, representing a logical "0" output, thereby implementing a NOT gate operation.