SCIENCE CHINA
Information Sciences

• LETTER •

December 2026, Vol. 69, Iss. 12, 229403:1–229403:2
https://doi.org/10.1007/s11432-025-4948-y

High-power and high-efficiency AlN/GaN HEMTs on silicon for low supply voltage operation

Hanghai DU[1,2], Zeyu SONG[1], Zhihong LIU[1,2*], Yachao ZHANG[1], Kui DANG[1], Weichuan XING[2], Jin ZHOU[2], Jing NING[1*], Zan LI[3] & Jincheng ZHANG[1,2*]

[1]*State Key Laboratory of Wide Bandgap Semiconductor Devices and Integrated Technology, School of Microelectronics, Xidian University, Xi'an 710071, China*
[2]*Guangzhou Wide Bandgap Semiconductor Innovation Center, Guangzhou Institute of Technology, Xidian University, Guangzhou, 510555, China*
[3]*State Key Laboratory of Integrated Services Networks, School of communication Engineering, Xidian University, Xi'an 710071, China*

Received 3 December 2025/Revised 25 February 2026/Accepted 28 April 2026/Published online 28 October 2026

Citation Du H H, Song Z Y, Liu Z H, et al. High-power and high-efficiency AlN/GaN HEMTs on silicon for low supply voltage operation. Sci China Inf Sci, 2026, 69(12): 229403, https://doi.org/10.1007/s11432-025-4948-y

Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) demonstrate superior performance in high-frequency and high-power applications. Recently, GaN HEMT research has strategically shifted toward low-voltage applications [1], specifically mobile terminals operating at 5 V and femtocell applications operating at 8 V, to balance efficiency, linearity, and power density. This shift aims to displace incumbent silicon (Si)- and gallium arsenide (GaAs)-based transistors currently used in radio frequency (RF) front-end modules. This transition is motivated by GaN's inherent material advantages; specifically, GaN's high breakdown electric field and high electron saturation velocity enable transistors to sustain significantly higher power density (P_{out}) while maintaining superior power-added efficiency (PAE) compared with Si and GaAs technologies. These attributes are critical for battery-powered devices and facilitate both enhanced performance and increased functional integration in mobile devices. Conventional AlGaN/GaN transistors employing thick barrier layers are limited by high ohmic contact resistance (R_c), high knee voltage, and high two-dimensional electron gas (2DEG) channel sheet resistance (R_{sh}). These factors restrict the potential of such transistors to achieve high power and efficiency in low-voltage applications. Consequently, heterostructures designed for low ohmic contact and low sheet resistance are essential for realizing high P_{out} and high PAE.

In this work, thin-barrier and strongly polarized AlN/GaN HEMTs grown on a Si substrate are demonstrated, achieving high P_{out} and high PAE under low-voltage operation.

Experiment methods. The AlN/GaN MISHEMT epitaxial heterostructure was grown on a 6-inch high-resistivity Si substrate via metal-organic chemical vapor deposition (MOCVD). As illustrated in the cross-sectional schematic in Figure 1(a), the epitaxial stack consists of a 1.7-μm unintentionally doped GaN buffer, a 5-nm AlN barrier, and a in situ SiN_x cap layer. Room-temperature Hall-effect measurements revealed a 2DEG density of 2.1×10^{13} cm^{-2}, an electron mobility of 1205 cm^{-2}·V^{-1}·s^{-1}, and a corresponding sheet resistance of 247 Ω·□$^{-1}$. Device fabrication commenced with ion implantation planar isolation. A Ti/Al/Ni/Au metal stack was deposited on a 4-nm-thick in situ SiN_x passivation layer, followed by rapid thermal annealing at 850°C for 30 s to form ohmic contacts [2]. The R_c was approximately 0.25 Ω·mm via the transmission line method. Subsequently, 150-nm T-gates (L_g) were defined, followed by gate metal evaporation and lift-off. A 50-nm-thick SiN_x layer was then deposited via plasma-enhanced chemical vapor deposition as an ex situ passivation layer. The transistor features a total gate width (W_g) of 2 × 25 μm and a source-to-drain spacing (L_{sd}) of 1.5 μm, with the gate centered between the source and drain. The transistor structure and its scanning electron microscope (SEM) image are presented in Figures 1(a) and (b), respectively.

Results and discussion. Figures 1(c) and (d) present the transfer characteristics of the transistor. The thin barrier layer enabled the 150-nm gate length device to achieve a high extrinsic transconductance (g_m) exceeding 500 mS·mm^{-1}. Further, the in situ SiN_x layer effectively suppressed gate leakage current, resulting in an I_d current on/off ratio exceeding 10^8. Negative differential resistance in I_g observed at $V_{gs} = -4$ V and $V_{ds} = 6$ V is attributed to electron trapping near the channel, which reduces the local potential and gate-channel voltage, leading to I_g reduction. In addition to dc output characteristics, current collapse was characterized under various bias voltages. Pulsed I_d-V_d curves are presented in Figure 1(f). The reduction of self-heating effects under cold bias enhances the I_d. Moreover, the pulsed I_d-V_d characteristics exhibit minimal degradation compared with dc characteristics, which is attributed to the optimized passivation process.

Figures 1(g) and (h) present the RF small-signal characteristics after de-embedding metal pads, alongside the extracted current gain cutoff frequency (f_{T}) and maximum oscillation frequency (f_{max}) as functions of V_{gs}. At $V_{gs} = -3$ V and $V_{ds} = 6$ V, the 150-nm gate length transistor achieved f_{T} and f_{max} values of 75

* Corresponding author (email: liuzhihong@ieee.org, ningj@xidian.edu.cn, jchzhang@xidian.edu.cn)

© Science China Press 2026

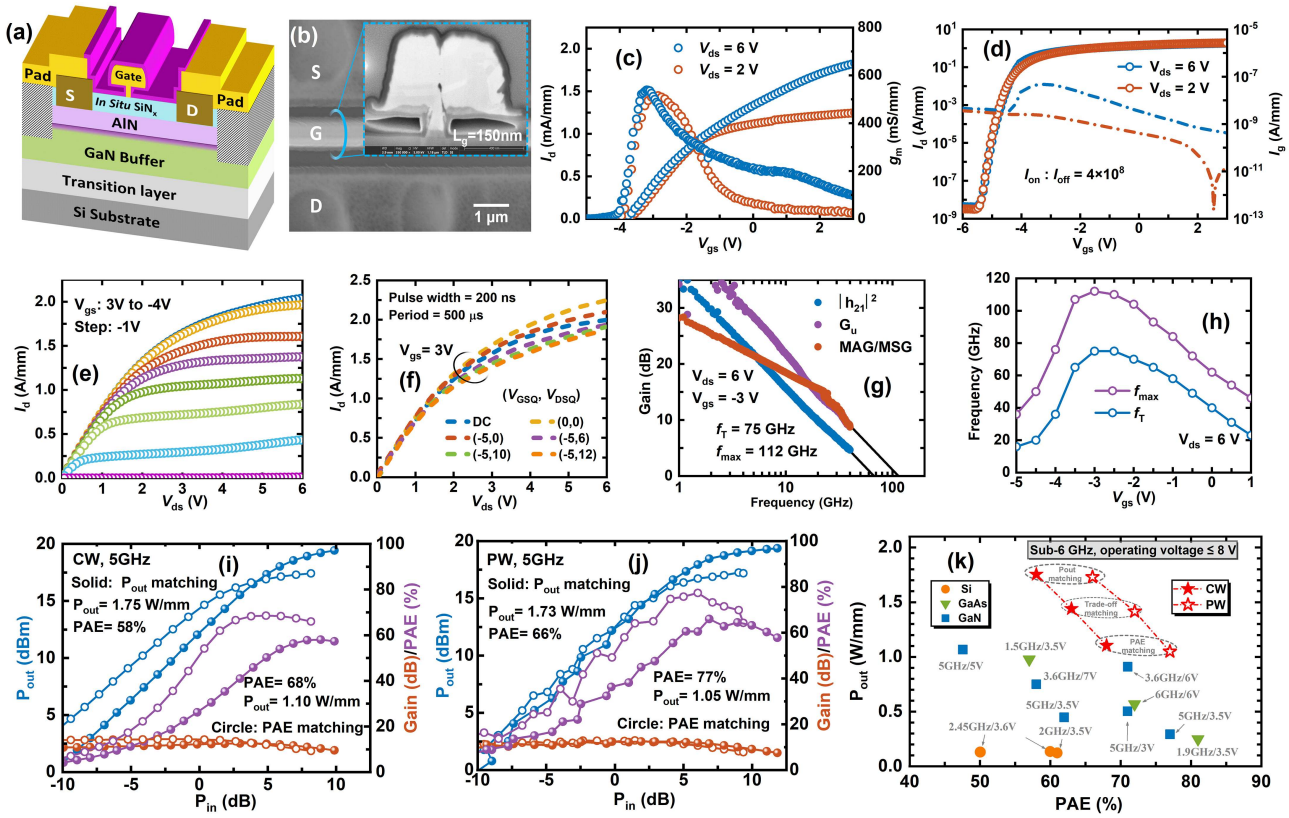

Figure 1 (Color online) (a) Cross-sectional schematic of the fabricated transistor; (b) top-view SEM image of the transistor; (c) linear and (d) log-scale transfer characteristics under varying bias voltages; (e) output characteristics; (f) pulsed I_d-V_d curves; (g) RF small-signal characteristics; (h) $f_{\max}$ and f_{T} versus V_{gs}; (i) CW and (j) PW load-pull power sweep characteristics; (k) benchmarking of P_{out} and PAE.

and 112 GHz, respectively. These results yield high values for $f_{\mathrm{T}} \times L_g$ (11.3 GHz·μm vs. 9.5 GHz·μm in [1]) and $f_{\max} \times L_g$ (16.8 GHz·μm vs. 15.0 GHz·μm in [1]). Maintenance a high $f_{\max}$ value over a wide V_{gs} range ensures that the power gain does not compress prematurely during large-signal RF input, a highly desirable characteristic for high-performance transistors.

Large-signal characteristics were characterized using an on-wafer load-pull system under 5 GHz continuous-wave (CW) and pulsed-wave (PW) signal operations (100 μs pulse width and 1 ms period). The transistor impedance was tuned for maximum P_{out} matching and maximum efficiency matching, as shown in Figures 1(i) and (j), respectively. Under CW operation, the transistor achieved a P_{out} of 1.75 W·mm^{-1} with a PAE of 58%, and a PAE of 68% with a P_{out} of 1.10 W·mm^{-1}. Under PW operation, it exhibited a P_{out} of 1.73 W·mm^{-1} with a PAE of 66%, and a PAE of 77% with a P_{out} of 1.05 W·mm^{-1}. Figure 1(k) benchmarks this performance against state-of-the-art semiconductor transistors for $V_{ds} \leqslant 8$ V. The results surpass the majority of reported Si, GaAs, and other GaN RF transistors [3–5].

Conclusion. We demonstrated high-power and high-efficiency AlN/GaN HEMTs for low-voltage applications using strongly polarized heterostructures and low-resistance ohmic contact technologies. The devices exhibited high transconductance and current density, yielding an f_{T} of 75 GHz and an $f_{\max}$ of 112 GHz. Notably, we achieved excellent large-signal RF performance, including a maximum P_{out} of 1.75 W·mm^{-1} and a maximum PAE of 77%. These results validate the potential of GaN-on-Si RF technology to enhance system performance and integration in low-voltage applications.

Acknowledgements This work was supported in part by National Natural Science Foundation of China (Grant Nos. 62504180, 62574156), National Science Fund for Distinguished Young Scholars (Grant Nos. 62525402, 61925404), and Postdoctoral Fellowship Program of CPSF (Grant Nos. GZB20240587, 2025M770518).

References

1 Then H W, Radosavljevic M, Jun K, et al. Gallium nitride and silicon transistors on 300 mm silicon wafers enabled by 3-D monolithic heterogeneous integration. IEEE Trans Electron Devices, 2020, 67: 5306–5314
2 Du H, Liu Z, Hao L, et al. Low ohmic contact resistivity realized by in situ SiN_x insertion for high Al-composition-AlGaN/GaN heterostructure. Appl Phys Lett, 2022, 121: 172102
3 Zhou Y, Mi M, Gong C, et al. High-efficiency millimeter-wave enhancement-mode ultrathin-barrier AlGaN/GaN fin-HEMT for low-voltage terminal applications. IEEE Trans Electron Devices, 2024, 71: 1383–1386
4 Yu Q, Shi C, Yang L, et al. High current and linearity AlGaN/GaN/-graded-AlGaN:Si-doped/GaN heterostructure for low voltage power amplifier application. IEEE Electron Device Lett, 2023, 44: 582–585
5 Li M, Zhu J, Zhang S, et al. High-performance SiN/AlGaN/GaN MIS-HEMTs on Si substrate with LPCVD-SiN passivation and n^+-InGaN ohmic contacts. Sci China Inf Sci, 2025, 68: 202402