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Electro-optically co-modulated β-Ga_2O_3 floating-gate transistors for neuromorphic computing

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Machine learning based on neural networks has achieved remarkable success in pattern recognition, autonomous systems, and intelligent sensing [1]. Most neural network workloads are currently implemented on digital hardware platforms following the von Neumann computing paradigm, where memory and logic units are physically separated. Such architectures suffer from frequent data transfer between memory and processor, resulting in substantial energy and latency overhead, especially for edge computing applications. This limitation has stimulated strong interest in neuromorphic computing hardware, which performs storage and computation locally at synaptic nodes. Non-volatile memory devices have been widely explored as artificial synapses, among which floating-gate transistors are particularly attractive due to their charge-based analog storage, large dynamic range, multi-level programmability, and CMOS compatibility [2]. Introducing optical stimuli into floating-gate synapses provides an additional programming dimension with potentially lower power consumption and improved interference immunity. Gallium oxide (Ga_2O_3), with an ultra-wide bandgap of ∼4.9 eV, exhibits intrinsic solar-blind ultraviolet absorption, enabling low-noise optical stimulation free from visible-light background interference [3]. However, defect-associated resistive switching in Ga_2O_3 memories often suffers from limited quantitative control over defect states, together with persistent photoconductivity, hindering fast and accurate conductance programming. Recently, Zeng et al. demonstrated a Ga_2O_3-based floating-gate memory using Ga_2O_3 as the dielectric layer, revealing the feasibility of electro-optical modulation [4]. In this work, we adopt a separated optical absorption and floating-gate control architecture to realize Ga_2O_3-channel floating-gate transistors (FGT). By engineering capacitive coupling and electrical-optical programming mechanisms, stable 3-bit nonvolatile weight states and microsecond-scale write/erase speeds are achieved, enabling efficient neural network computation and handwritten digit recognition.

Experiment. Figure 1(a) schematically illustrates the structure of the Ga_2O_3 FGT. The channel consists of a 200 nm Ga_2O_3 film epitaxially grown on a sapphire substrate by metal-organic chemical vapor deposition (MOCVD). Device isolation was achieved by inductively coupled plasma etching, followed by ion implantation for source and drain doping. A Ti/Au bilayer was then deposited and subjected to rapid thermal annealing at 475°C for 1 min to form ohmic contacts. The floating-gate stack, from bottom to top, comprises a 10 nm HfO_2 tunneling layer (TL), a 20 nm Ni floating-gate (FG) layer, a 30 nm Al_2O_3 dielectric layer (DL), and a control gate (CG) electrode. By varying the lateral length of the control gate (L_{CG}), the voltage across the tunneling layer can be effectively modulated, enabling tunable threshold voltage characteristics. The lower panel of Figure 1(a) shows an optical microscope image of a representative device with a 2 μm CG. The optoelectronic measurements were performed on a probe station equipped with a Keysight B1505A, a commercial 254 nm light emitting diode (LED), and an external signal generator.

Results and discussion. To elucidate the operating mechanism, the FGT band structure was extracted using commercial simulation software SILVACO. As shown in Figure 1(b), a negative control-gate bias ($-V_{CG}$) drives electron tunneling from the floating gate through the HfO_2 layer into the Ga_2O_3 channel, enabling conductance writing. The HfO_2 layer forms an energy barrier that prevents electrons from spontaneously returning to the floating gate, ensuring nonvolatile storage. Conversely, a positive bias ($+V_{CG}$) extracts electrons from the channel back to the floating gate, achieving conductance erasure. Furthermore, the FGT supports precise conductance programming through three complementary strategies, the first of which is capacitive coupling modulation. As illustrated in Figure 1(b), the CG-Al_2O_3-FG stack and the FG-HfO_2-Ga_2O_3 stack can be represented by equivalent capacitances C_{CG} and C_{FG} in series. The voltage on the floating gate (V_{FG}) is then given by $V_{FG} = V_{CG} \times C_{CG}/(C_{CG}+C_{FG})$. In this architecture, reducing the L_{CG} is expected to increase the capacitive coupling ratio C_{FG}/C_{CG}, thereby lowering the V_{FG} at a fixed V_{CG}. As a result, tunable conductance states and memory windows can be achieved by geometrically scaling

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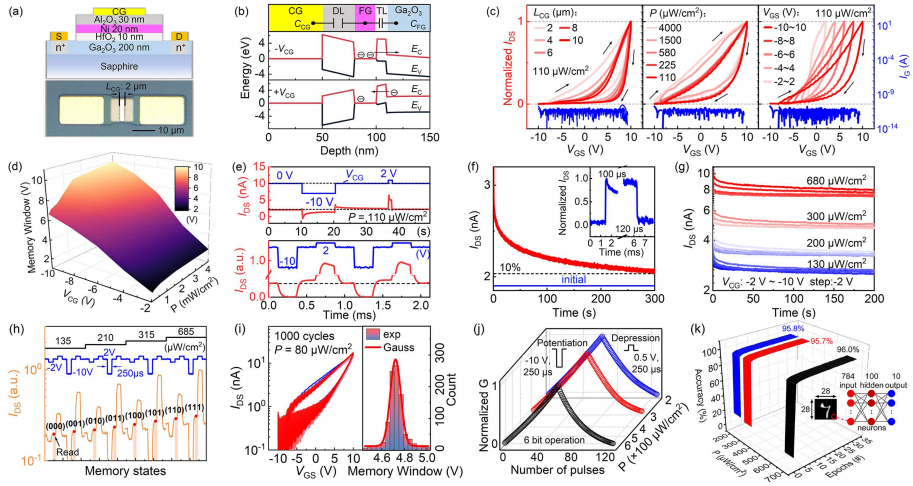


Figure 1 (Color online) (a) Schematic and optical microscope images of the Ga_2O_3 FGT; (b) band structure of the Ga_2O_3 FGT; (c) transfer curves under different L_{CG}, optical intensities, and V_{CG}; (d) memory window as a function of optical intensity and V_{CG}; (e) write and erase operations of the FGT; (f) retention characteristics of the FGT; (g) 20 states with each sampled for 200 s; (h) 3-bit multilevel storage of the FGT; (i) transfer curves from 1000 consecutive cycles; (j) potentiation and depression behaviors of the FGT under illumination with different intensities; (k) recognition rate as a function of the number of training epochs.

L_{CG}. This capacitive-coupling-controlled behavior is experimentally confirmed in the left panel of Figure 1(c), which shows the hysteresis characteristics of devices with L_{CG} = 2, 4, 6, 8, 10 μm. The corresponding memory windows are extracted to be 6.5, 4.4, 4, 3.8, and 3.4 V, respectively. Owing to the largest memory window, L_{CG} = 2 μm is adopted for all subsequent measurements unless otherwise specified; the V_{DS} is set to 2 V by default. Beyond geometric capacitive tuning, the FGT enables additional conductance modulation through optical and electrical stimuli enabled by the spatially separated channel and floating-gate design. Using Ga_2O_3 as the channel material, 254 nm Ultra-Violet (UV) illumination precisely modulates photogenerated carrier density in the channel, producing systematic changes in conductance and threshold voltage, and thus tuning the memory window. In parallel, electrical modulation is realized by adjusting the writing voltage to control electron tunneling through the HfO_2 layer, thereby shifting the channel threshold voltage. The middle and right panels of Figure 1(c) present the evolution of the memory window under optical and electrical modulation, respectively, showing pronounced and controllable changes in both cases. Notably, the gate leakage current remains at the 0.38 pA level throughout all measurements, confirming reliable floating-gate operation. Figure 1(d) summarizes the memory window as a function of optical intensity and writing voltage. The results indicate that increasing the optical intensity and writing voltage effectively enlarges the memory window, reaching a maximum value of 10 V. Figure 1(e) illustrates the write and erase operations of the device, with the read voltage fixed at 0 V. After a −10 V programming pulse with a duration of 10 s (250 μs), the channel conductance increases markedly, whereas a +2 V pulse applied for 1 s (250 μs) restores the conductance to its initial state. The retention characteristics are evaluated in Figure 1(f), showing that the channel current decays to 10% of its maximum value after 300 s. In addition, time-resolved measurements using a high-bandwidth oscilloscope reveal that both write and erase operations can be completed within 120 μs. As shown in Figure 1(g), the device supports 20 stable conductance states spanning 2.5–8.5 nA. Based on μs-scale pulse programming, eight well-resolved conductance levels are further obtained to enable 3-bit multilevel storage (Figure 1(h)). Device endurance was tested over 1000 consecutive write/erase cycles. As shown in Figure 1(i), the overlaid curves exhibit minimal conductance drift, with a memory window of 4.72 V (FWHM: 0.09 V), indicating robust stability and reproducible multilevel operation. In neuromorphic vision processing, hardware synaptic devices must support accurate weight modulation for image recognition tasks. The linearity and symmetry of synaptic weight updates therefore play a critical role in determining network accuracy. Accordingly, the conductance evolution of the proposed Ga_2O_3 FGT was characterized under 64 potentiation and 64 depression pulses at different optical intensities (210, 315, and 685 μW/cm^2), as shown in Figure 1(j). Based on the experimentally extracted conductance characteristics, an artificial neural network comprising 784 input neurons, 100 hidden neurons, and 10 output neurons was constructed for image recognition, as shown in Figure 1(k). After 30 training epochs, the network achieved recognition accuracies of 95.8%, 95.7%, and 96.0% under the three optical intensities, respectively, demonstrating the feasibility of the proposed device as a neuromorphic vision processing unit.

Conclusion. The Ga_2O_3 FGT enables stable 3-bit multilevel storage with fast 120 μs programming and supports neuromorphic vision processing, achieving 92.26% recognition accuracy, demonstrating strong potential for optoelectronic neuromorphic computing.

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