SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

December 2026, Vol. 69, Iss. 12, 222401:1–222401:10
https://doi.org/10.1007/s11432-025-4989-8

Mutually reinforcing effect between ferroelectric polarization and charge trapping in FeFET-based NAND flash memory

Xin GONG[1], Bao ZHANG[1*], Jingwen HOU[1], Tianhao ZHENG[1], Lei LIU[2], Kechao TANG[3], Zhiliang XIA[2], Qi WANG[1*], Yimao CAI[3] & Zongliang HUO[2*]

[1]*Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China*
[2]*Yangtze Memory Technologies Co., Ltd. (YMTC), Wuhan 430078, China*
[3]*School of Integrated Circuits, Beijing Advanced Innovation Center for Integrated Circuits, Peking University, Beijing 100871, China*

Received 31 October 2025/Revised 8 January 2026/Accepted 3 June 2026/Published online 28 October 2026

Abstract To assist with the future application of ferroelectric materials in 3D NAND flash memory, we clarify the coupling mechanism between ferroelectric polarization and charge trapping, which intensifies the memory window (MW), in a gate-stack ferroelectric field-effect transistor (FeFET). Based on Gauss's law, the mutual reinforcement effect is revealed: the charge trapping efficiency is boosted as a result of ultrafast polarization switching, and the trapped charge, in turn, improves remanent polarization. The MW is consistently enlarged through the coupling mechanism for an FeFET with dominant gate-side injection, while it depends on the competition between charge trapping enhancement and the MW counteracting effect for an FeFET with dominant channel-side injection. Through an in-depth investigation of the quantitative relationships between the MW and FeFET parameters, we explain the intrinsic mechanism of the MW enlargement/narrowing phenomenon using crucial theoretical formulas. With engineering optimization, such a coupling mechanism can intensify the MW in an FeFET by more than 50%. These findings will benefit further studies on hafnium-based nonvolatile memory.

Keywords ferroelectric, charge trapping, coupling, field-effect transistors, memory window

Citation Gong X, Zhang B, Hou J W, et al. Mutually reinforcing effect between ferroelectric polarization and charge trapping in FeFET-based NAND flash memory. Sci China Inf Sci, 2026, 69(12): 222401, https://doi.org/10.1007/s11432-025-4989-8

1 Introduction

With the rapid development of information technologies such as artificial intelligence in the era of big data, the demand for high-density information storage and computing has become increasingly critical [1, 2]. To address these challenges, the application of a novel nonvolatile memory using a ferroelectric material, which has an ultrafast polarization switching property, is considered one of the most promising solutions [3, 4]. Since the discovery of robust ferroelectricity (FE) in doped hafnium oxide (HfO_2) [5], this material has attracted much attention because of its excellent process compatibility with complementary metal-oxide-semiconductor technology and its superior scalability at ultrathin dimensions [6]. A wide spectrum of applications has been proposed [7–16], most notably in nonvolatile memory, where HfO_2 is the cornerstone of the ferroelectric random-access memory (FeRAM) [17–22], the ferroelectric field-effect transistor (FeFET) [23–30], and the ferroelectric tunnel junction (FTJ) [31–35]. Beyond memory, the polarization switching and negative capacitance effect are being harnessed for low-power logic transistors and neuromorphic computing systems that emulate synaptic plasticity [36–40].

However, despite the considerable advances made, a large number of challenges still need to be fully addressed, and various FeFET structures are being investigated. The Si-channel FeFET has a metal-ferroelectric-insulator-semiconductor structure, and its memory window (MW) is usually small due to channel-side injection (CSI), which inevitably occurs in the oxide layer between the channel and HfO_2 [41–46]. However, this can be improved through interface optimization [47, 48] or through the use of an oxide semiconductor channel [49, 50]. Improved device performance with dual ferroelectric and charge-trapping (CT) layers has been reported for ferroelectricity-boosted gate stacks [51–54]. By introducing gate-side injection (GSI) in MIFIS-FeFETs with a metal-insulator-ferroelectric-insulator-semiconductor structure, the dual mechanism of FE and CT is utilized to greatly improve the MW [55–67].

* Corresponding author (email: zhangbao@ime.ac.cn, wangqi1@ime.ac.cn, zongliang_huo@ymtc.com)

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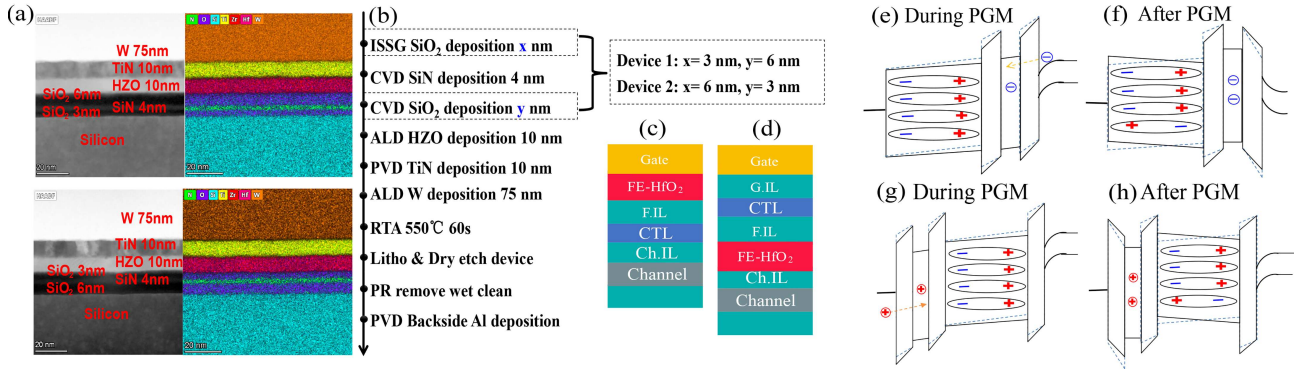

Figure 1 (Color online) (a) TEM and EDS images of the two MFINIS-FeFETs (M: W and TiN, F: HZO, I: SiO_2, N: SiN) and (b) the key fabrication processes. Cell structures of (c) MFINIS-FeFET and (d) MINIFIS-FeFET used in theoretical analysis and simulations. G.IL, F.IL, and Ch.IL represent different interlayers. In this work, the ferroelectric layer is HZO, and the charge trapping layer (CTL) is SiN. Band structure analysis during and after PGM: (e) and (f) for the MFINIS-FeFET, and (g) and (h) for the MINIFIS-FeFET. During PGM, (solid line) HfO_2 in the $Pca2_1$-phase had a smaller voltage than (dashed line) in the monoclinic phase, as this provided the oxide layer with a larger electric field for tunneling. After PGM, the depolarization field (solid line) contributes to charge retention in the devices, and the trapped charge also helps inhibit polarization degradation.

However, although it has been reported that the MW contributions from FE and CT are one-third and two-thirds, respectively [59], these results contradict the theoretical prediction that the maximum MW from FE cannot exceed $2E_c \cdot d$. Although all these results indicate the existence of a coupling effect between FE and CT [68–72], systematic theoretical research on this phenomenon is lacking.

In this study, we focused on the physical mechanism of the coupling effect in various FeFET structures, which are abstracted into two major categories: MFINIS-FeFET with CSI and MINIFIS-FeFET with GSI. Based on Gauss's law, it is found that the MW contribution from FE and GSI is mutually reinforcing, contrary to that from CSI, leading to an expansion of the MW in some structures and a narrowing in others. Through experiments and TCAD simulations, a detailed analysis is performed on device performance variations with program/erase voltage, tunneling oxide layer thickness, trap concentration, and polarization strength. By comparing the results of the same FeFET structure with/without FE or CT, we verify the coupling mechanism between FE and CT. Ferroelectric polarization can boost the CT efficiency during the program (PGM) and erase (ERS) processes, and the depolarization field improves the charge retention, while the trapped charge, in turn, prevents polarization degradation and enhances remanent polarization. Moreover, the coupling term can intensify the total MW from FE and CT by more than 50% and supply an MW contribution to the FeFET of more than 30%; in contrast, the contribution from FE is smaller than $2E_c \cdot d$. In summary, we provide a comprehensive understanding of the coupling mechanism between FE and CT, as well as its influence on the MW, offering valuable guidelines for the future application of FeFET-based NAND.

2 Methodology

In the experiment based on the MFINIS-FeFET structure, a 3/4/6 nm or 6/4/3 nm $SiO_2/Si_3N_4(SiN)/SiO_2$ (ONO) stack is deposited via in-situ steam generation and chemical vapor deposition on a p-silicon substrate. Using $Hf[N(C_2H_5)CH_3]_4$ (TEMAH), $Zr[N(C_2H_5)CH_3]_4$ (TEMAZ), and O_3 as precursors for Hf, Zr and O in atomic layer deposition (ALD), a 10 nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) film is deposited after the ONO stack. An Hf:Zr ratio of 1:1 is chosen to achieve optimal ferroelectric performance [73, 74]. After depositing 10 nm TiN and 75 nm tungsten (W), rapid thermal annealing at 550°C for 60 s is performed to promote ferroelectric phase formation in HZO. The final devices are characterized using transmission electron microscopy (TEM) and energy-dispersive spectroscopy (EDS), and the corresponding images are shown in Figure 1. Meanwhile, TCAD simulations are performed, and a detailed analysis is conducted. Simulation details, such as the PGM/ERS time series and the calculations of electric field, ferroelectric polarization [75], and trapped charge, are shown in Appendix B.

Theoretically, the electric field of each layer in a FeFET is perpendicular to the gate, and the threshold voltage is

$$V = \phi_{ms} + \psi_s + \sum_i E_i d_i, \tag{1}$$

where ϕ_{ms} is the metal-semiconductor work function difference, ψ_s is the surface potential, and i contains all layers

between the channel and gate. With Gauss's law,

$$(\varepsilon_0\varepsilon_i E_i + P_i) - (\varepsilon_0\varepsilon_j E_j + P_j) = (Q_i - Q_j), \tag{2}$$

we can derive the MW formula. For MFINIS-FeFET,

$$\mathrm{MW} = V_{\mathrm{pgm}} - V_{\mathrm{ers}} = (E_{\mathrm{pgm}} - E_{\mathrm{ers}})d_{FE} - (Q_{\mathrm{pgm}} - Q_{\mathrm{ers}})\left(\alpha\frac{d_{CTL}}{\varepsilon_0\varepsilon_{CTL}} + \frac{d_{F.IL}}{\varepsilon_0\varepsilon_{F.IL}}\right); \tag{3}$$

and for MINIFIS-FeFET,

$$\mathrm{MW} = V_{\mathrm{ers}} - V_{\mathrm{pgm}} = -(E_{\mathrm{pgm}} - E_{\mathrm{ers}})d_{FE} + (Q_{\mathrm{pgm}} - Q_{\mathrm{ers}})\left(\alpha\frac{d_{CTL}}{\varepsilon_0\varepsilon_{CTL}} + \frac{d_{G.IL}}{\varepsilon_0\varepsilon_{G.IL}}\right), \tag{4}$$

where E_{pgm} (E_{ers}) and Q_{pgm} (Q_{ers}) are the electric field of the ferroelectric layer and trapped charge in CTL after the PGM (ERS) process, respectively; α is a correction factor which origins from the nonuniform charge distribution in CTL, and $\alpha = 1/2$ for the uniform charge distribution. Further calculation details are shown in Appendix A.

During the PGM/ERS process, polarization switching occurs in nanoseconds, boosting hole/electron injection through the polarization-charge coupling mechanism. Furthermore, orthorhombic phase ($Pca2_1$) HfO_2 has a larger permittivity than HfO_2 in monoclinic (m) phase, resulting in a smaller electric field in HZO but a larger tunneling electric field in the oxide, as shown in Figure 1. After PGM, the ferroelectric layer has positive remanent polarization with a negative electric field, interacting with trapped charges on the channel (gate) side. Applying the same analysis to ERS and substituting the signs of $E_{\mathrm{pgm}}, E_{\mathrm{ers}}, Q_{\mathrm{pgm}}, Q_{\mathrm{ers}}$ into (3) and (4), we find that $E_{\mathrm{pgm}} - E_{\mathrm{ers}}$ is negative, and $Q_{\mathrm{pgm}} - Q_{\mathrm{ers}}$ for CSI (GSI) is negative (positive). Therefore, the MW induced by FE and GSI counteracts CSI. Naturally, the adjacent SiO_2 and SiN have a limited surface charge density compared to the polarization of HZO. To meet the charge equilibrium in a steady state, ferroelectric polarization will degrade. The trapped charge can compensate for the external surface charge to prevent polarization degradation and influence the electric field. By decoupling FE and CT in FeFET, the coupled ferroelectric electric field and trapped charge, as well as the MW, can be written as

$$\Delta E = E_{\mathrm{pgm}} - E_{\mathrm{ers}} = E_0 + f(\mathrm{CT}, \mathrm{FE}), \tag{5a}$$

$$\Delta Q = Q_{\mathrm{pgm}} - Q_{\mathrm{ers}} = Q_0 + g(\mathrm{CT}, \mathrm{FE}), \tag{5b}$$

$$\mathrm{MW(CT + FE)} = \mathrm{MW(CT)} + \mathrm{MW(FE)} + \mathrm{MW(coupling)}, \tag{6}$$

where MW(CT + FE) is the MW for the coupled FeFET with both CT and FE; E_0 is the electric field for the FeFET with FE but not CT, leading to the memory contribution MW(FE); Q_0 is the trapped charge for the FeFET with CT but not FE, leading to the memory contribution MW(CT); $f(\mathrm{CT}, \mathrm{FE})$ and $g(\mathrm{CT}, \mathrm{FE})$ are the extra electric field and trapped charge from the coupling of CT and FE, resulting in the memory contribution MW(coupling). For MFINIS-FeFET,

$$\mathrm{MW(coupling)} = f(\mathrm{CT}, \mathrm{FE}) \cdot d_{FE} - g(\mathrm{CT}, \mathrm{FE}) \cdot \left(\alpha\frac{d_{CTL}}{\varepsilon_0\varepsilon_{CTL}} + \frac{d_{F.IL}}{\varepsilon_0\varepsilon_{F.IL}}\right); \tag{7}$$

and for MINIFIS-FeFET,

$$\mathrm{MW(coupling)} = -f(\mathrm{CT}, \mathrm{FE}) \cdot d_{FE} + g(\mathrm{CT}, \mathrm{FE}) \cdot \left(\alpha\frac{d_{CTL}}{\varepsilon_0\varepsilon_{CTL}} + \frac{d_{G.IL}}{\varepsilon_0\varepsilon_{G.IL}}\right). \tag{8}$$

Generally, ferroelectric HZO is formed by controlling the fabrication conditions to make a coupled FeFET for MW(CT + FE) measurements in experiments. By replacing HZO with HfO_2 as the dielectric layer, FeFET with only CT and MW(CT) can be obtained, and by introducing a thick tunneling layer to suppress CT, FeFET with only FE and MW(FE) can be estimated. In simulations, this can be simply achieved by adding or removing the ferroelectric model in the ferroelectric layer and setting a zero or nonzero trap concentration in the CT layer.

3 Results and discussion

3.1 Memory window variation in MFINIS-FeFET

First, the interaction between FE and CSI is investigated, with CSI amplified (suppressed) by changing the tunneling oxide layer thickness. As in the former analysis, there is competition between CT enhancement and the MW

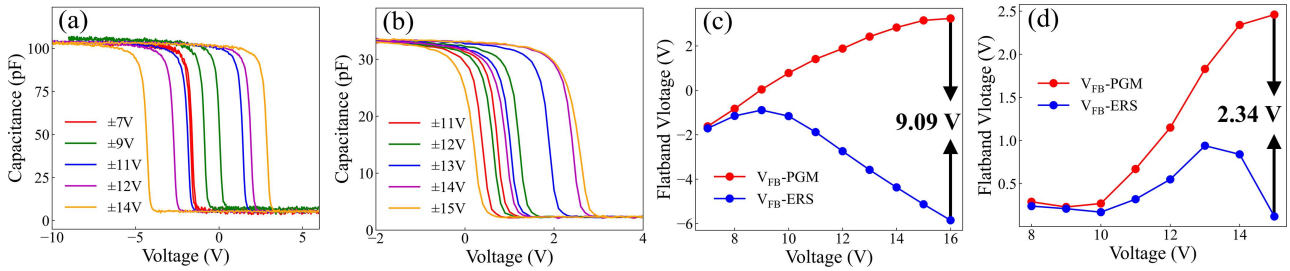

Figure 2 (Color online) *C-V* testing and flatband voltages of (a) and (c) Device 1 with thin tunneling oxide and (b) and (d) Device 2 with a thick tunneling oxide under forward and negative voltage sweeping.

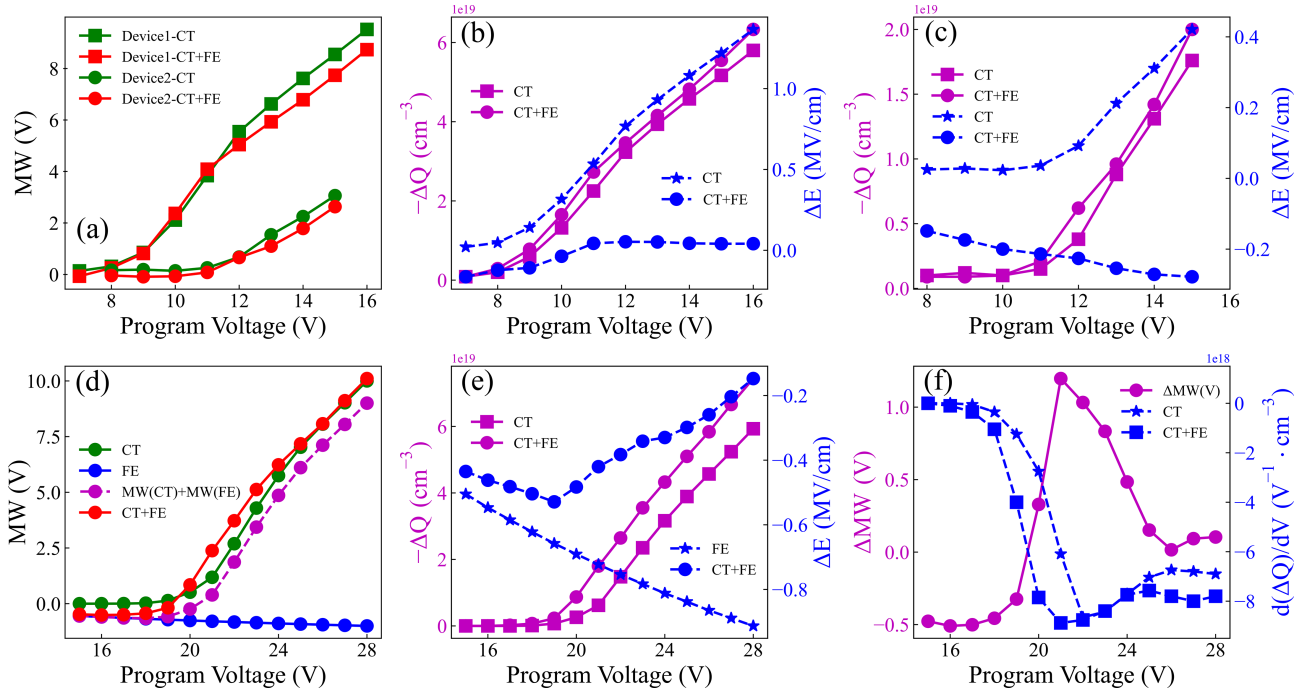

Figure 3 (Color online) (a) Memory windows at different program voltages, and the average trapped charge density and HZO electric field variations in (b) device 1 with fast and (c) device 2 with slow tunneling rates in simulations. (d) Memory window and (e) average trapped charge density and HZO electric field variations for the device with a medium tunneling rate. (f) Maximum MW enhancement by FE, $\Delta\mathrm{MW} = \mathrm{MW(CT + FE)} - \mathrm{MW(CT)}$, coincident with the extreme point of $\mathrm{d}(\Delta Q)/\mathrm{d}V$.

counteracting effect. Figure 2 shows the *C-V* measurements of the two MFINIS-FeFETs, with an AC frequency of 100 kHz and an amplitude of 30 mV. With an increase in the sweeping voltage, the MW of the measured flatband voltages from the forward and backward scanning *C-V* curves is calculated. For both devices, the flatband voltages of PGM are larger than those of the ERS state, suggesting that CT is the primary mechanism. When applying small voltages, PGM and ERS flatband voltages increase in Device 1 because the hole tunneling efficiency is much lower, and the ERS process cannot completely offset trapped electrons from PGM. However, minimal CT occurs in Device 2, and it shows a decreasing tendency at voltages of 8–10 V as a result of the MW counteracting effect arising from the increased FE. At a high voltage, Device 1 shows much larger MW (9.09 V) than Device 2 (2.34 V) because of the thinner tunneling layer and the greater CT capability. Overall, the *C-V* and MW results indicate that CT plays a more significant role than FE in contributing to the MW.

To conduct an in-depth analysis, we perform TCAD simulations comparing FeFET with and without FE after calibration with experimental data. Despite the limited CT enhancement, the MW of MFINIS-FeFET with FE is smaller because of the larger MW counteracting effect, as shown by the differences in trapped charge and HZO electric field shown in Figures 3(a)–(c). However, by varying the tunneling efficiency to a moderate value through adjustment of the tunneling mass, the MW is enhanced by FE when the PGM/ERS voltage is increased from 20 to 25 V, despite the opposite MW contributions from CT and FE, as shown in Figure 3(d). However, at voltages from 15 to 20 V and 25 to 28 V, FE led to more distinct MW counteracting. CT enhancement and suppression of the electric field are shown in Figure 3(e), and the positive f and g can be calculated through (5). Interestingly, the

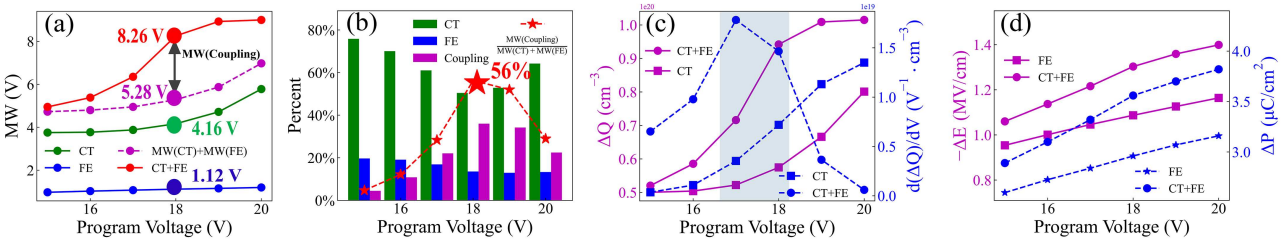

Figure 4 (Color online) (a) Voltage-dependent MW components: MW(CT + FE), MW(CT), MW(FE) and MW(coupling); (b) MW(coupling) contribution reaching 36% (2.98 V/8.26 V) of total MW(CT + FE), with MW(CT) + MW(FE) intensified by 56% (2.98 V/5.28 V) at 18 V; (c) behavior in the vicinity of the extreme point of d(ΔQ)/dV; (d) increases in HZO electric field difference ΔE and polarization difference ΔP between the PGM and ERS state with program voltage.

extreme point of maximum MW enhancement (1.2 V) coincides with the differential of the trapped charge versus the program voltage (21 V), as shown in Figure 3(f), indicating that the strength of the FE-CT coupling effect is closely related to the influence of voltage on CT ability.

Such enhancement of the tunneling efficiency suggests that ferroelectric HZO can increase the voltage across the oxide, which is consistent with our former analysis. When charge tunneling is either too easy or too hard, an increase in voltage has little effect. The MW counteracting effect dominates and leads to the narrowing of the MW. Only in the range where tunneling is strongly voltage-dependent can a slight increase in voltage significantly enhance CT to surpass the negative MW counteracting effect. As shown in Appendix C, replacing the blocking oxide with an appropriately thick ferroelectric HZO layer in a custom 3D NAND architecture and utilizing the CT enhancement effect provide an enhanced incremental step pulse programming (ISPP) threshold voltage in 3D MFINIS-stack FeNAND. Although the maximum threshold voltage and MW decrease because of the MW counteracting effect, this trade-off may be overcome in future investigations using anti-ferroelectric ZrO_2 or $Hf_{0.25}Zr_{0.75}O_2$ (Hf:Zr = 1:3).

3.2 Memory window enhancement in MINIFIS-FeFET

Unlike the competitive effect on CT enhancement and MW counteracting in the CSI-dominated MFINIS-FeFET, CT and FE are mutually reinforcing in all aspects of the GSI-dominated MINIFIS-FeFET. To reduce the operating voltage, high-k Al_2O_3 is used in the Ch.IL and F.IL blocking layers during the TCAD simulations. Building upon prior research on the dependence of FeFET performance on various parameters [55–59], a series of reliable electrical results demonstrating consistency with experiments are acquired. As shown in Figure 4, MW of MINIFIS-FeFET with both CT and FE is larger than the sum of MW from pure CT and FE, which further confirms the existence of an external contribution from FE-CT coupling. As the PGM/ERS voltage increases from 15 to 18 V, the MW contribution from FE, MW(FE), is lower than 20%, while the contribution from CT is more than 50%. In the simulation, MW(FE) is consistently smaller than $2E_c \cdot d$, where E_c is about 1 MV cm^{-1}. The coupling contribution, MW(coupling), is nearly zero at 15 V, but reaches 36% (2.98 V/8.26 V) at 18 V, intensifying the total MW of CT and FE, MW(CT) + MW(FE), by 56% (from 5.28 to 8.26 V). Subsequently, MW(coupling) starts decreasing. Notably, the dramatic increase in the MW occurs near the extreme point of d(ΔQ)/dV, similar to that shown in Figure 3(f). In addition to MW enlargement, the increased trapped charge with increasing PGM/ERS voltage facilitates a higher electric field and remanent polarization in FeFETs with CT and FE as a result of the FE-CT coupling mechanism.

According to (4), the thickness of G.IL also plays an important role in the MW. The results of gate-stack engineering under 15 and 20 V PGM/ERS voltages are shown in Figure 5, where the MW and contribution percentages show opposite trends with increasing oxide thickness. Under a 15 V PGM/ERS voltage, hole tunneling diminishes across the 2.5 nm oxide layer, resulting in a sudden drop in trapped charge, MW(CT), and MW(CT+FE). At 20 V, FE significantly improves hole tunneling, leading to a 35% MW contribution (3.5 V/9.8 V) or a 55% (3.5 V/6.3 V) intensification from coupling at 3.5 nm. In both cases, MW(FE) slowly decreases as the oxide thickness increases because of the reduced voltage applied to the ferroelectric layer. Therefore, the optimum oxide thickness depends strongly on the charge tunneling ability and program voltage. Moreover, an FE-CT coupling enhancement phenomenon is realized in 3D MINIFIS-FeNAND when the influence of curvature is considered, as shown in Appendix C.

By varying the ferroelectric polarization, it is found that the coupling enhancement reaches a maximum when the saturation polarization is 8 μC cm^{-2}, as shown in Figure 6(a). The improvement in hole trapping induced by ferroelectricity leads to a significant variation in the PGM threshold voltage until saturation, which is attributed to the multidomain property and polarization degradation effect of HZO. As the concentration increases in Figure

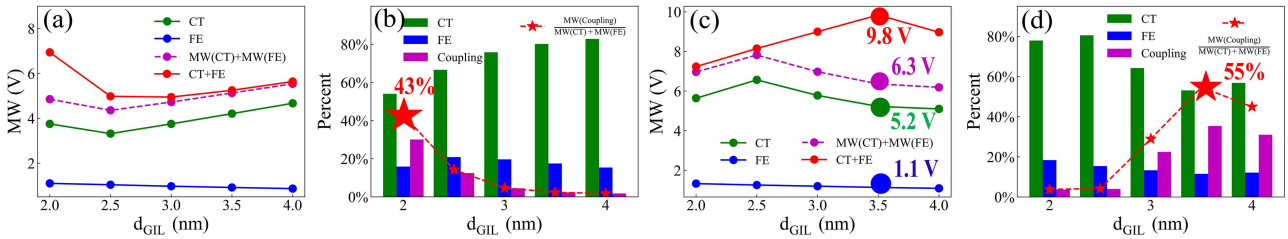

Figure 5 (Color online) Thickness-dependent MW of MINIFIS-FeFET under program voltages of (a) 15 V and (c) 20 V. (b) Reduced coupling contribution due to suppressed hole tunneling; (d) coupling contribution increasing to a maximum of 35% in total MW (or a 55% enhancement) at 3.5 nm, followed by a decrease.

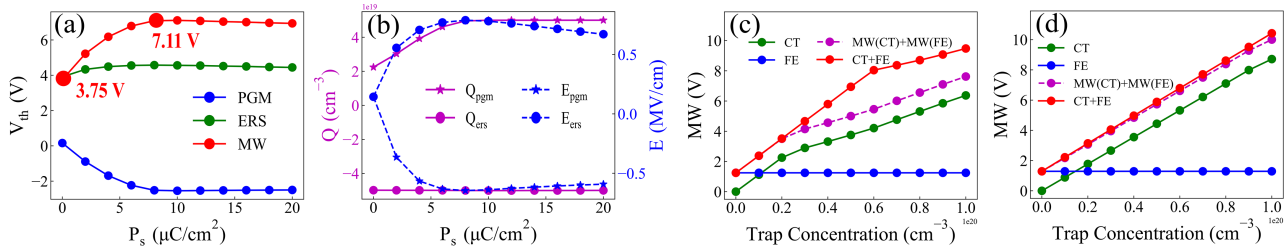

Figure 6 (Color online) Enhanced polarization increasing (a) the MW and (b) trapped charge. MW dependence on (c) free and (d) fixed trap concentrations.

6(c), the coupling enhancement continues to increase until the trap concentration reaches the maximum trapped hole density of 6×10^{19} cm^{-3}. Subsequently, the FE-CT coupling contribution begins to decrease. By setting fixed trapped charges, the MW contribution of the coupling term nearly diminishes, while the electric field and polarization increase with trapped charge density. Consequently, we conclude that the enlargement of MW is mainly derived from the enhancement of CT by ferroelectric polarization. For future experimental validation, such increased ferroelectric polarization may be achieved by accurately controlling the proportion of doped Zr.

4 Conclusion

In summary, in addition to deriving the theoretical formula for the MW of FeFETs, we also clarify the physical mechanism of FE-CT coupling and the mutual reinforcement effect between the trapped charge and remanent polarization. For FeFETs with CSI, such coupling can lead to MW suppression/enlargement, depending on the competition between the CT boosting and MW counteracting effects. For FeFETs with GSI, the MW is always enlarged, and FE-CT coupling can increase the MW by 50% relative to the noncoupled baseline.

Acknowledgements This work was supported by National Key Research and Development Program Young Scientist Project of China (Grant No. 2023YFB4402500) and National Natural Science Foundation of China (Grant No. 62104250).

References

1 Zou X, Xu S, Chen X, et al. Breaking the von Neumann bottleneck: architecture-level processing-in-memory technology. Sci China Inf Sci, 2021, 64: 160404
2 Zhu J, Zhang T, Yang Y, et al. A comprehensive review on emerging artificial neuromorphic devices. Appl Phys Rev, 2020, 7: 011312
3 Yu X, Zhong N, Cheng Y, et al. Ferroelectric materials, devices, and chips technologies for advanced computing and memory applications: development and challenges. Sci China Inf Sci, 2025, 68: 160401
4 Mikolajick T, Slesazeck S, Park M H, et al. Ferroelectric hafnium oxide for ferroelectric random-access memories and ferroelectric field-effect transistors. MRS Bull, 2018, 43: 340–346
5 Böscke T S, Müller J, Bräuhaus D, et al. Ferroelectricity in hafnium oxide thin films. Appl Phys Lett, 2011, 99: 102903
6 Lehninger D, Müller F, Raffel Y, et al. Ferroelectric hafnium oxide: a potential game-changer for nanoelectronic devices and systems. Adv Elect Mater, 2025, 11: 2400686
7 Li X, Tai L, Dou X, et al. Temperature-dependent wakeup behavior in back-end-of-line compatible ultra-thin $Hf_xZr_{1-x}O_2$ ferroelectric film. Sci China Inf Sci, 2025, 68: 160408
8 Shao M H, Zhao R T, Liu H, et al. Challenges and recent advances in HfO_2-based ferroelectric films for non-volatile memory applications. Chip, 2024, 3: 100101
9 Silva J P B, Alcala R, Avci U E, et al. Roadmap on ferroelectric hafnia- and zirconia-based materials and devices. APL Mater, 2023, 11: 089201
10 Kim I J, Lee J S. Ferroelectric transistors for memory and neuromorphic device applications. Adv Mater, 2023, 35: 2206864
11 Schroeder U, Park M H, Mikolajick T, et al. The fundamentals and applications of ferroelectric HfO_2. Nat Rev Mater, 2022, 7: 653–669
12 Park J Y, Choe D H, Lee D H, et al. Revival of ferroelectric memories based on emerging fluorite-structured ferroelectrics. Adv Mater, 2023, 35: 2204904
13 Chen H, Zhou X, Tang L, et al. HfO_2-based ferroelectrics: from enhancing performance, material design, to applications. Appl Phys Rev, 2022, 9: 011307

14 Dutta S, Ye H, Khandker A A, et al. Logic compatible high-performance ferroelectric transistor memory. IEEE Electron Device Lett, 2022, 43: 382–385
15 Hsain H A, Lee Y, Materano M, et al. Many routes to ferroelectric HfO_2: a review of current deposition methods. J Vacuum Sci Tech A, 2022, 40: 010803
16 Luo Q, Cheng Y, Yang J, et al. A highly CMOS compatible hafnia-based ferroelectric diode. Nat Commun, 2020, 11: 1391
17 Liu C, Shen Z, Mao W, et al. A parallel computing-in-memory accelerator utilizing FeRAM array with retention loss correction. Sci China Inf Sci, 2025, 68: 160409
18 Yu J, Guo S, Zhang J, et al. 3D trench $Hf_{0.5}Zr_{0.5}O_2$-based 32 Kbit 1T1C FeRAM chip with 2/5 ns write/read speed, low power consumption (0.605 pJ/bit) and prominent high-temperature reliability (Baking@ 175°C). In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024
19 Ramaswamy N, Calderoni A, Zahurak J, et al. NVDRAM: a 32 Gb dual layer 3D stacked non-volatile ferroelectric memory with near-DRAM performance for demanding AI workloads. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2023
20 Wang Y, Tao L, Guzman R, et al. A stable rhombohedral phase in ferroelectric $Hf(Zr)_{1+x}O_2$ capacitor with ultralow coercive field. Science, 2023, 381: 558–563
21 Sung M, Rho K, Kim J, et al. Low voltage and high speed 1Xnm 1T1C FE-RAM with ultra-thin 5 nm HZO. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2021
22 Zeng M, Yan S, Liu S, et al. Improvement with low operation voltage in ultrathin La-doped $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric capacitors. Sci China Inf Sci, 2025, 68: 160402
23 Chen B, Liu Y, Wu Y, et al. Co-optimization of ferroelectric gate stacks on operation voltage and memory window for next-generation NAND flash. Sci China Inf Sci, 2025, 68: 160404
24 Liu Y, Lu X, Li S, et al. Enhanced memory window and reliability of α-IGZO FeFET enabled by atomic-layer-deposited HfO2 interfacial layer. Sci China Inf Sci, 2025, 68: 160405
25 Li W, Zhou Z, Wang L, et al. An energy-efficient FeFET-based computing-in-memory macro using BEOL-integrated HZO ferroelectric capacitors. Sci China Inf Sci, 2025, 68: 209405
26 Xu J, Zhao J, Zhang H, et al. An AND-type 1T-FeFET array with robust write and read operations. Sci China Inf Sci, 2025, 68: 129404
27 Chen L, Zhu R, Gao X, et al. A novel high endurance HZO FeFET with monolayer graphene inserted in the gate oxide. Nanoscale, 2025, 17: 18756–18765
28 Li Q, Wang S, Li Z, et al. High-performance ferroelectric field-effect transistors with ultra-thin indium tin oxide channels for flexible and transparent electronics. Nat Commun, 2024, 15: 2686
29 Cheema S S, Shanker N, Wang L C, et al. Ultrathin ferroic HfO_2-ZrO_2 superlattice gate stack for advanced transistors. Nature, 2022, 604: 65–71
30 Mulaosmanovic H, Breyer E T, Dünkel S, et al. Ferroelectric field-effect transistors based on HfO_2: a review. Nanotechnology, 2021, 32: 502002
31 Greig S R, Firby C J, Muneshwar T, et al. A plasmon-electron addressable and CMOS compatible random access memory. Sci Adv, 2025, 11: eadr1172
32 Zheng N, Li J, Sun H, et al. Ferroelectric tunnel junctions integrated on semiconductors with enhanced fatigue resistance. Sci Adv, 2025, 11: eads0724
33 Wang H, Guan Z, Li J, et al. Silicon-compatible ferroelectric tunnel junctions with a $SiO_2/Hf_{0.5}Zr_{0.5}O_2$ composite barrier as low-voltage and ultra-high-speed memristors. Adv Mater, 2024, 36: 2211305
34 Wu Z, Duan T, Tian Z, et al. Ferroelectric tunnel junctions based on a HfO_2/dielectric composite barrier. Appl Phys Lett, 2024, 125: 112903
35 Yu J, Wang T, Li Z, et al. Improved ferroelectricity and tunneling electro resistance in Zr-Rich $Hf_xZr_{1-x}O_2$ ferroelectric tunnel junction. IEEE Electron Device Lett, 2022, 44: 245–248
36 Cheng W L, Chen D, Liu W, et al. Y-doped HfO_2 ferroelectric memristor for information processing and neuromorphic computing. ACS Appl Mater Interfaces, 2025, 17: 32646–32656
37 Lederer M, Kämpfe T. Synaptic devices based on ferroelectric hafnium oxide: recent advances, challenges, and future perspectives. Appl Phys Lett, 2025, 126: 130503
38 Zhang J, Xu K, Lu L, et al. Ferroelectric/Antiferroelectric $HfZrO_x$ artificial synapses/neurons for convolutional neural network–spiking neural network neuromorphic computing. Nano Lett, 2025, 25: 13739–13747
39 Zhao L, Fang H, Wang J, et al. Ferroelectric artificial synapses for high-performance neuromorphic computing: status, prospects, and challenges. Appl Phys Lett, 2024, 124: 030501
40 Wu S, Zhang X, Cao R, et al. Multi-state nonvolatile capacitances in HfO_2-based ferroelectric capacitor for neuromorphic computing. Appl Phys Lett, 2024, 124: 102902
41 Cui T, Chen D, Dong Y, et al. Can interface layer be really free for $Hf_xZr_{1-x}O_2$ based ferroelectric field-effect transistors with oxide semiconductor channel? IEEE Electron Device Lett, 2024, 45: 368–371
42 Cho S, Toprasertpong K, Takenaka M, et al. Unveiling memory-window narrowing mechanism after bipolar cycling in HZO/Si FeFETs: critical role of hole trap generation and carrier de-trapping behavior. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024
43 Yoo S, Choe D H, Lee H J, et al. An analytical interpretation of the memory window in ferroelectric field-effect transistors. Appl Phys Lett, 2023, 123: 222902
44 Zhou Y, Liang Z, Luo W, et al. Ferroelectric and interlayer co-optimization with in-depth analysis for high endurance FeFET. In: Proceedings of International Electron Devices Meeting (IEDM), 2022
45 Toprasertpong K, Takenaka M, Takagi S. On the strong coupling of polarization and charge trapping in HfO_2/Si-based ferroelectric field-effect transistors: overview of device operation and reliability. Appl Phys A, 2022, 128: 1114
46 Sun X, Zhang Y, Xiang J, et al. The effect of interface traps at the Si/SiO_2 interface on the transient negative capacitance of ferroelectric FETs. IEEE Trans Electron Devices, 2021, 68: 4735–4740
47 Huang Y, Yuan H, Gong T, et al. In-depth understanding of nitridation-induced endurance enhancement in FeFETs: defect properties and dynamics characterized by nonradiative multi-phonon model. IEEE Trans Electron Devices, 2024, 71: 5388–5392
48 Agarwal A, Walke A M, Ronchi N, et al. Study of endurance performance of SiO_2 interfacial layer scaling through O scavenging in Si channel n-FeFET with Si:HfO_2 ferroelectric layer. IEEE Trans Electron Devices, 2024, 71: 4619–4625
49 Chen Z, Ronchi N, Walke A, et al. Improved MW of IGZO-channel FeFET by reading scheme optimization and interfacial engineering. In: Proceedings of IEEE International Memory Workshop (IMW), 2023
50 Fernandes L, Venkatesan P, Tian M, et al. Comparative study of channel materials for ferroelectric NAND applications. In: Proceedings of IEEE International Memory Workshop (IMW), 2025
51 Breuil L, Popovici M, Stiers J, et al. Optimization of retention in ferroelectricity boosted gate stacks for 3D NAND. In: Proceedings of IEEE International Memory Workshop (IMW), 2023
52 Higashi Y, Bastos J, Chasin A, et al. Investigation of the impact of ferroelectricity boosted gate stacks for 3D NAND on short time data retention and endurance. In: Proceedings of IEEE International Reliability Physics Symposium (IRPS), 2024
53 Shin E, Shin S, Lee S, et al. Capacitance boosting by anti-ferroelectric blocking layer in charge trap flash memory device. In: Proceedings of International Electron Devices Meeting (IEDM), 2020
54 Ali T, Mertens K, Olivo R, et al. A novel hybrid high-speed and low power antiferroelectric HSO boosted charge trap memory for

high-density storage. In: Proceedings of International Electron Devices Meeting (IEDM), 2020
55 Yoo S, Kim T J, Nam S G, et al. Ferroelectric transistors for low-power NAND flash memory. Nature, 2025, 648: 320–326
56 Yoo S, Kim D, Choe D, et al. Highly enhanced memory window of 17.8 V in ferroelectric FET with IGZO channel via introduction of intermediate oxygen-deficient channel and gate interlayer. In: Proceedings of IEEE Symposium on VLSI Technology and Circuits, 2024
57 Hu T, Jia X, Han R, et al. Effect of top Al_2O_3 interlayer thickness on memory window and reliability of FeFETs with TiN/Al_2O_3/$Hf_{0.}5Zr_{0.}5O_2$/SiO_x/Si (MIFIS) gate structure. IEEE Trans Electron Devices, 2025, 72: 5958–5965
58 Han R, Yang J, Hu T, et al. Improved memory window and retention of silicon channel $Hf_{0.5}Zr_{0.5}O_2$ FeFET by using SiO_2/HfO_2/SiO_2 gate side interlayer. IEEE International Reliability Physics Symposium (IRPS), 2025
59 Qin Y, Chakraborty S, Zhao Z, et al. Clarifying the role of ferroelectric in expanding the memory window of ferroelectric fets with gate-side injection: isolating contributions from polarization and charge trapping. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024
60 Venkatesan P, Khan A. Ferroelectrics for vertical NAND flash applications. In: Proceedings of IEEE International Memory Workshop (IMW), 2025
61 Shon M, Park C, Ravindran P V, et al. Modeling dynamic interplay between charge traps and polarization for memory window enhancement in gate injection layers. In: Proceedings of IEEE International Reliability Physics Symposium (IRPS), 2025
62 Kuk S H, Kim B H, Park Y, et al. Superior QLC retention (10 Years, 85°C) and record memory window (12.2 V) by gate stack engineering in ferroelectric FET: from "MIFIS" to" MIKFIS". In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024
63 Kim K, Lim S, Woo J, et al. Gate-stack optimization to mitigate the cylindrical effect in ferroelectric VNAND. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024
64 Zhou Z, Jiao L, Zheng Z, et al. First study of the charge trapping aggravation induced by anti-ferroelectric switching in the MFIS stack. In: Proceedings of IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), 2023
65 Hu T, Sun X, Bai M, et al. Enlargement of memory window of Si channel FeFET by inserting Al_2O_3 interlayer on ferroelectric $Hf_{0.5}Zr_{0.5}O_2$. IEEE Electron Device Lett, 2024, 45: 825–828
66 Lim S, Kim T, Myeong I, et al. Comprehensive design guidelines of gate stack for QLC and highly reliable ferroelectric VNAND. In: Proceedings of International Electron Devices Meeting (IEDM), 2023
67 Yoon S, Hong S I, Choi G, et al. Highly stackable 3D ferroelectric NAND devices: beyond the charge trap based memory. In: Proceedings of IEEE International Memory Workshop (IMW), 2022
68 Choi H, Kim G, Lee S, et al. Positive interaction between charge trapping and polarization switching in metal-interlayer-ferroelectric-interlayer-silicon (MIFIS) ferroelectric field-effect transistor. IEEE Electron Device Lett, 2024, 45: 2351–2354
69 Hao T, Zeng B, Sun Z, et al. Coupling effects of interface charge trapping and polarization switching in HfO_2-based ferroelectric field effect transistors. APL Mater, 2024, 12: 011108
70 Zhang B, Hong P, Hou J, et al. Doped HfO_2-based ferroelectric-aided charge-trapping effect in MFIS gate stack of FeFET. J Appl Phys, 2023, 133: 164103
71 Yoo S, Choe D H, Lee H J, et al. An analytical interpretation of the memory window in ferroelectric field-effect transistors. Appl Phys Lett, 2023, 123: 222902
72 Lee J G, Kim J, Suh D I, et al. Memory window expansion for ferroelectric FET based multilevel NVM: hybrid solution with combination of polarization and injected charges. In: Proceedings of IEEE International Memory Workshop (IMW), 2022. 1–4
73 Zhang B, Li C, Hong P, et al. Ferroelectric control of the perpendicular magnetic anisotropy in PtCoRu/$Hf_{0.5}Zr_{0.5}O_2$ heterostructure. Appl Phys Lett, 2021, 119: 022405
74 Hou J, Xu C, Li Q, et al. Enhanced memory window of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ by NH_3 treatment. J Appl Phys, 2025, 137: 164104
75 Jiang B. Computationally efficient ferroelectric capacitor model for circuit simulation. In: Proceedings of Symposium on VLSI Technology, 1997. 141–142

Appendix A Memory window formula

Applying Gauss's law to each layer of the cell structure, the MW formula can be calculated. For MFINIS-FeFET,

$$(\varepsilon_0\varepsilon_{FE}E_{FE}+P)-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=-Q, \tag{A1}$$

$$\varepsilon_0\varepsilon_{F.IL}E_{F.IL}-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=-Q, \tag{A2}$$

$$\varepsilon_0\varepsilon_{CTL}\overline{E_{CTL}}-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=-\alpha Q, \tag{A3}$$

where Q is the average trapped charge surface density in CTL (C cm^{-2}). Since the charge distribution ρ is nonuniform, the electric field within the CTL exhibits spatial dependence, and the statistical average and a correction factor α are used. By defining the direction pointing from channel to gate as the y-axis, and the location of the CTL/Ch.IL interface as $y=0$, the electric field in CTL is

$$\varepsilon_0\varepsilon_{CTL}E(y)-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=-\int_0^y\rho\mathrm{d}y', \tag{A4}$$

$\overline{E_{CTL}}$ and α are

$$\overline{E_{CTL}}=\frac{\int_0^{d_{CTL}}E(y)\mathrm{d}y}{d_{CTL}}, \tag{A5}$$

$$\alpha=\frac{\int_0^{d_{CTL}}[\int_0^y\rho\mathrm{d}y']\mathrm{d}y}{d_{CTL}\int_0^{d_{CTL}}\rho\mathrm{d}y}. \tag{A6}$$

If $\rho=constant$, $\alpha=1/2$ is obtained. In the TCAD simulation, the unit of output trapped charge density is cm^{-3}, and it is necessary to multiply the thickness of CTL, 4 nm, and the elementary charge of 1.6×10^{-19} C to obtain Q in the above equations. The gate voltage is

$$V_g=\phi_{ms}+\psi_s+E_{Ch.IL}d_{Ch.IL}+\overline{E_{CTL}}d_{CTL}+E_{F.IL}d_{F.IL}+E_{FE}d_{FE}. \tag{A7}$$

For MINIFIS-FeFET,

$$(\varepsilon_0\varepsilon_{FE}E_{FE}+P)-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=0, \tag{A8}$$

$$\varepsilon_0\varepsilon_{F.IL}E_{F.IL}-\varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL}=0, \tag{A9}$$

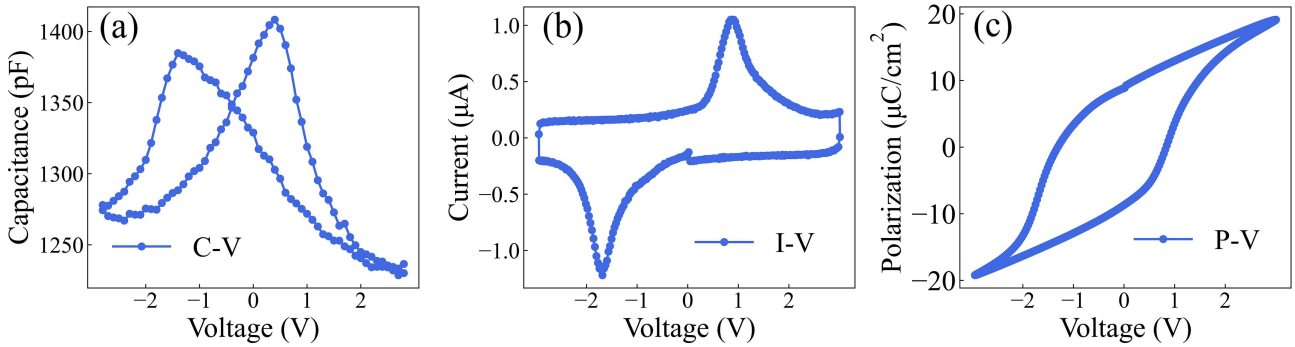

Figure B1 (Color online) Ferroelectric nature of HZO verified through the characterization of (a) *C-V*, (b) *I-V*, and (c) *P-V*.

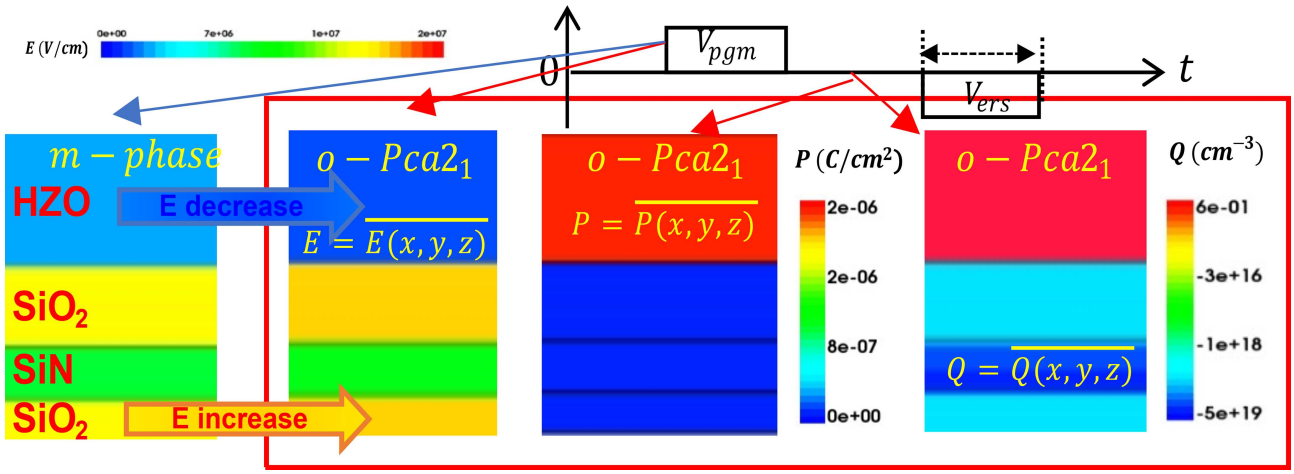

Figure B2 (Color online) Electric field difference in HZO between monoclinic (m) and orthorhombic $Pca2_1$ phases under identical programming voltages, including average remanent polarization P and trapped charge density Q.

$$\varepsilon_0\varepsilon_{CTL}\overline{E_{CIL}} - \varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL} = -\alpha Q, \tag{A10}$$

$$\varepsilon_0\varepsilon_{G.IL}E_{G.IL} - \varepsilon_0\varepsilon_{Ch.IL}E_{Ch.IL} = -Q. \tag{A11}$$

The gate voltage is

$$V_g = \phi_{ms} + \psi_s + E_{Ch.IL}d_{Ch.IL} + E_{FE}d_{FE} + E_{F.IL}d_{F.IL} + \overline{E_{CTL}}d_{CTL} + E_{G.IL}d_{G.IL}. \tag{A12}$$

For the same total capacitance in *C-V* testing or the drain current in I_d–V_g measurements (depending on device feature size), ϕ_{ms}, ψ_s and $E_{Ch.IL}$ are expected to be the same. Therefore, we can write E_i as functions of $E_{Ch.IL}$ from A1–A3 and A8–A11. Then the MW is

$$\mathrm{MW} = |V_g(PGM) - V_g(ERS)| = \left|\sum_i \Delta E_i d_i\right|, \tag{A13}$$

where $i = FE, F.IL, CTL, G.IL$.

Appendix B Experiment and simulation details

In this work, the thickness of the HZO layer is 10 nm. The ferroelectricity of the layer is measured by a Keithley 4200-SCS, as shown in Figure B1. The typical butterfly *C-V* curve and *P-V* hysteresis loop reflect the ferroelectric properties of HZO.

In the TCAD simulation, the ferroelectric *P-V* loop is described using the Preisach-based model [75]:

$$P = P_s \cdot \tanh\left[\ln\frac{P_s + P_r}{P_s - P_r} \cdot \frac{(E \pm E_c)}{2E_c}\right], \tag{B1}$$

where P_s, P_r, E_c are the saturation polarization, remanent polarization, and coercive field. The thickness of SiN is 4 nm, with a single-level electron/hole trap concentration equal to 5×10^{19} cm^{-3}. The tunneling mass is approximately 0.36 m_0–0.5 m_0, the trap volume is 10^{-17} cm^{-3}, and nonlocal tunneling from the gate or channel to the CT layer is used in the simulation. The program or erase time period is 10^{-4} s. It is worth emphasizing that the selection of other materials or parameters will lead to different numerical results but will not affect the analysis of physical mechanisms. The average electric field, polarization, and charge density calculations are shown in Figure B2.

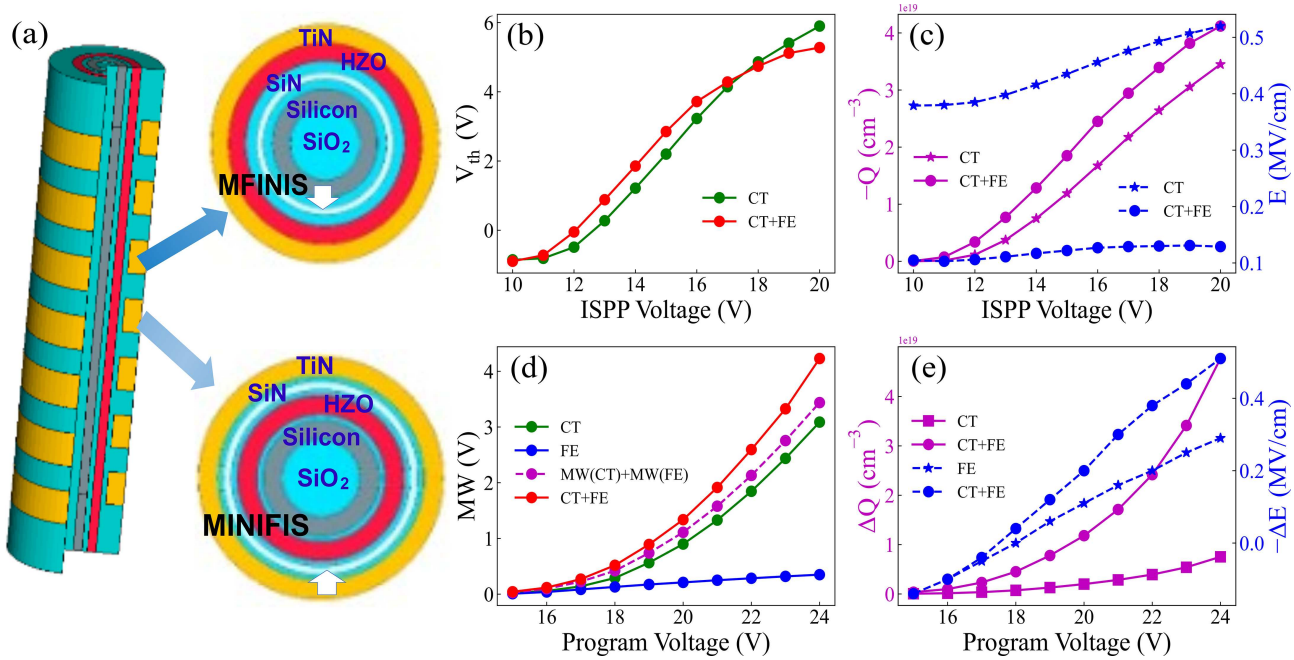

Figure C1 (Color online) (a) Cell structures of 3D FeNAND: top, channel-side injection; bottom, gate-side injection. (b) Threshold voltage and (c) trapped electron density and HZO electric field with ISPP voltage for 3D MFINIS-FeNAND. (d) MW and (e) trapped charge and HZO electric field with program voltage for 3D MINIFIS-FeNAND.

Appendix C Application in 3D NAND

In 3D structures, the electric field of the inner layers is higher than that of the outer layers. Consequently, 3D MFINIS-FeNAND with CSI achieves a lower programming voltage than its 2D counterpart, while MINIFIS-FeNAND with GSI exhibits an inverse dependence, as shown in Figure C1. These results underscore the need to incorporate the curvature effects into the design of 3D gate-stack FeNAND.