SCIENCE CHINA
Information Sciences

• Supplementary File •

High-isolation radio frequency switches enabled by Cu_2S/GeSe conductive bridge threshold switch

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Appendix A Device Fabrication and Characterization

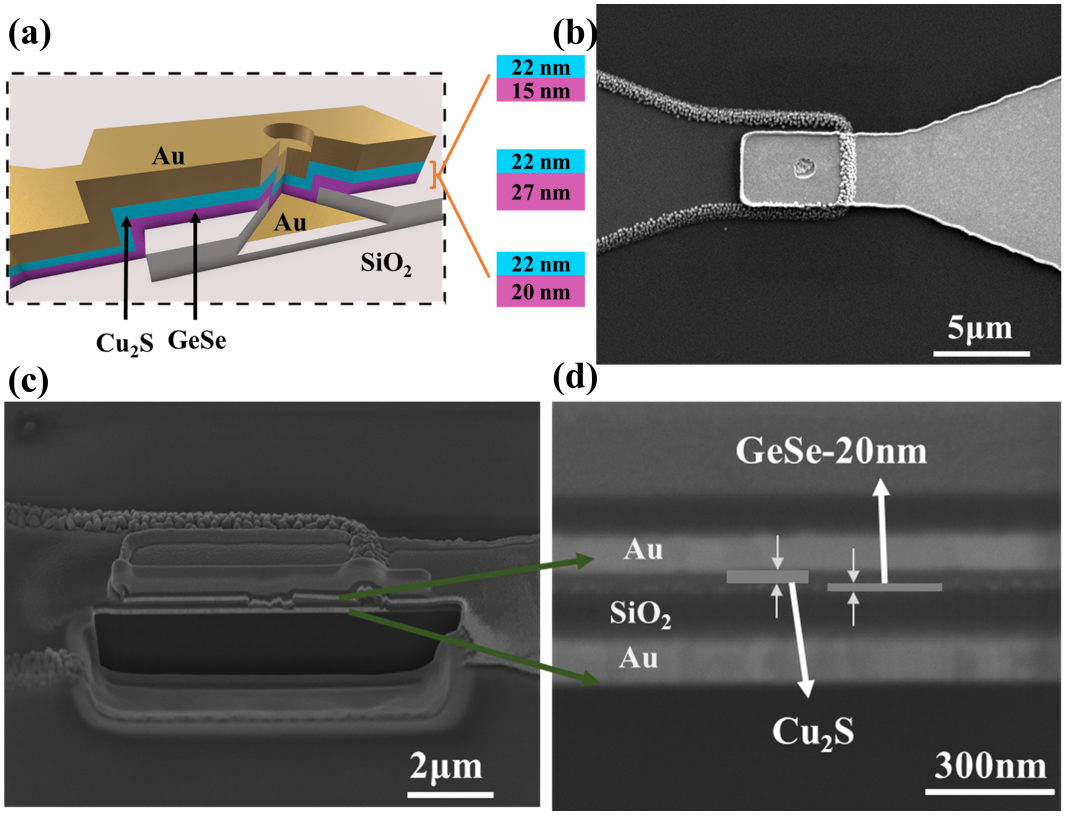

Figure A1 Device architecture and material configuration. (a) Cross-sectional view of the active switching region, illustrating the vertical integration of the electrodes and Cu_2S/GeSe functional layers, with varying GeSe thicknesses (15, 20 and 27 nm). (b) Top-view SEM image of the fabricated RF switch, detailing the via-hole morphology. (c) Cross-sectional FIB-SEM image of the via-hole structure. (d) The image shows the uniform thickness of each thin film layer, with the GeSe functional layer having a thickness of 20 nm.

The Cu_2S/GeSe-based RF switch employs a vertical via structure, comprising the common ground, RF signal electrodes, and the functional material stack, as illustrated in Figure A1(a). The device was fabricated on a high-resistivity silicon substrate to minimize substrate loss. Patterning for all layers was performed using ultraviolet (UV) lithography. The fabrication process commenced with the formation of the bottom electrode, where a Cr/Au (10 nm/100 nm) bilayer was deposited by electron-beam evaporation (EBE). To confine the active switching region, a 100 nm SiO_2 isolation layer was deposited using plasma-enhanced chemical vapor deposition (PECVD). Subsequently, a circular via with a 1 μm diameter was defined and opened through the SiO_2 layer by inductively coupled plasma (ICP) etching, exposing the bottom electrode.

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Following this, the functional stack was integrated. GeSe switching layers with designated thicknesses of 15 nm, 20 nm, and 27 nm were first deposited via RF magnetron sputtering. This was followed by the deposition of a Cu_2S ion source layer (approximately 22 nm thick). To ensure strict thickness accuracy, the deposition rate was calibrated in advance using flat control samples, with the precise thickness verified by a surface step profilometer. Furthermore, the structural integrity of the optimized device was verified using focused ion beam scanning electron microscopy (FIB-SEM). Top-view and cross-sectional profiles (Figure A1(b) and (c)) confirm the precise definition of the device via, while high-resolution cross-sectional imaging precisely corroborates the targeted 20 nm thickness of the GeSe layer (Figure A1(d)). The slight morphological undulations observed in the cross-section reflect the conformal deposition over the topological variations of the underlying etched SiO_2 via. Based on this highly stable calibrated rate, the 15 nm and 27 nm variants were achieved by strictly scaling the sputtering duration under identical plasma conditions. Finally, the top electrode was patterned and deposited, and the device fabrication was completed using a standard lift-off process.

Appendix B Optimization of GeSe Thickness

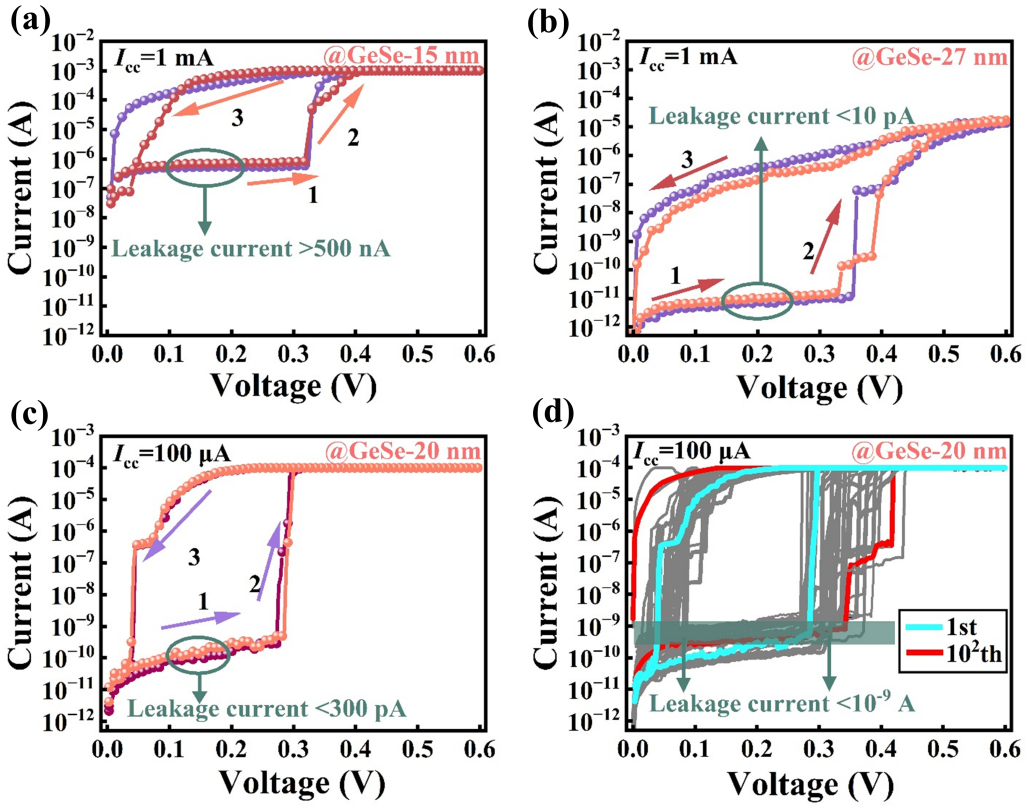

Figure B1 Impact of GeSe layer thickness on the electrical switching characteristics. (a) I-V characteristics of the device with a 15-nm-thick GeSe layer, exhibiting a high off-state leakage current of approximately 500 nA. (b) Characteristics of the device with a 27-nm-thick GeSe layer; while leakage is suppressed below 10 pA, the on-state current is severely limited to < 10 μA. (c) Optimized characteristics of the device with a 20-nm-thick GeSe layer, achieving a balanced performance with low leakage (<300 pA) and high on-state current. (d) DC cycling endurance test of the optimized 20-nm device, demonstrating stable switching behavior over 100 consecutive cycles.

The switching characteristics of the fabricated RF device are fundamentally governed by the functional Cu_2S/GeSe heterostructure. In this design, the Cu_2S layer acts as a reservoir for active Cu ions, while the amorphous GeSe layer functions as the high-resistance solid electrolyte for filament evolution. Consequently, the thickness of the GeSe layer becomes the critical design parameter: it must be thick enough to suppress carrier tunneling (leakage) yet thin enough to allow robust filament formation (drive current). To identify the optimal geometry that reconciles this intrinsic trade-off, we performed systematic current-voltage (I-V) characterization on devices with varying GeSe thicknesses.

For the device with a thin 15 nm GeSe layer (Figure B1(a)), the leakage current reaches 500 nA ($R_{\text{off}} = 400$ kΩ). This high leakage is attributed to ohmic leakage paths originating from non-uniform film coverage and the likely presence of physical pinholes. These pinholes act as localized metallic shorts, providing a direct, low-resistance pathway for current. Conversely, increasing the thickness to 27 nm (Figure B1(b)) successfully blocks leakage (<10 pA, R_{off} =2 GΩ) utilizing the high intrinsic resistivity of the wide-bandgap GeSe [1,2]. However, this excessive thickness impedes the formation of robust filaments, severely throttling the on-state current to only 10 μA ($R_{\text{on}} = 50$ kΩ), which would introduce unacceptable insertion loss for RF applications. The optimal balance is achieved at a thickness of 20 nm, as shown in Figure B1(c). Here, the device maintains a suppressed leakage below 300 pA (R_{off} =600 MΩ) without compromising the on-state drive capability.

Beyond static performance, the optimized device demonstrates robust reliability, maintaining stable switching over 100 consecutive

DC cycles (Figure B1(d)). It is worth noting that a discernible hysteresis and a slight shift in the threshold voltage (V_{th}) are observed during these consecutive DC sweeps. This behavior is attributed to the prolonged electrical stress and substantial Joule heating inherent to quasi-static DC measurements at a high compliance current of 100 μA, which drives excessive Cu^+ injection. During the backward sweep, the retraction of this robust filament occurs gradually, manifesting as hysteresis rather than a sharp snap-back [3]. Crucially, the device entirely recovers its high-resistance state at 0 V, confirming the preservation of its volatile nature. Notably, the turn-on voltage remains very low (<0.8 V), which offers advantages in low-voltage, CMOS logic-compatible driving, eliminating the need for complex high-voltage control circuitry.

Appendix C Switching Kinetics and Reliability

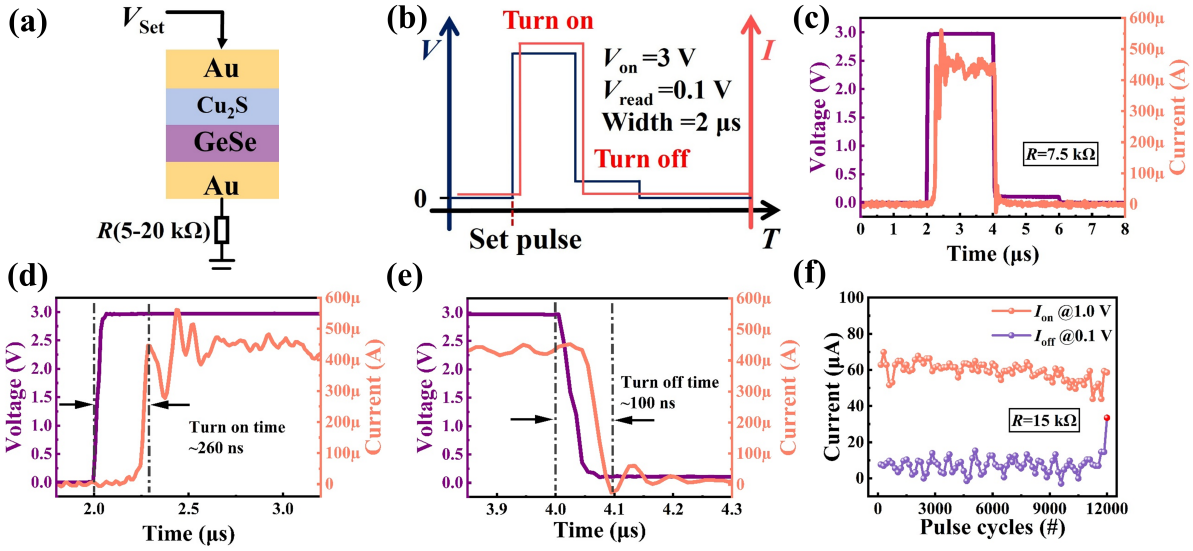

Figure C1 Switching speed and cycle endurance testing of the device. (a) Schematic of the pulse test circuit for measuring switching speed. (b) Schematic diagram of the corresponding pulse sequence. (c) Switching transient response waveform showing the device's turn-on and turn-off processes. (d) Magnified view of the turn-on time (260 ns). (e) Magnified view of the turn-off time (100 ns). (f) DC cycling test results of the device under a 15 kΩ current-limiting resistor, demonstrating a switching lifetime exceeding 12,000 cycles.

The transient response of the device was characterized using an Agilent B1530A Waveform Generator Fast Measurement Unit (WGFMU). The circuit connection method and pulse waveform are shown in the Figures C1(a) and (b). The switching kinetics were characterized by applying a 3 V/2 μs excitation pulse, followed immediately by a 0.1 V read pulse to verify the state transition [4]. The resulting transient waveforms, detailed in Figures C1(c)-(e), reveal a rapid turn-on time of 260 ns and an exceptionally fast turn-off time of 100 ns. Furthermore, we assessed the device's long-term reliability through cycling endurance tests (Figure C1(f)). To mitigate filament overgrowth and prevent stuck-ON failure under prolonged high-current stress, a 15 kΩ series resistor was integrated to regulate the compliance current. Under a cyclic stress of 1 V/2 μs (SET) and 0.1 V/2 μs (READ), the device demonstrated robust operational stability, sustaining over 1.2×10^4 switching cycles before exhibiting degradation. This endurance capability, combined with sub-microsecond switching speeds, underscores the device's potential for agile RF reconfiguration.

Appendix D RF Performance and Benchmarking

Figures D1(a)-(b) elucidate the critical dependence of off-state isolation (S_{21}) on the GeSe layer thickness. For the device with a thin 15 nm GeSe layer, the substantial DC leakage current translates directly into poor RF blocking capability, with isolation degrading to <15 dB (at frequencies >25 GHz) and a deteriorated return loss (S_{11}). In stark contrast, increasing the thickness effectively suppresses the signal leakage.

To validate the reliability and reproducibility of the proposed technology for practical implementations, we systematically evaluated the device-to-device (D2D) uniformity. Figure D1(c) presents the broadband insertion loss and off-state isolation curves measured from 12 distinct optimized Cu_2S/GeSe devices (20 nm GeSe). The RF responses exhibit a tightly grouped distribution across the entire 10 MHz to 40 GHz spectrum. Furthermore, the power handling capability was assessed by characterizing the device under continuous wave signals with varying input powers. As shown in Figure D1(d), the device exhibits stable insertion loss from –30 dBm to –5 dBm, with negligible deviation from small-signal measurements. At 3 dBm, a slight upward shift in S_{21} is observed, indicating the onset of non-linear RF response, likely associated with increased filament heating. The measurement was terminated at 3 dBm due to the built-in protection threshold of the vector network analyzer. While the absolute power handling of CBTS devices in the Cu_2S/GeSe system is currently moderate, this limitation does not preclude their application in low-power scenarios such as receiver front-ends and on-chip calibration networks. Moreover, further performance improvements are anticipated through process optimization, such as enhancing thin film quality and by adopting advanced device architectures like parallel via arrays.

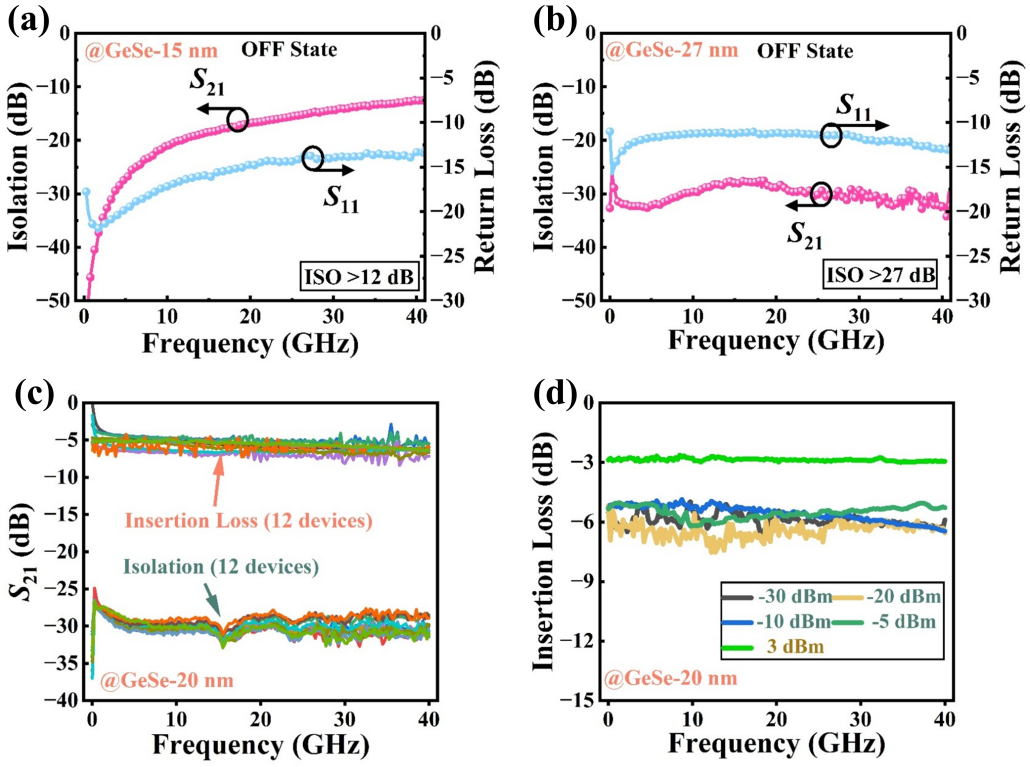

Figure D1 Broadband RF performance of the Cu_2S/GeSe switch as a function of GeSe layer thickness. (a) Off-state isolation (S_{21}) and return loss (S_{11}) of the 15-nm thick device. The isolation exhibits significant spectral fluctuation, degrading to <15 dB at frequencies >25 GHz due to high leakage. (b) Off-state characteristics of the 27-nm thick device, demonstrating robust isolation exceeding 27 dB across the entire bandwidth (10 MHz-40 GHz). (c) Device-to-device (D2D) uniformity demonstrating the broadband insertion loss and isolation curves measured from 12 distinct optimized 20-nm devices. (d) Power handling evaluation showing the ON-state S_{21} responses under varying RF input power levels from -30 dBm to 3 dBm.

Table D1 Performance Benchmark of State-of-the-art RF Switch Technologies

Ref	Technology	Frequency (GHz)	Isolation (dB)	Insertion Loss (dB)	Switching Speed (ns)	Bias (V)
[7]	PCM (GeTe)	DC−67	>15	<1.5	1100	–
[12]	PIN	1.8−2.6	>20	<0.65	260	–
[5]	CMOS (130nm)	57−66	>10	<5.8	<1	<1.2
[10]	RF MEMS	DC−10	>20	<0.8	1800	>30
[6]	CMOS (180nm)	2.4−7.1	>22	<3.3	48	<1
[11]	RF MEMS (SCMC)[1)]	DC−20	>10	<1	100,000	60
[8]	MoS_2	DC−50	>15	<1	30	<1.2
[9]	VO_2	0.1−20	>20	<0.4	100	–
This Work	**CBTS(Cu_2S/GeSe)**	**DC−40**	**>28**	**<6.3**	**260**	**<0.8**

Table D1 benchmarks the proposed Cu_2S/GeSe technology against state-of-the-art RF switching paradigms. The most defining advantage of our device is its exceptional off-state isolation capability across a broad frequency spectrum. As operating frequencies increase, parasitic capacitive coupling typically reduces the blocking performance of traditional CMOS [5, 6], PCM [7], and emerging 2D material and oxide based switches [8, 9], often limiting isolation to 10–20 dB. In stark contrast, the proposed CBTS switch defies this trend, maintaining a robust isolation exceeding 28 dB from DC up to 40 GHz. This superior signal suppression capability is particularly indispensable for interference-critical scenarios, such as on-chip calibration networks, Built-In Self-Test (BIST) routing, and tunable filter selection in receive chains, where signal purity is prioritized over transmission loss. Unlike RF MEMS solutions [10, 11], which mandate high bias voltages (>30 V) and necessitate complex charge-pump circuitry for integration, our device operates within a CMOS-compatible logic window (<0.8 V).

While the current insertion loss (< 6.3 dB) limits the direct application of these devices in the main transceiver front end, this loss is primarily related to the on-resistance of a single nanoscale filament formed under 1 mA current-limited conditions. The on-resistance R_{on} can be further reduced through structural and material optimization to meet standard RF requirements. Architecturally, using a

1) Single-Cantilever Multi-Contact RF-MEMS Switch.

parallel multi-via layout can proportionally reduce the effective resistance; for example, paralleling multiple vias to collaboratively carry large currents can further reduce the on-resistance without affecting the switching characteristics of a single filament. At the material level, the R_{on} can be further minimized by precisely tuning the Cu_xS stoichiometry to increase the mobile ion concentration.

References

1 Okazaki A. The crystal structure of germanium selenide GeSe. J Phys Soc Jpn, 1958, 13: 1151–1155
2 Liu G, Wu L, Chen X, et al. The investigations of characteristics of GeSe thin films and selector devices for phase change memory. J Alloys Compd, 2019, 792: 510–518
3 Wang Z, Rao M, Midya R, et al. Threshold switching of Ag or Cu in dielectrics: materials, mechanism, and applications. Adv Funct Mater, 2018, 28: 1870036
4 Li N, Cai W, Xiang J, et al. Mitigating set-stuck failure in 3D phase change memory: substituting square pulses with surge pulses. Sci China Inf Sci, 2024, 67: 152403
5 Ta C M, Skafidas E, Evans R J. A 60-GHz CMOS transmit/receive switch. In: Proc IEEE Radio Freq Integr Circuits Symp, Honolulu, USA, 2007. 6–12
6 Chung M A, Fan Y H. A high-isolation SPDT T/R switch in 0.18-μm CMOS for Wi-Fi 7 applications. In: Proc IEEE Eurasia Conf IOT, Commun Eng, 2022. 137–140
7 Singh T, Mansour R R. Experimental investigation of performance, reliability, and cycle endurance of nonvolatile DC-67 GHz phase-change RF switches. IEEE Trans Microw Theory Tech, 2021, 69: 4697–4710
8 Kim M, Ge R, Wu X, et al. Zero-static power radio-frequency switches based on MoS_2 atomristors. Nat Commun, 2018, 9: 2524
9 Seo D, Kim D, Ryu J, et al. VO_x-based non-volatile radio-frequency switches for reconfigurable filter. Adv Sci, 2025, 12: e01989
10 Bansal D, Bajpai A, Mehta K, et al. Improved design of ohmic RF MEMS switch for reduced fabrication steps. IEEE Trans Electron Devices, 2019, 66: 4361–4366
11 Liu Y, Liu J, Yu B, et al. A compact single-cantilever multicontact RF-MEMS switch with enhanced reliability. IEEE Microw Wireless Compon Lett, 2018, 28: 191–193
12 Ghorbani F, Dayan A, Zhou J, et al. Linearity enhancement in PIN-diode-based switches. IEEE Trans Microw Theory Tech, 2025, 73: 789–800