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First demonstration of a novel 1.2 kV asymmetric P^+ buried layer 4H-SiC MOSFET with recored short-circuit capability

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SiC MOSFETs are considered promising candidates for next-generation power devices due to their high breakdown voltage and low specific on-resistance ($R_{on,sp}$), however, their short-circuit (SC) capability is still constrained by gate oxide reliability and high power density [1]. Previous approaches, including oxide improvement, JFET width (W_{JFET}) and doping optimization, as well as split-gate and deep P-well designs, can partially enhance SC robustness [2–4], but the improvement remains limited, especially under narrow W_{JFET} and high voltages. Moreover, implementing split-gate structures under narrow W_{JFET} tends to introduce oxide electric-field crowding, further challenging long-term reliability. To address these issues, this work experimentally demonstrates a novel 1.2 kV asymmetric P^+ buried layer MOSFET (ABL-MOS), which enables split-gate integration while effectively suppressing oxide electric-field concentration and reducing SC current density (I_{SC}). As a result, the fabricated devices achieve an SC withstand time (SCWT) of 22 μs at V_{DD} = 800 V, reaching the conventional Si IGBT level, and highlighting the strong potential of the proposed structure for high-reliability power applications.

Design and fabrication. Figure 1(a) shows the schematic view of the ABL-MOS. A P^+ buried layer with a depth of 2.7 μm was formed by 700 keV channeling implantation into a 14 μm n-type epi with 8×10^{15} cm^{-3}. Subsequently, a 2 μm n-type epi with 6×10^{16} cm^{-3} was grown as the CSL. By selecting large alignment marks and performing deep marker etching (exposure size ⩾ 10 μm, etch depth ⩾ 5 μm), the increase in overlay error caused by the coverage of photolithography marks during epi growth was effectively mitigated. Afterward, the P^1 region was formed by channeling implantation, enabling the buried layer to be connected to the source. Finally, a conventional process was used to create an asymmetric structure; the active area is 0.02 cm^2, and the threshold voltage is 4.7 V. The SEM image of the fabricated ABL-MOS is shown in Figure 1(b). Because the channeling implantation is wider at the top and narrower at the bottom, with more pronounced lateral diffusion, the actual width of the buried layer over the JFET (W_{BLO}) is larger than the designed value. In addition, due to the secondary epi growth causing blurring of the photolithography marks, overlay errors still exist. Both of these factors can lead to degradation of the device's $R_{on,sp}$, which needs to be mitigated through careful parameter design and enhanced process control. To investigate the effects of W_{JFET} and the W_{BLO}, devices were fabricated with W_{JFET} values of 1.0, 1.2, and 1.4 μm, and W_{BLO} values of 0.5 and 0.7 μm.

Results and discussion. Figure 1(c) shows the simulated electric field distribution under a 1.2 kV blocking state with different W_{JFET}. Due to the P^+ buried layer beneath the Pwell, the high electric field is constrained below the P^+ buried layer, and the maximum electric field is lower than 2.2 MV/cm. In addition, it can be seen that the corner electric field of the split gate structure does not exceed 2 MV/cm at any structural size. This result indicates that the buried layer effectively reduces the risk of oxide electric field crowding caused by the split gate.

Figures 1(d) and (e) show the measured output characteristics of the ABL-MOS. As the W_{JFET} increases, the cell pitch becomes larger and the $R_{on,sp}$ increases from 7.5 to 8.1 mΩ·cm^2. At W_{JFET} = 1.0 μm, a larger W_{BLO} will intensify the JFET effect of the buried layer, and the $R_{on,sp}$ of W_{BLO} = 0.7 μm is 7.9 mΩ·cm^2. Under this influence, the $R_{on,sp}$ of ABL-MOS hardly changes at low V_{DS}, but as V_{DS} rises, the saturation current of the device significantly decreases. Figure 1(f) show the blocking characteristics of ABL-MOS with different W_{JFET} and W_{BLO} under the blocking current limit of 10 μA. The blocking ability of these devices exceeds 1800 V. Figure 1(g) shows the measured Miller capacitance of the ABL-MOS. It can be observed that the ABL-MOS simultaneously preserves the low Miller capacitance inherent to the split-gate structure, with a minimum Miller capacitance of only 0.65 pF, demonstrating the advantage for fast-switching applications.

Figure 1(h) shows the SC waveforms of the ABL-MOS with a W_{JFET} = 1.0 μm and W_{BLO} = 0.7 μm under V_{DD} = 800 V.

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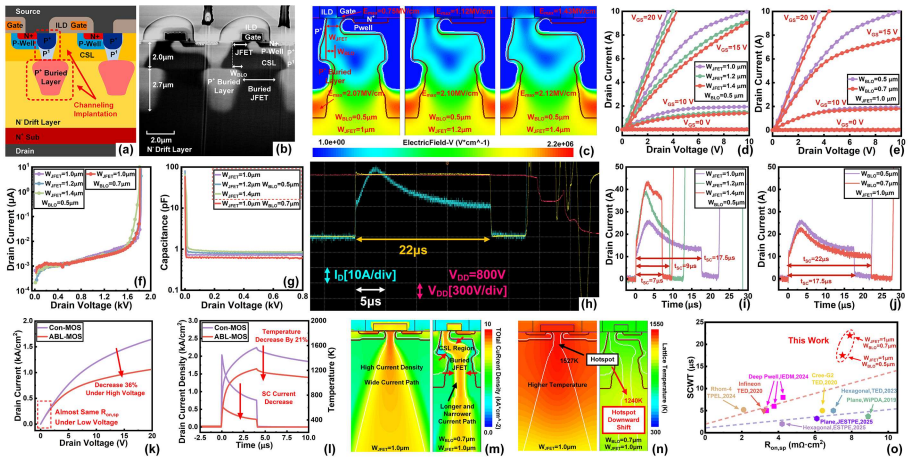

Figure 1 (Color online) (a) The schematic view and (b) SEM image of the ABL-MOS. (c) Simulated electric field distribution of the ABL-MOS with different W_{JFET} at V_{DS} = 1200V. The output characteristics with (d) different W_{JFET} and (e) W_{BLO}. The blocking characteristics of ABL-MOS with (f) different W_{JFET} and W_{BLO}. (g) The Miller capacitance of the ABL-MOS. (h) SC waveform for ABL-MOS with the W_{JFET} = 1.0 μm and W_{BLO} = 0.7 μm tested at V_{DD} = 800 V. (i) SC curve with different W_{JFET} and (j) W_{BLO}. (k) Output characteristic curves of Con-MOS and ABL-MOS at V_{GS} = 20 V obtained from simulations. (l) SC curves of Con-MOS and ABL-MOS at V_{GS} = 20 V and V_{DD} = 800 V obtained from simulations, the total t_{SC} = 4 μs. (m) The current density distribution and (n) temperature distribution of Con-MOS and ABL-MOS at W_{BLO} = 0.5 μm and 0.7 μm at t_{SC} = 4 μs. (o) $R_{on,sp}$ vs. t_{SC} of our ABL-MOS and state-of-the-art 1.2 kV plane and trench SiC MOSFET.

It can be seen that the ABL-MOS achieved the t_{SC} of 22 μs for the first time, effectively overcoming the limitation of poor SC robustness in SiC MOSFETs. Figures 1(i) and (j) summarize the impact of structural variations on SCWT. As W_{JFET} increases and W_{BLO} decreases, the shielding effect of the buried layer on the CSL weakens, leading to higher I_{SC} and a rise in temperature during the SC. However, these structural modifications do not significantly affect the $R_{on,sp}$, indicating that the ABL-MOS structure can enhance SC robustness without noticeably compromising the $R_{on,sp}$.

Figure 1(k) presents the simulated output characteristics of the conventional MOSFET (Con-MOS) and the ABL-MOS. The Con-MOS adopts the same epi but without secondary epi growth, and conventional implantation is used to form the Pwell and CSL. It can be observed that under low V_{DS}, the two devices exhibit nearly identical $R_{on,sp}$, whereas at high V_{DS} the current density of the ABL-MOS is reduced by 36%. As a consequence of this behavior, the simulated I_{SC} of the ABL-MOS at V_{DD} = 800 V is reduced by 75% compared with the Con-MOS, and the peak temperature is lowered by 21%, as shown in Figure 1(l). These changes are due to the longer and narrower current path induced by the buried layer.

Figures 1(m) and (n) show the current density and temperature distributions of the Con-MOS and ABL-MOS, respectively, at t_{SC} = 4 μs. At low V_{DS}, owing to the relatively high doping concentration of the CSL, the JFET resistances of the two devices are nearly identical, resulting in no significant difference in the overall device resistance. In contrast, at high V_{DS}, the depletion region expands significantly. In the ABL-MOS, the presence of the buried layer leads to a longer and narrower current path. When this path is compressed and narrowed by the expanding depletion region, the proportion of JFET resistance increases markedly. Consequently, under high V_{DS}, the resistance of the ABL-MOS increases, and the current density decreases, as illustrated in Figure 1(m). Therefore, at the same SC duration, the simulated maximum temperature of the ABL-MOS is significantly reduced to only 1240 K, demonstrating its superior SC robustness.

Figure 1(o) compares state-of-the-art SiC MOSFET in terms of $R_{on,sp}$ vs. t_{SC}. Based on previously reported results, trend lines were added to Figure 1(o) to separately describe the specialized devices, such as trench and deep-Pwell structures, and the Con-MOS that only differ in cell topology. In this work, although the ABL-MOS were not optimized for minimal $R_{on,sp}$ through buried layer design and CSL doping control, it can be seen that the fabricated devices achieve a significantly higher trade-off level between $R_{on,sp}$ and SCWT compared to current devices. The fabricated ABL-MOS achieves an SCWT exceeding 10 μs for the first time, reaching the current state-of-the-art level. These results demonstrate the great potential of the proposed structure for advancing SiC MOSFET technology and its applications in power electronics.

Conclusion. This work proposes and fabricates a novel ABL-MOS. Through an asymmetric design combined with a channeling-implantation buried layer, the device can achieve a high doping level in the CSL while maintaining a low oxide electric field. The narrow and elongated current path also helps reduce I_{SC} under high V_{DS} conditions, effectively suppressing SC power. The prepared device achieved a t_{SC} of up to 22 μs, marking the first time that a SiC MOSFET has reached and exceeded the SC robustness level of Si IGBT. This enables the device to meet the high-performance requirements of a wide range of power electronics applications. These characteristics highlight the great potential of the proposed structure for future power electronics development.

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References

1 Zhang M, Li H, Yang Z, et al. Short circuit protection of silicon carbide MOSFETs: challenges, methods, and prospects. IEEE Trans Power Electron, 2024, 39: 13081–13095
2 Chen Y, Li C, Wu Y, et al. Improved HF-FOM and SC ruggedness of split-gate 4H-SiC MOSFET with P^+ buffer. IEEE Electron Device Lett, 2024, 45: 1269–1272
3 Kim D, Sung W. Improved Short-circuit ruggedness for 1.2 kV 4H-SiC MOSFET using a deep P-well implemented by channeling implantation. IEEE Electron Device Lett, 2021, 42: 1822–1825
4 Kim D, deBoer S, Lynch J, et al. Enhancing 1.2 kV 4H-SiC MOSFET performance and ruggedness through deep P-well technology. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2024