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An optoelectronic memory device utilizing traps in insulator/insulator interface for weak-light detection and storage

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Abstract Owing to the multilevel storage and integrated sensing-storage capabilities enabled by the dual regulation of optical and electrical signals, optoelectronic memory devices have garnered growing attention. Weak-light performance is indispensable for achieving low-power consumption storage or high-performance detectors. However, the low light utilization efficiency of currently reported optoelectronic memory devices generally leads to high optical energy consumption. Herein, we report a novel indium-gallium-zinc-oxide (IGZO) thin-film transistor (TFT) integrated with a gallium oxide/aluminum oxide (Ga_2O_3/Al_2O_3) dual dielectric layer. Under irradiation with 254 nm ultraviolet (UV) light at 160 $\mu W{\cdot}cm^{-2}$, this device exhibits a substantial threshold voltage shift (ΔV_{th}) exceeding 30 V. Even with an irradiation time of only 20 ms, a 5 V storage window can still be attained. Notably, when the optical power density decreases to 0.8 $\mu W{\cdot}cm^{-2}$, the device maintains a 2 V response. Through performance analysis of samples with Ga_2O_3 layers of varying thicknesses, we attribute the excellent weak-light detection capability to the high interface trap density (1.38×10^{13} cm^{-2}) and sufficient thickness of the Ga_2O_3 layer. Our research demonstrates the potential of insulator-insulator interface traps in realizing an optoelectronic memory for weak-light detection and storage for the first time.

Keywords optoelectronic memory, insulator/insulator interface traps, weak-light, thin film transistor, gallium oxide

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1 Introduction

In the big data era, the escalating demand for high-capacity storage has spurred research on emerging multilevel memory devices [1–4]. As a hotspot in multi-bit non-volatile memory research, optoelectronic memory has been extensively studied over the past few years, primarily attracting attention due to its dual regulation of electrical and optical signals [5–8]. This unique characteristic endows it with the potential to achieve multi-state manipulation, i.e., higher storage capacity, and integration of photodetection and signal storage, which meets the multifunctional development needs of devices in the post Moore era [5, 8, 9].

Since optoelectronic memory is an emerging field, research efforts have predominantly focused on the realization of multilevel storage and the exploration of new device architectures, with little attention paid to the capability of weak-light detection and storage [10]. Nevertheless, this capability is indispensable for the subsequent reduction of energy consumption and improvement of detection sensitivity, especially given the rapid attenuation of the ultraviolet (UV) light in air. Currently reported devices typically suffer from low light utilization efficiency. For example, photochromic materials require light absorption to generate heat for chemical bond cleavage, light-assisted tunneling devices exhibit low carrier tunneling efficiency, and devices utilizing channel traps for charge storage possess poor light-harvesting efficiency [3, 11–17]. These limitations result in the required optical power density typically falling in the range of milliwatts per square centimeter ($mW{\cdot}cm^{-2}$) [18, 19].

Our group previously proposed the concept of realizing optoelectronic storage by utilizing a photosensitive dielectric layer and achieved excellent linear multilevel storage capability at 160 $\mu W{\cdot}cm^{-2}$ [2]. Though this work has realized a reduction in optical energy consumption, there remains substantial room for further exploration of the

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weak-light detection potential. Furthermore, drawing inspiration from commercial flash memory development—from polysilicon floating gates decades ago to SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) structures using nitride as charge traps—the performance of flash memory has been significantly enhanced, giving us a hint that charge traps in the dielectric layer may replace the floating gate in our previous design to simplify the device structure and reduce fabrication complexity and cost [2, 20, 21].

In this work, we utilize charge traps at the interface between gallium oxide (Ga_2O_3) and aluminum oxide (Al_2O_3) to demonstrate an indium-gallium-zinc-oxide (IGZO)-based thin-film transistor (TFT) optoelectronic memory device. The memory device exhibits outstanding memory performance, including a large threshold voltage shift ($\Delta V_{\rm th}$) exceeding 30 V under 160 $\mu W{\cdot}cm^{-2}$ irradiation for 2 s. In particular, under different weak-light conditions (20 ms of irradiation or an irradiance of 3.2 $\mu W{\cdot}cm^{-2}$), a $\Delta V_{\rm th}$ of over 5 V can be achieved. Notably, even at an optical power density of 0.8 $\mu W{\cdot}cm^{-2}$, the device maintains a $\Delta V_{\rm th}$ shift window of more than 2 V. Additionally, performance analysis of samples with different Ga_2O_3 thicknesses elucidates that the key to excellent weak-light detection and storage capability lies in the increasing thickness and the high density of interface trap states between the two dielectric layers. Our findings highlight the potential of utilizing interface traps between two dielectric layers for optimizing weak-light detection and storage performance, paving the way for further applied research.

2 Materials and method

The device fabrication process is as follows. First, molybdenum (Mo) was deposited on clean quartz substrates via radio frequency (RF) magnetron sputtering in a pure argon (Ar) atmosphere and patterned via the lift-off process to form source and drain electrodes. Both the channel length and width were set to 20 μm. Second, an IGZO thin film was deposited at 100°C with precisely controlled oxygen flux and then wet-etched using diluted hydrochloric acid (HCl) to form the channel layer. Third, a 60 nm Al_2O_3 layer was grown via atomic layer deposition (ALD) as the insulating dielectric layer. Fourth, under finely tuned oxygen flux, Ga_2O_3 of different thicknesses was deposited by RF magnetron sputtering for 0, 1, 2, and 3 h, yielding samples labeled Sample 1 (S1), Sample 2 (S2), Sample 3 (S3), and Sample 4 (S4) with Ga_2O_3 thicknesses of 0, 130, 257, and 378 nm, respectively. Finally, gold was deposited as the gate electrode via RF sputtering, and devices were patterned through a sequential combination of lithography and wet etching: gold etching solution for the gate electrode, and 60°C diluted tetramethylammonium hydroxide (TMAH) solution for Ga_2O_3 and Al_2O_3 to expose the source and drain electrodes. Samples were subsequently annealed on a hotplate at 200°C for 30 min in air to improve the Schottky contact of the gate electrode, after which they were ready for testing. Photoelectrical tests were performed using a Keithley 2636B source meter and a 254 nm deep ultraviolet (DUV) lamp equipped with a monochromator.

3 Results and discussion

Figures 1(a) and (b) show the schematic and optical microscopy images of the fabricated IGZO-based TFT optoelectronic memory with Ga_2O_3 as the photosensitive dielectric layer. IGZO is selected as the semiconductor channel layer due to its exceptionally high carrier mobility, enabling easy control with a high on/off ratio and low subthreshold swing (SS) [22, 23]. Additionally, its relatively low off-current enhances the sensitivity and detectivity of detectors based on this structure [24]. Mo is one of the optimal source and drain electrode materials due to its low contact resistance with IGZO [25]. In contrast, the gate electrode requires a high-work-function material to form a good Schottky barrier with Ga_2O_3, reducing leakage current and the likelihood of charge detrapping. Prior to the formal tests, we conducted hysteresis tests of transfer curves on four samples in a dark environment, as shown in Figure A1 in Appendix A. It was found that none of the samples exhibited hysteresis characteristics, indicating that the devices themselves do not induce shifts under bias stress, thus ensuring the accuracy of optical information. Transfer characteristic curves of all samples under 1 V drain voltage ($V_{\rm DS}$) in different states are shown in Figures 1(c)–(f). In this article, we uniformly set the threshold voltage ($V_{\rm th}$) to the gate voltage ($V_{\rm GS}$) corresponding to a drain current ($I_{\rm DS}$) of 1 nA. The initial threshold voltage (black line) of all samples is generally around 0 V. The write (blue line)/erase (red line) state is the state after irradiation with a 254 nm light pulse for 2 s at a $V_{\rm GS}$ of 8 V/−8 V. Since no Ga_2O_3 was deposited on Al_2O_3 for S1, the transfer curves of S1 in the three states are almost completely overlapped, indicating no memory effect which directly eliminates the possibility of trap storage caused by 254 nm irradiation in the Al_2O_3 dielectric layer, Al_2O_3/IGZO interface, and IGZO channel. For S2, S3, and S4, obvious memory windows defined by the difference of $V_{\rm th}$ in written and erased states have appeared, directly proving that stable storage can also be achieved without floating gate layers. Especially, as the thickness of Ga_2O_3 increases, S4 achieves a super large memory window of 31 V, which means that the device's

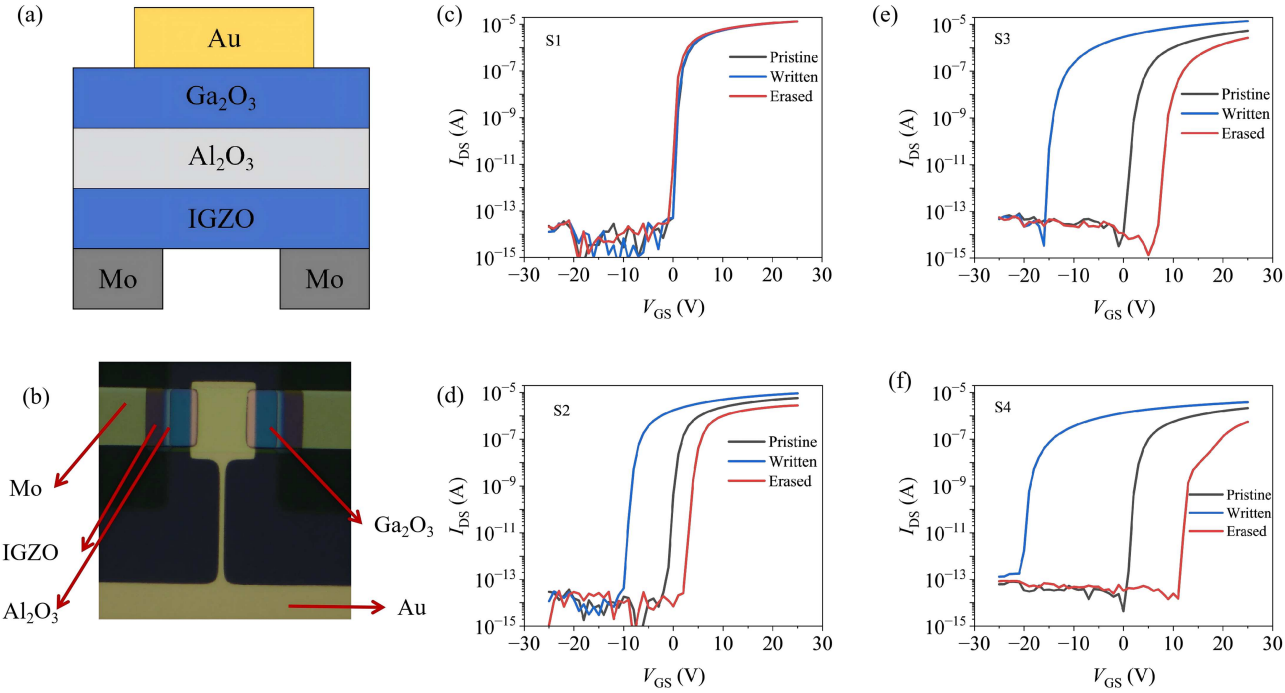

Figure 1 (Color online) Structures and transfer characteristic curves of the optoelectronic memory devices with different thicknesses of Ga_2O_3. (a) Schematic illustration of the optoelectronic memory device. (b) Optical microscopy image of the optoelectronic memory device. (c)–(f) The transfer curves under $V_{DS} = 1$ V for S1, S2, S3, S4. The black line, blue line, and red line represent the initial state, written state, and erased state, respectively. Both writing and erasing operations involve a 254 nm light pulse with a light intensity of 160 μW·cm^{-2} and a duration of 2 s. The difference is that V_{GS} of 8 V is applied during writing operation, while V_{GS} of −8 V is applied during erasing operation.

information storage will have strong anti-interference ability. Moreover, we can foresee that S4 will have excellent weak light detection and storage capabilities, as detailed in the subsequent data.

Because of the absence of the photosensitive layer-Ga_2O_3, S1 hardly responds to 254 nm UV, so further discussions on weak-light detection and storage do not include it. Figures 2(a)–(c) show the responses of the other three samples to weak 254 nm UV (power density = 0.8 μW·cm^{-2}) at a gate bias of −8 V. All three samples were first subjected to a writing operation to fill the hole traps, resulting in an initial V_{th} from −10 to −20 V for each. Compared with the negligible storage window of S2 and S3, S4 still has a response of approximately 2 V. We believe the thickness of Ga_2O_3 is a crucial factor in weak-light detection because sufficient thickness enables more efficient photon absorption. High-energy photons are less likely to be fully captured if the absorber is not thick enough, especially when the number of photons is small. Next, we compare the response speeds of the three samples, as shown in Figures 2(d)–(f). Under 20 ms short pulse irradiation, S2, S3, and S4 formed response windows of 1.3, 3, and 4.3 V, respectively. All three samples show a wide shift of V_{th} enough to distinguish between the "0" state and the "1" state. Besides, Figure A2 better illustrates the dynamic response of writing and erasing operations of S4. According to this, the optical writing and erasing speed can be seen as 20 ms. However, due to the modulation speed of the electrical switch in the test, we did not conduct tests with shorter pulses, but we can predict that the real response speed of S4 is much less than 20 ms.

Then, we conducted the stability tests for S4. Figure 3(a) presents the retention characteristics of device S4 over 10000 s under dark conditions without external stimuli, except for intermittent read operations. The current of the "1" state exhibits a slight decay during the 10000 s retention period, suggesting that the injected charges are stably trapped within the trap states. In contrast, the "0" state current shows relatively pronounced fluctuations, which arise from its ultra-low magnitude close to the detection limit of the measurement system, rendering it vulnerable to noise interference. Despite such fluctuations, the "0" state current remains below 0.1 pA even after 10000 s, and the two resistance states maintain excellent distinguishability. Linear fitting was conducted on the current values of both states to extrapolate the long-term retention performance. The memory window after ten years is estimated to retain 84% of its initial value, verifying the superior retention characteristics of the device for both data-storage states. These results guarantee reliable data accuracy and highlight the promising potential of the device for multi-level data storage applications. Figure 3(b) shows the "0" and "1" state currents (corresponding to I_{DS} at a fixed readout $V_{GS} = -6$ V) over 100 consecutive writing and erasing cycles. Under 100 fatigue tests, both

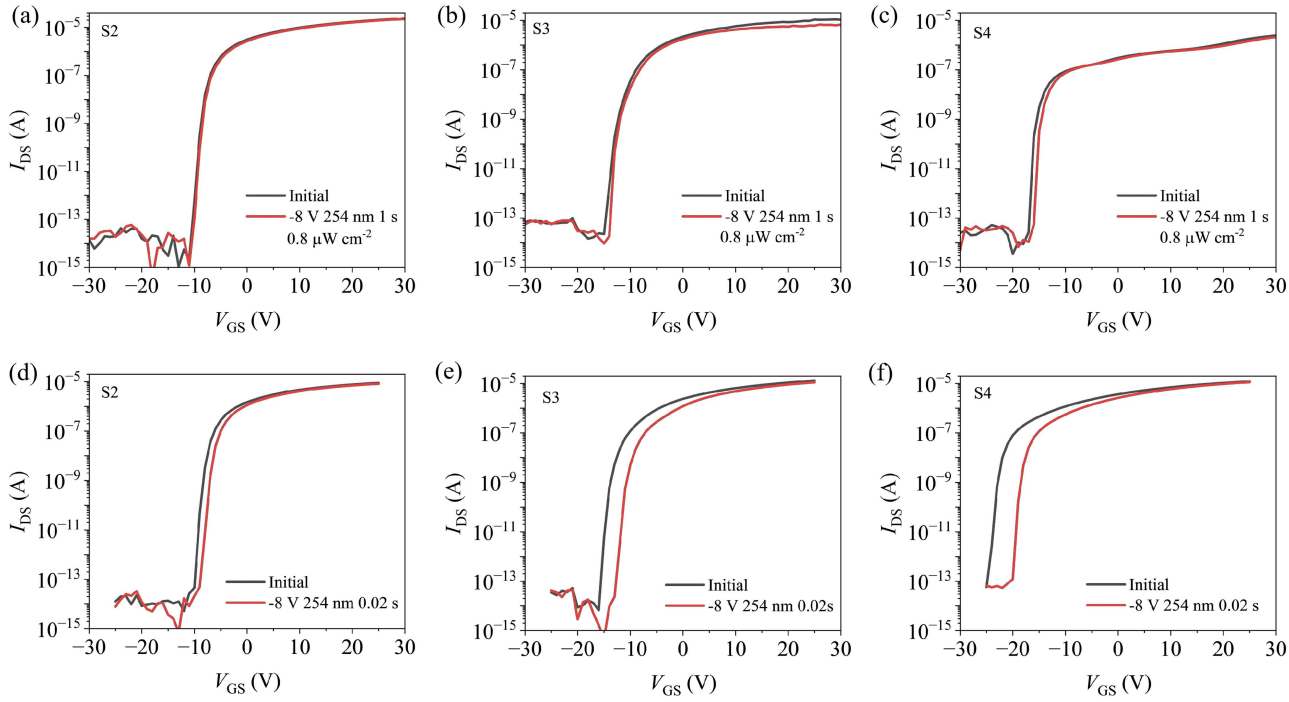

Figure 2 (Color online) Transfer characteristic curves of S2, S3, and S4 under two different weak light conditions. (a)–(c) Transfer characteristic curves of S2, S3, and S4 in the initial state and after 1 s irradiation of 254 nm UV whose power density is 0.8 μW·cm^{-2} at a gate bias of −8 V. (d)–(f) Transfer characteristic curves of S2, S3, and S4 in the initial state and after 0.02 s irradiation of 254 nm UV whose power density is 160 μW·cm^{-2} at a gate bias of −8 V.

state "0" and state "1" maintained stable currents. The slight upward shift of the "1" state should be attributed to the weak persistent photoconductivity effect of IGZO, which can be solved by using other channel materials, but it does not affect the differentiation of states at all.

To investigate the solar-blind photoresponse selectivity, UV-Vis absorption measurements were carried out on the as-fabricated Ga_2O_3 thin film, and the photoresponse characteristics of device S4 were examined under illumination at various wavelengths ranging from 400 to 800 nm. As shown in Figure 3(c), the Ga_2O_3 film exhibits strong absorption in the wavelength region of 200–270 nm. Using the Tauc plot method, the optical bandgap of the Ga_2O_3 thin film is determined to be approximately 5.0 eV. Specifically, the absorptance of 254 nm light is 40%, which is converted to an absorption coefficient of 6.4×10^4 cm^{-1}. Therefore, the absorption of 254 nm by S2, S3, and S4 is 56.5%, 80.7%, and 91.1%, respectively. As illustrated in Figure 3(d), S4 shows negligible response to writing and erasing operations under visible-light illumination at 405, 450, 532, and 650 nm, as evidenced by the absence of obvious shifts in the transfer curves. These results collectively verify the outstanding solar-blind selectivity of S4.

In theory, utilizing deep traps in the dielectric layer for storage will have better storage characteristics than metal floating gate structures. Furthermore, we tested the response characteristics of S4 under different light intensities. Figures 4(a)–(h) show the transfer characteristics of S4 under the same test conditions except for the UV power density, which was varied from 0.8 to 100 μW·cm^{-2}. Higher power densities induce larger shift windows, as shown in Figure 4(i) with an exponential fitting curve that coincides with the resistor-capacitor (RC) series model proposed in our previous work [2,10]. Furthermore, the results indicate that each power density corresponds to a unique $V_{\rm th}$ state, enabling power intensity-programmable multibit storage and intensity calibration.

Figure 5(a) presents a comparison of optical power density and operation time between S4 and other optoelectronic memory devices [2, 12, 16–18, 26–31]. It is evident that our device has greatly improved its weak light capability, partly due to the structural design of the photosensitive dielectric layer, which enhances the storage utilization efficiency of photogenerated carriers, and partly due to the increased thickness of Ga_2O_3. The excellent weak-light capability not only greatly reduces the light energy consumption of our device in memory applications, which is very important in the era of big data, but also greatly improves the detectivity in the field of ultraviolet detection, which is extremely important for weak-signal solar blind light due to severe environmental extinction effects.

The S2–S4 data above all demonstrate good storage performance even in the absence of metal floating gates, while the S1 data exclude trap storage in IGZO, the IGZO/Al_2O_3 interface, and Al_2O_3. Therefore, charges can only be stored in Ga_2O_3 bulk traps or Al_2O_3/Ga_2O_3 interface traps. To simplify the analysis of storage locations,

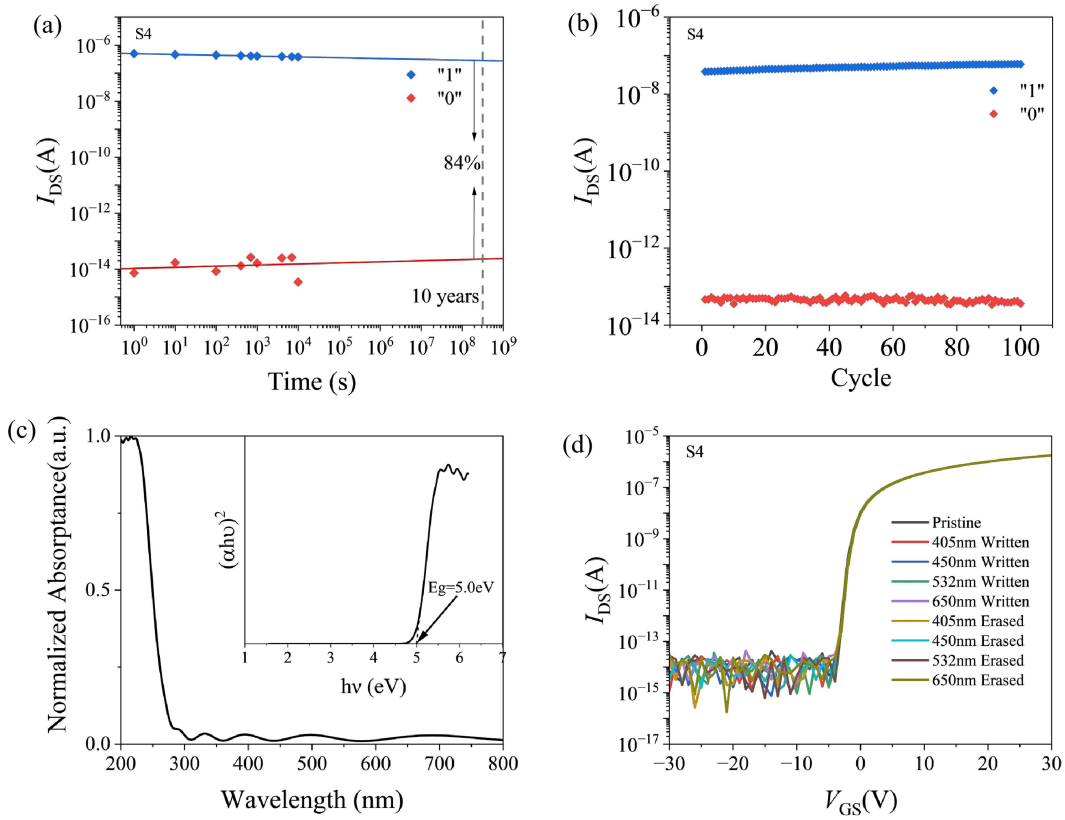

Figure 3 (Color online) Reliability and solar-blind selectivity characterization of S4. (a) Retention tests of S4. Storage current in the "0" state and "1" state for 10000 s and linear fitting of both states. (b) Fatigue tests of S4. Storage current in the "0" state and the "1" state as a function of consecutive writing and erasing operation cycles of S4 (V_{DS} = 1 V, optical pulse: 254 nm, 160 μW·cm^{-2}, 2 s; V_{GS} pulse: −8 V/8 V). The readout gate voltage was set to −6 V. (c) UV-Vis absorption spectrum, and the inset is an estimation of the optical bandgap through a Tauc plot. (d) Transfer curves of S4 after writing and erasing operation with varying wavelength (V_{DS} = 1 V, optical pulse: 405, 450, 532, 650 nm, 160 μW·cm^{-2}, 2 s; V_{GS} pulse: −8 V/8 V).

we consider two extreme scenarios: charges are either fully stored in the interface traps between Ga_2O_3 and Al_2O_3 or fully stored uniformly in the bulk traps of Ga_2O_3. For these two situations, according to Gauss's law, the relationship between the stored charge density σ_{int}/ρ_{bulk} and ΔV_{th} can be expressed as

$$\Delta V_{th} = \frac{\sigma_{int}}{C_{GO}} = \sigma_{int}\frac{d_{GO}}{\epsilon_0\epsilon_{GO}}, \tag{1}$$

$$\Delta V_{th} = \frac{\rho_{bulk}d_{GO}}{2C_{GO}} = \rho_{bulk}\frac{(d_{GO})^2}{2\epsilon_0\epsilon_{GO}}, \tag{2}$$

respectively [32, 33], where d_{GO} is the thickness of the Ga_2O_3 layer, ϵ_0 and ϵ_{GO} are the vacuum permittivity and relative permittivity of Ga_2O_3, which are both constants, and σ_{int} and ρ_{bulk} are the surface charge density and volume charge density, respectively.

Based on the above data, we find that hole traps play a dominant role because the V_{th} mainly shifts in the negative direction. Next, we mainly analyze the location of hole traps. In order to completely fill the hole traps, multiple erasing and writing operations were performed on each sample with a large gate voltage (20 V) and light pulses with a wide width (20 s), until V_{th} of the final transfer curve no longer exhibited any shift. Figures 5(b)–(d) present the data corresponding to the last transfer curves after saturated operations. The extracted ΔV_{th} values, which are mainly induced by hole traps, are 23.77, 50.58, and 74.31 V for S2, S3, and S4, respectively. According to (1), if all charges are stored in the interface traps, σ_{int} would be constant, as there are no available trap states for excess photogenerated holes. Thus, ΔV_{th} is proportional to the thickness of Ga_2O_3. However, according to (2), if charges are entirely stored in the bulk of Ga_2O_3, ρ_{bulk} is still a constant, but ΔV_{th} increases with the square of the thickness of the Ga_2O_3 layer ideally. This is because a thicker layer provides more trap states and enables absorption of more photons, resulting in more photogenerated holes being captured. The ratio of ΔV_{th} for S2, S3, and S4 is 1:2.13:3.13, which is close to the thickness ratio of Ga_2O_3 for S2, S3, and S4 (1:1.98:2.91). The influence

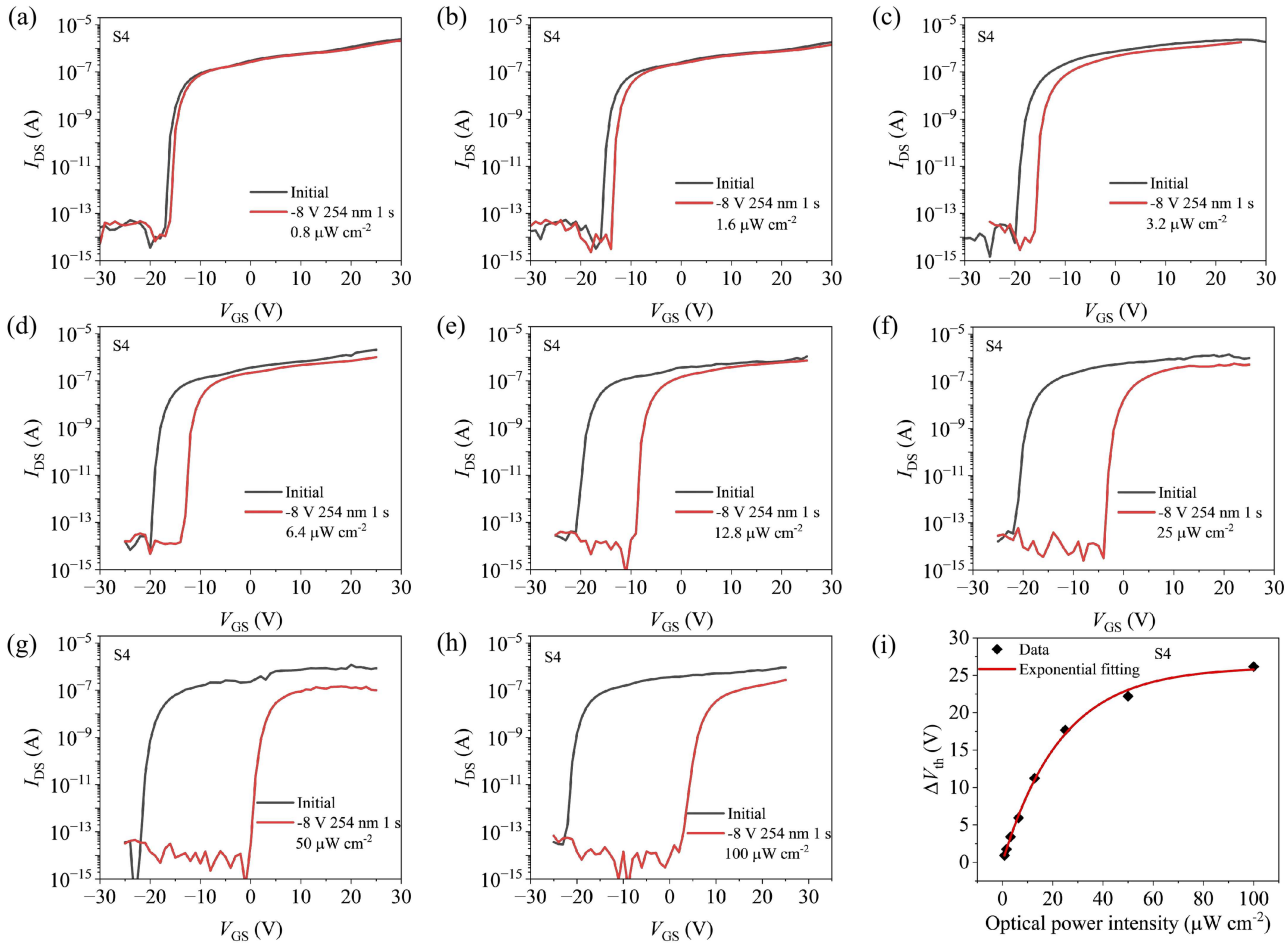

Figure 4 (Color online) Transfer characteristic curves of S4 after irradiation of different power densities. (a)–(h) Transfer characteristic curves of S4 in the initial state and after 1s irradiation of 254 nm UV whose power density increases from 0.8 to 100 μW·cm^{-2} at a gate bias of −8 V. (i) Exponential fitting of $\Delta V_{\rm th}$ for different states formed by different power intensities.

of electron traps cannot be avoided in the test, and they are presumed to contribute partially to $\Delta V_{\rm th}$. Therefore, the actual $\Delta V_{\rm th}$ contributed by hole traps is smaller than the extracted result, and its ratio would be even closer to the thickness ratio, showing better consistency with (1). On this basis, we can infer that the hole traps are located at the interface or at least distributed near the interface. The density of interface trap states can be calculated as approximately 1.38×10^{13} cm^{-2}. This thickness-dependent method accurately clarifies the location of traps; however, the detailed density-of-states distribution and energy levels of interface traps require further in-depth investigation.

Finally, the operating mechanism of the optoelectronic storage process is schematically illustrated in Figure 6. Based on our previous work, Figure 6(a) shows the band alignment of the materials before contact [10, 34]. Figure 6(b) specifically illustrates the schematic diagrams of the energy bands and trap states during the writing/erasing operation and retention phases. During the writing operation, the device is subjected to 254 nm UV irradiation; the interface traps capture photogenerated holes, while excess photoexcited electrons are driven by the electric field induced by a positive gate bias and flow into the gate electrode. In the retention phase, the charges stored in the interface traps maintain a continuous positive bias to the channel. Without environmental irradiation, the device exhibits good stability due to the deep trap energy. When a readout voltage is applied to retrieve the current state, the device remains stable and reliable because the low gate voltage barely causes holes to escape from the interface traps, resulting in a positive shift in $V_{\rm th}$ and a "1" state under an appropriate readout voltage. Conversely, during the erasing operation, photogenerated electrons neutralize with the holes in the interface traps, and the excess photogenerated holes are recombined with the electrons flowing from the gate electrode, driven by the electric field induced by a negative gate bias. This reversal leads to a negative shift in $V_{\rm th}$ and a "0" state.

Obviously, the interface traps in Ga_2O_3/Al_2O_3 play a critical role in this device. In future work, we can further improve performance through interface engineering. Regarding long-term stability, in accordance with the Shockley-

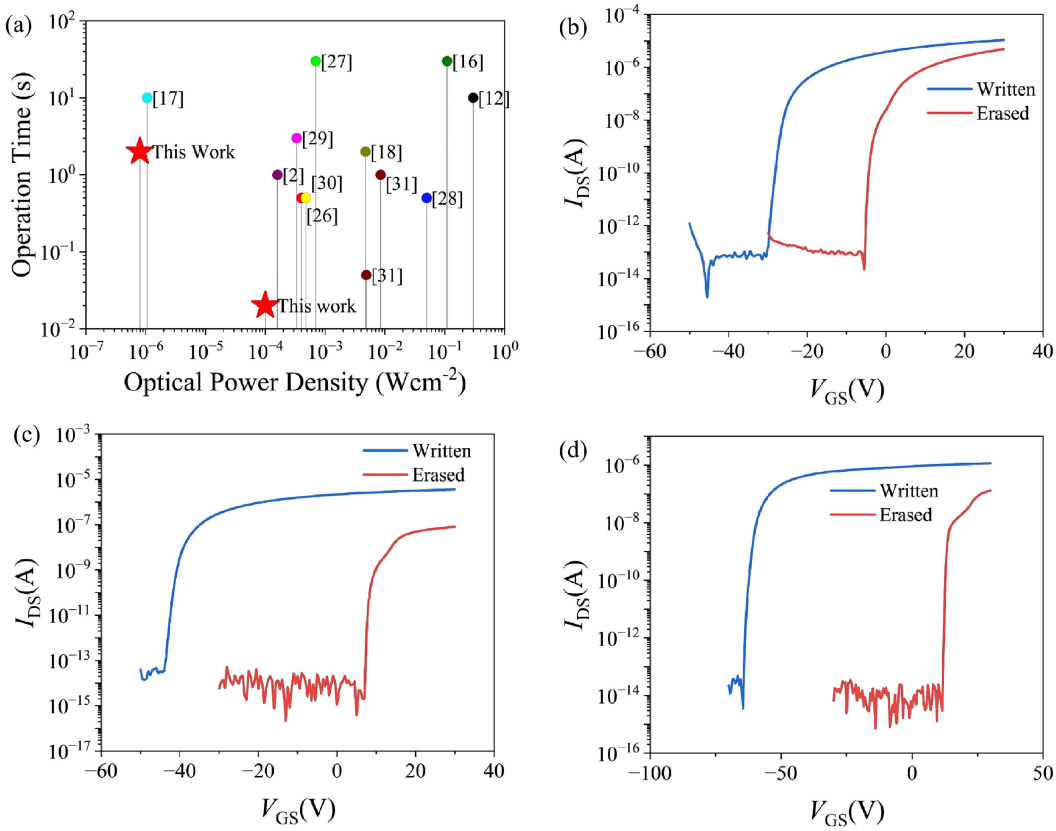

Figure 5 (Color online) Saturation test results of S2, S3, and S4. (a) Comparison of operation time (irradiation time) and optical power density between the S4 device and other reported optoelectronic memory devices. (b)–(d) Transfer curves of S2, S3, and S4, respectively, after saturation erasing (performed first) and saturation writing (performed subsequently) (V_{DS} = 1 V, optical pulse: 254 nm, 160 μW·cm^{-2}, 20 s; V_{GS} pulse: −20 V/20 V).

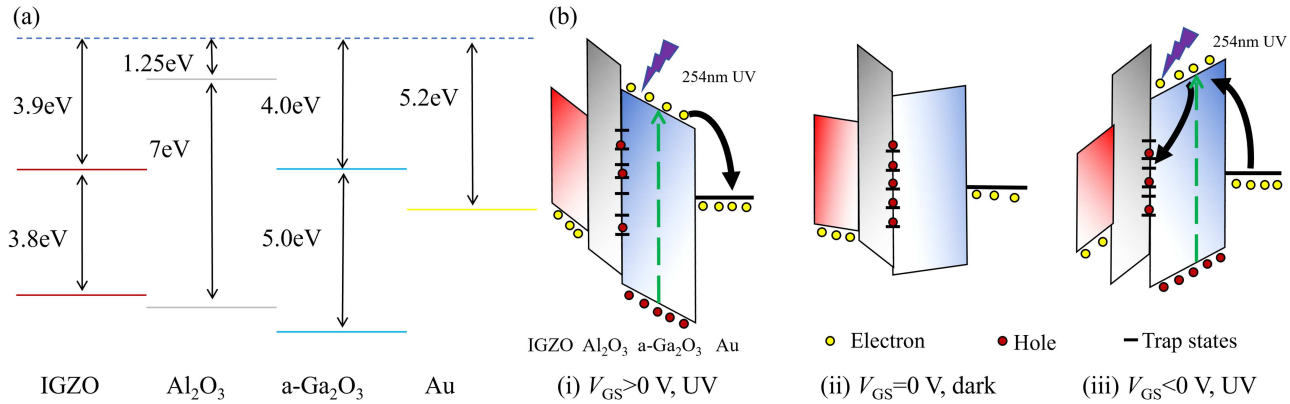

Figure 6 (Color online) Schematic illustration of the writing and erasing mechanism of the energy band diagram. (a) Energy band alignment of four materials before contact. (b) (i) Writing operation; (ii) retention phase; (iii) erasing operation.

Read-Hall (SRH) theory, the emission rate of carriers trapped by trap states is strongly dependent on the depth of the trap energy level, which can be mathematically expressed as

$$e \propto \sigma \exp\left(-\frac{\Delta E}{k_B T}\right), \tag{3}$$

where e denotes the emission rate, σ represents the capture cross-section of traps, and ΔE is the energy difference between the trap level and the relevant band edge [35]. An excessively shallow trap energy level will lead to a high charge emission rate, which causes a short storage retention time. To increase storage stability, we can increase the ratio of deep traps to shallow traps.

4 Conclusion

In summary, a novel and feasible optoelectronic memory based on an IGZO-TFT is proposed and demonstrated, utilizing interface hole traps in the dual dielectric layer for the trapping and detrapping of photogenerated holes. The device performs well in weak-light detection and storage, showing a large ΔV_{th} even at a low 254 nm UV output power density of 0.8 $\mu W{\cdot}cm^{-2}$ and a short irradiation time of 20 ms. The excellent weak-light capability is due to a high insulator/insulator interface trap concentration (1.38×10^{13} cm^{-2}) and a thick light absorption length. The results of this work provide a promising direction for the low-energy development and high-sensitivity detection of optoelectronic memory in the future.

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Appendix A

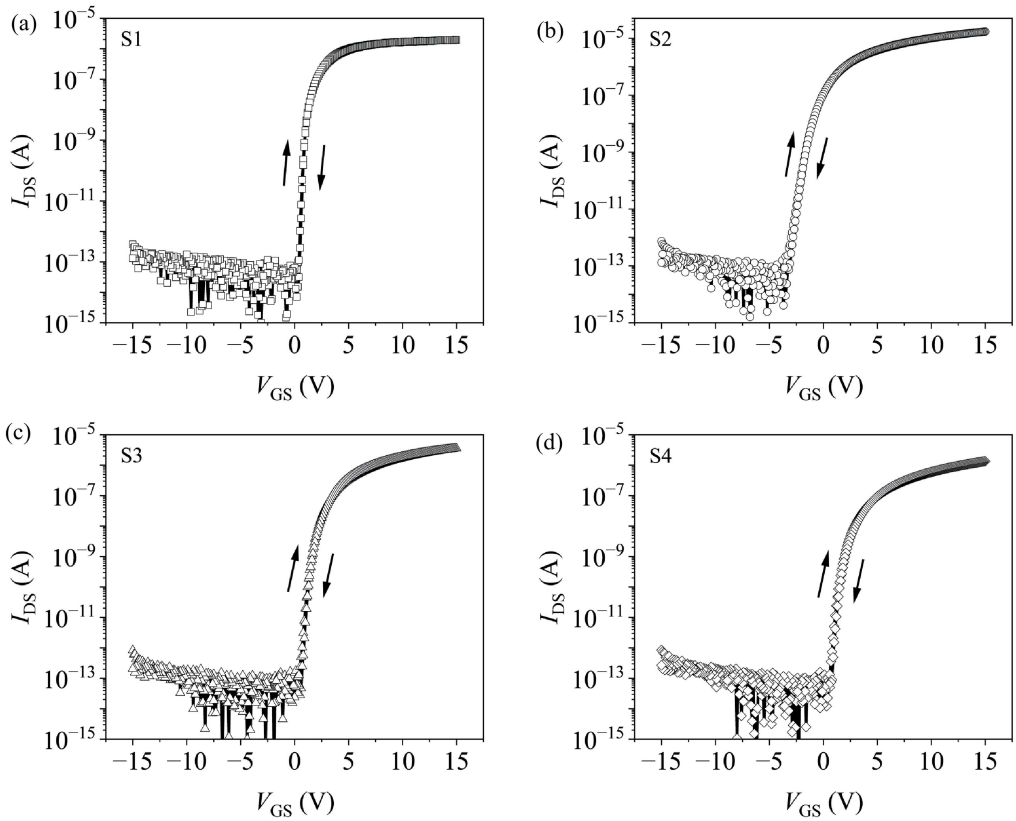

Figure A1 Cyclic sweep of transfer characteristic curves of four samples. (a)–(d) Transfer curves obtained by cyclic sweeps for S1, S2, S3, and S4, respectively, in the dark.

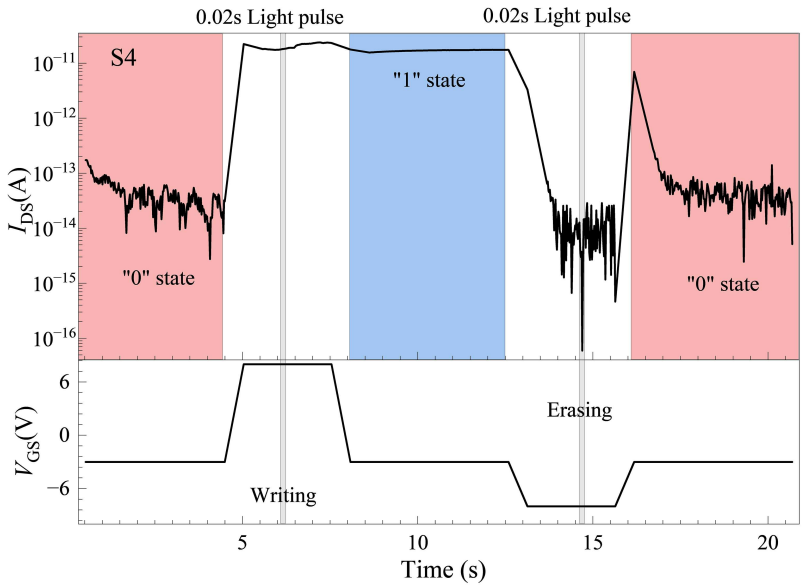

Figure A2 (Color online) The single writing/erasing operations and corresponding results (V_{DS} = 1 V, optical pulse: 254 nm, 70 μW·cm^{-2}, 0.02 s; V_{GS} pulse: −8 V/8 V). The readout voltage was set to −3 V.