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# All-SiC integrated process platform: development roadmap and challenges

Jie MA[1], Yawen XU[1], Mengyao ZHAO[1], Yong GU[1], Jiaxing WEI[1], Yu HUANG[2], Runhua HUANG[2], Song BAI[2], Long ZHANG[1*], Siyang LIU[1*] & Weifeng SUN[1*]

[1]*National ASIC System Engineering Research Center, School of Integrated Circuits, Southeast University, Nanjing 210096, China*
[2]*Nanjing Electronic Device Institute, Nanjing 100048, China*

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**Abstract** With exceptional high-temperature tolerance and radiation hardness, Silicon carbide (SiC) integrated circuits (ICs) have emerged as a promising candidate for extreme-environment applications in automotive, aerospace and deep-well drilling. This paper provides a comprehensive review of monolithic SiC IC platforms, encompassing a low-voltage (LV) IC platform incorporating exclusively LV devices and a power IC platform featuring concurrent integration of high-voltage (HV) and LV devices. Fundamental components evolve from bipolar junction transistors (BJTs) to junction field-effect transistors (JFETs), and subsequently to metal-oxide-semiconductor field-effect transistors (MOSFETs). A systematic review is conducted on the state-of-the-art and key technical hurdles for each device platform, with a focus on high-temperature and radiation-hardened applications. Finally, critical challenges confronting MOSFET-based integration process platforms are delineated, namely threshold voltage ($V_{\rm th}$) mismatch between NMOS and PMOS devices and radiation reliability issues, necessitating focused research initiatives to propel the industrialization of SiC monolithic ICs.

**Keywords** SiC, integration, monolithic, process platform, IC, BJT, JFET, MOSFET, threshold voltage, radiation reliability

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## 1 Introduction

Silicon carbide (SiC) demonstrates superior material properties compared to silicon (Si), featuring a 3× wider bandgap and 10× higher critical breakdown electric field. This enhanced stability originates from the strong covalent bonding between C and Si atoms, which effectively suppresses electron transitions under extreme thermal and radiation conditions [1]. These intrinsic characteristics establish SiC as an ideal semiconductor material for high-power, high-temperature and radiation applications.

Conventional Si-based power integrated circuits (ICs) face operational limitations with maximum operation temperature typically below 150°C and radiation tolerance generally under 100 krad [2, 3]. Even silicon-on-insulator (SOI) power ICs, while exhibiting improved performance, are constrained to approximately 200°C operational temperatures and 500 krad [2] irradiation resistance [4]. Compared to conventional Si-based ICs, SiC ICs can theoretically demonstrate superior performance characteristics, including high operational temperature over 800°C and high radiation hardness over 100 Mrad [5, 6]. In addition, SiC power ICs enable significant reductions in system volume and power losses while improving overall energy conversion efficiency. Currently, the monolithic integration of SiC high-voltage (HV) power devices and low-voltage (LV) circuits has become a critical research focus.

To clarify the scope of this review, we briefly position SiC-based monolithic integration against GaN-based integration platforms. In mainstream power electronics, SiC and GaN generally address complementary application envelopes: SiC is often favored for high-voltage and harsh-environment operation, whereas GaN is widely adopted for high-frequency, medium-voltage conversion where switching speed and power density dominate system-level benefits [7–12]. At the integration-technology level, SiC platforms are primarily constrained by MOS interface/oxide-related manufacturability and threshold-voltage stability, while GaN platforms are strongly influenced by normally-off implementations, trapping-induced dynamic effects, and gate-stack reliability [8–11]. Besides, GaN-based ICs also face severe substrate bias effect (also called the back-gating effect), deteriorating performance under certain conditions [13]. A qualitative comparison is provided in Table 1.

* Corresponding author (email: longzh@seu.edu.cn, liusy2017@seu.edu.cn, swffrog@seu.edu.cn)

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**Table 1** Qualitative comparison between SiC- and GaN-based integration platforms.

| Aspect | SiC-based integration platforms | GaN-based integration platforms |
|---|---|---|
| Fabrication complexity | Interface bottlenecks: $SiO_2$/SiC interface ($D_{it}$), $V_{th}$ stability, and CMOS/BCD feasibility (especially p-channel devices) [10, 11] | Device/stack and trapping bottlenecks: normally-off realization, trap-induced dynamics (e.g., dynamic $R_{on}$), and gate-stack reliability [8, 9] |
| Cost | Substrate/epitaxy quality, yield learning, and process step count (deep isolation/HV termination can increase complexity) [7] | Often leveraging GaN-on-Si with cost/scale benefits tied to wafer size and manufacturing ecosystem; yield/reliability screening and thermal management remain key cost factors [8, 12] |
| Typical application | Harsh-environment electronics and high-voltage power/control co-integration [7, 12] | High-frequency, medium-voltage power conversion and high power-density applications [8, 12] |
| Reliability focus | Key concerns include oxide/interface-related $V_{th}$ drift and long-term MOS reliability [10, 11] | Key concerns include trapping-related transient behavior, dynamic $R_{on}$, and gate reliability under switching stress [9] |

This paper systematically reviews the technological developments in SiC ICs and summarizes their advantages and limitations. Section 2 examines the current state of the LV IC platform integrating LV devices exclusively. A comprehensive discussion is provided on the technical obstacles in different device technologies, with a focus on the performance of SiC ICs in their advantageous areas, i.e., radiation-rich and high-temperature environments. Section 3 then details the power IC platform that co-integrates both HV and LV devices. Section 4 further explores key challenges in the development of SiC MOSFET-based integrated circuits, primarily addressing issues of CMOS's threshold voltage ($V_{th}$) matching and radiation reliability issues.

## 2 LV IC platform

Among the numerous polytypes of SiC, 6H-SiC and 4H-SiC are the two most commercially successful in industrial applications. Early SiC LV IC platforms, particularly the earliest-developed JFET-based ones, utilized 6H-SiC substrates primarily because 6H-SiC achieved relatively mature processing techniques first in the late 20th century following CREE's (now Wolfspeed) pioneering production of 1-inch 6H-SiC wafers in 1991 [14–17]. Since the early 21st century, 4H-SiC (hereafter referred to simply as SiC) has become the dominant material for IC fabrication due to its enhanced carrier mobility with reduced anisotropy and lower dopant ionization energy [17, 18].

Similar to Si technology, SiC LV ICs are also based on three fundamental device types: bipolar junction transistors (BJTs), junction field-effect transistors (JFETs), and metal-oxide-semiconductor field-effect transistors (MOSFETs). This section will sequentially present the historical development of SiC LV IC platforms based on these three device types. It will also provide a critical examination of their high-temperature and radiation reliability, as well as the driving forces behind the technological iterations between different device architectures.

### 2.1 BJT-based SiC IC platform

#### 2.1.1 *Historical development*

The first monolithic SiC IC based on BJT was demonstrated by Purdue University in 2008 [19]. The BJT employs an N+/P/N-/N+ epitaxial stack grown on a P+ substrate, leveraging the superior minority carrier lifetime in epitaxial layers compared to implantation regions. Notably, the P+ implantation shown in Figure 1 is confined to the localized base-contact region for forming acceptable ohmic contacts, while the primary base transport region is provided by the epitaxial P layer, thereby avoiding the impact of implantation-induced defects on the base transport region. The vertical emitter-base-collector (E/B/C) structure, shown in Figure 1, is patterned using reactive ion etching (RIE) for precise dimensional control. To minimize etch-induced surface recombination, the base contact is strategically positioned 4 μm from the emitter edge. Besides, surface passivation involving wet oxide growth followed by NO ambient annealing (1175°C, 2 h) is adopted to optimize interface quality. Ohmic contacts are implemented with 70 nm Ni for N-type emitter/collector and 33 nm Ti/167 nm Al stack for P-type base.

The BJTs implemented in this platform demonstrate a peak current gain ($\beta$) of 22, with performance primarily constrained by surface passivation quality. This critical process step governs interface state density ($D_{it}$) reduction and consequently suppresses surface recombination velocity [20]. Despite this limitation, the integrated transistor-transistor logic (TTL) inverters exhibit robust digital performance: achieving a high-level noise margin (NMH) of 1.5 V, a low-level noise margin (NML) of 3.9 V and a propagation delay ($t_{pd}$) of 108 ns at fan-out = 10. In their 2011 work [21], the P+ substrate is replaced with a semi-insulating substrate to minimize collector-substrate capacitance and enhance switching performance, resulting in a reduced $t_{pd}$ of 9.8 ns.

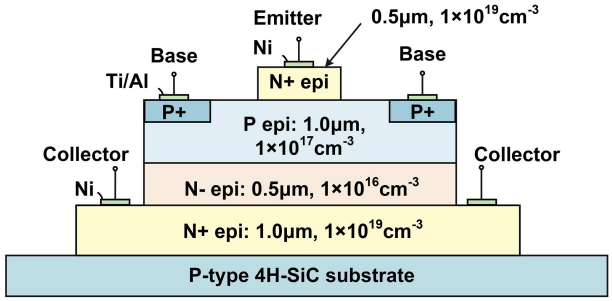


**Figure 1** (Color online) Cross-sectional view of the BJT used in Purdue's work utilizing P-type substrate [19].

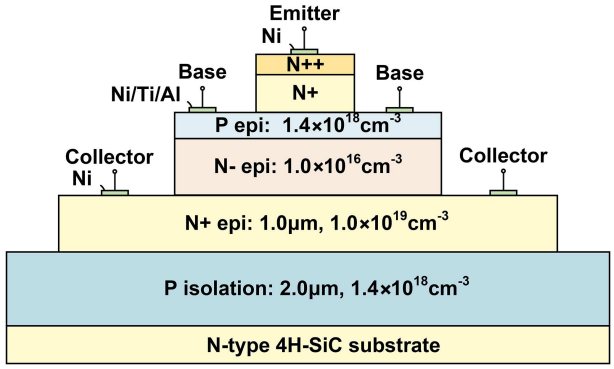


**Figure 2** (Color online) Cross-sectional view of fabricated n-p-n transistor [22].

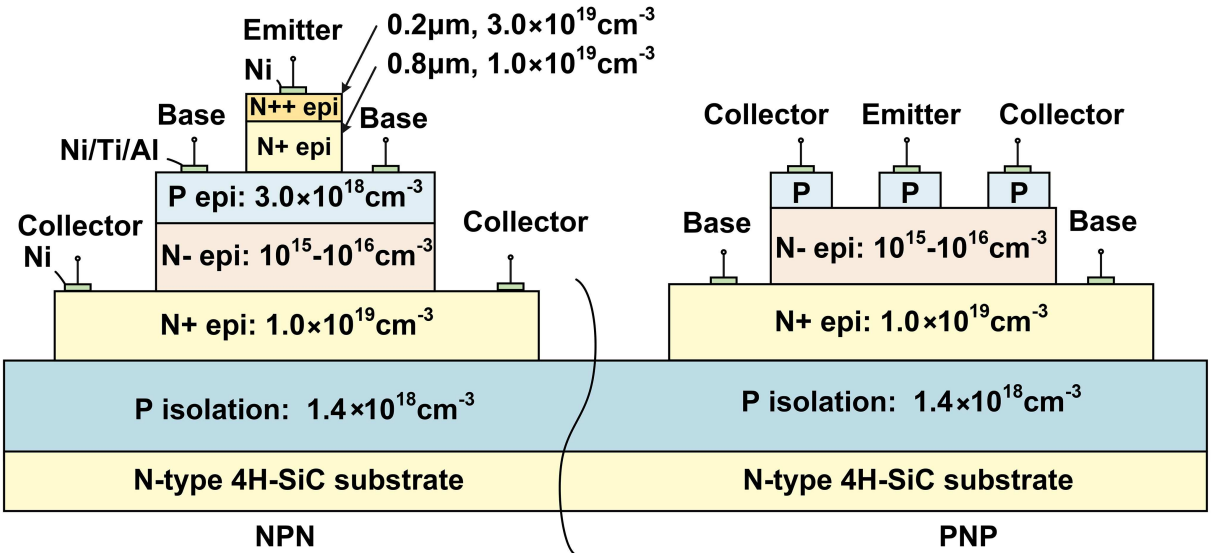


**Figure 3** (Color online) Cross-sectional view of vertical NPN and lateral PNP transistors fabricated in the same IC technology [25].

P-type and semi-insulating SiC substrates have many defects due to the immature technology. Therefore, wafers with N-type substrates are widely used. However, this also brings about the problem of difficult isolation between devices. As shown in Figure 2, Zetterling's group from KTH Royal Institute of Technology adopted N-type substrates with epitaxial P-isolation layers to achieve effective device isolation [22]. Furthermore, they investigated surface passivation effects on 4H-SiC BJT performance and then proposed an optimized process [20]. Their methodology employed 50-nm plasma-enhanced chemical vapor deposition (PECVD) $SiO_2$ followed by $N_2O$ annealing (1150°C, 3 h) to minimize interface states, and the BJT obtains a high $\beta$ of 45. The two-input OR/NOR gate fabricated based on this BJT achieves a stable noise margin of 1 V in the temperature range of 27°C to 300°C

Extra Ti and TiW layers are adopted in the interconnect stack to enhance the step coverage as well as the adhesion between Al and $SiO_2$ in their further work [23, 24]. Such a metallization system demonstrates stable high-temperature reliability under electromigration testing [23] and has extended the upper limit of BJT ICs from 300°C to 500°C while maintaining the 1 V stable noise margin benchmark [24].

In 2014, Zetterling's group introduced a complementary SiC bipolar technology enabling monolithic integration of vertical NPN and lateral PNP transistors (Figure 3) [25]. The fabrication of lateral PNP devices requires only one additional mask and a dry-etching step, where the emitter and collector are formed within the P-type base region of the NPN transistor, followed by isolation etching. The PNP base is implemented using the lightly doped NPN collector layer. However, despite successful single-chip co-integration, the PNP transistors in this platform have not yet been incorporated into functional analog circuits.

The collective research on SiC BJT technology has culminated in the development of the High-Temperature Power Electronic Systems with SiC Integrated Circuits (HOTSiC) platform [26], pioneered by Zetterling's group

at KTH. This platform employs advanced multi-layer epitaxial growth and mesa-etching techniques. Utilizing this technology, various circuit components have been successfully demonstrated and characterized at temperatures exceeding 300°C, including OR-NOR gate [22–24], operational amplifier [27], digital-to-analog converter (DAC) [28], analog-to-digital converter (ADC) [29], ring oscillator [30], gate driver [31], signal conditioning block [32].

#### 2.1.2 *High temperature reliability*

As previously discussed, the current maximum operating temperature for BJT integrated circuits is 500°C, primarily limited by the metal interconnection system—especially the challenges associated with step coverage of metal layers due to the mesa structure [24]. The variations of the two key electrical parameters of BJTs, current gain and on-resistance, with increasing temperature are summarized as follows.

The current gain of BJTs initially decreases (−40°C to 300°C) and then increases (300°C to 500°C) with rising temperature. This non-monotonic behavior is attributed to two competing mechanisms: the increase in the ionization rate of aluminum acceptor impurities in the base region and the increase in carrier lifetime.

In the KTH study, the on-resistance first decreases (−40°C to 200°C) and subsequently increases (200°C to 500°C) with temperature. This trend is ascribed to the competition between the degradation of carrier mobility and the enhancement of the impurity ionization rate at elevated temperatures [24]. In contrast, the study of Purdue University reported a monotonic increase in on-resistance with temperature (25°C to 325°C) [19]. These divergent observations are potentially due to different base doping concentrations, which lead to varying temperature sensitivities of the impurity ionization rate in the respective devices.

#### 2.1.3 *Radiation reliability*

Based on their BJT technologies, Zetterling's group discovered that their SiC BJTs exhibited a radiation hardness of up to 38 Mrad ($SiO_2$), with a degradation in $\beta$ of less than 10% [33]. Such degradation of BJT current gain is attributed to two potential factors: an increase in the interface recombination rate due to the growth of interface traps at the passivation oxide/SiC interface, and a widening of the emitter-base junction space charge region caused by the accumulation of positive charge within the oxide layer.

Therefore, contrary to conventional wisdom, the radiation response of a BJT remains constrained by the quality of the passivation oxide interface, despite the absence of a gate oxide structure. Also, subsequent research demonstrated that thermally grown oxides possess superior radiation tolerance. This enhanced robustness is attributed to the denser structure and fewer initial defects of thermal oxides, which make them less susceptible to ionization damage under radiation [34].

#### 2.1.4 *Technical challenges*

However, the HOTSiC platform still faces several technical challenges.

(1) The P-type base terminal exhibits significantly higher contact resistivity compared to N-type emitter and collector terminals. This creates an additional voltage drop in the base region, consequently leading to increased driving difficulty and limited high-frequency performance.

(2) High power dissipation issue in SiC BJT ICs stems from two primary factors: (a) the 15 V supply voltage requirement (3× higher than Si TTL's 5 V) dictated by 4H-SiC's wider bandgap and correspondingly higher built-in PN junction voltage, and (b) the inherent static power consumption due to continuous base current flow in BJT operation.

(3) A multi-layer mesa structure is adopted in SiC BJTs, as opposed to the planar structure common in Si BJTs. This is primarily necessitated by the poor quality of the SiC/dielectric interface. Severe recombination of minority carriers injected into the base region would happen at the interface if a planar structure was employed, resulting in excessively low emitter efficiency. Such a mesa structure inevitably increases manufacturing costs and complexity as well as limits the scalability and industrialization of this process platform for large-scale circuit integration.

### 2.2 JFET-based SiC IC platform

Compared to BJTs, the operation of JFETs does not involve minority carriers, thus exhibiting lower temperature sensitivity. Therefore, JFETs are preferred in applications where SiC ICs must exhibit superior long-term high-temperature performance, such as continuous data collection on the Venusian surface or extended jet engine ground testing.

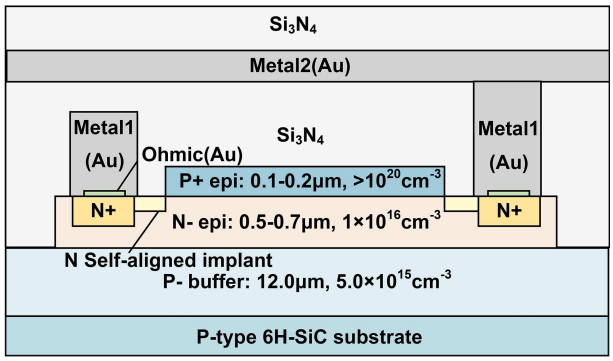


**Figure 4** (Color online) Cross-section of 6H-SiC epitaxial JFET used to implement 600°C logic gates in NASA's 2000 work [35].

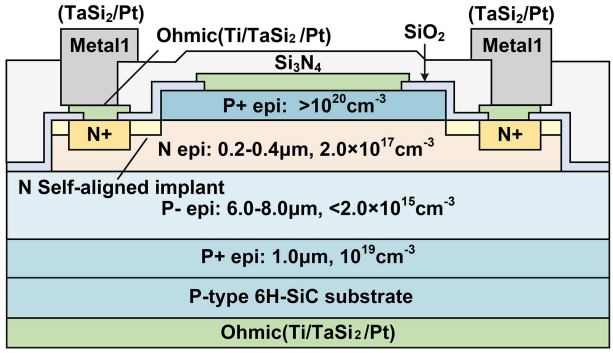


**Figure 5** (Color online) Cross-section of 6H-SiC epitaxial JFET in NASA's 2008 work [39].

### 2.2.1 *Historical development*

The first practice of SiC JFET integration is reported by NASA in 2000 [35]. As shown in Figure 4, a 0.5–0.7 μm, $1 \times 10^{16}$ cm$^{-3}$ doped N-channel layer is grown upon the P-type substrate and P-buffer epilayer to achieve near-zero $V_{\rm th}$. The P+ gate epilayer, is patterned via RIE along with the N-channel region. After the N+ source/drain implantation, a lower-dose nitrogen implantation step is introduced to improve gate controllability. Gold is utilized for both ohmic contacts and metal interconnects, and the dielectric layer is silicon nitride ($Si_3N_4$). The NAND and NOR based on the JFET can withstand a high temperature over 300°C, but they exhibit functional failure when the temperature exceeds 500°C, with visible destruction of contacts and pads observed after electrical testing. Such failure can be attributed to two primary factors: (1) instability of probe tips during wafer-level testing, (2) the degradation of ohmic contacts under high temperature.

To overcome these two limitations, NASA conducted several studies on high-temperature packaging and ohmic contact technologies [36, 37]. Accordingly, in their 2008 work, SiC chips are custom packaged with ceramic before high-temperature testing, and Ti/TaSi/Pt and TaSi/Pt are employed as contact and interconnection, respectively [38]. Additionally, a 600 Åoxide layer is formed through a thermal oxidation process [39] (Figure 5). This method not only passivates the dangling bonds on the SiC surface to stabilize the high-temperature interface, but also mitigates the Young's modulus mismatch between $Si_3N_4$ and SiC. Consequently, the on-state characteristics of JFETs demonstrate less than 10% variation after 3007 h of operation at 500°C. The initial off-state leakage current ($\sim 10^{-5}$ A) shows a thirtyfold reduction after 100 h of thermal stress at 500°C.

With the maturity of 4H-SiC p-substrate growth technology, NASA's 2016 study [40] employed 6–8 μm thick 4H-SiC P-type substrates with doping concentration below $5 \times 10^{15}$ cm$^{-3}$ as shown in Figure 6. Ohmic contacts are further optimized through replacing nitrogen implantation of source and drain with phosphorous (for higher solid solubility and thus an extended doping range) and utilizing Hf instead of Ti as the contact metal. Additionally, silicon oxide ($SiO_2$) dielectric stack was implemented, with a $Si_3N_4$ interlayer inserted between the third and fourth $SiO_2$ layers to prevent atmospheric oxygen diffusion at elevated temperatures. As a result, the on-state characteristics of the JFETs demonstrate less than 5% variation after 2196 h of operation at 500°C. Furthermore, the time delay between gate and mesa etching is reduced to suppress the gate-notching defect, decreasing the off-state leakage current to the order of $10^{-7}$ A (both pre-/post-500°C testing).

The optimized JFET process remained unchanged except for extending N+ implant activation time at 1360°C from 4 h [41] to 100 h and adopting Ti metal ultimately due to processing challenges encountered with Hf-based contacts. Based on the process, NASA demonstrated ring oscillator circuits operational up to 961°C [5] and simple logic gates functioning up to 1022°C [42]. Regarding long-term high-temperature stability, JFET ICs with about 200 transistors are verified to maintain continuous functionality for over one year at 500°C in air atmosphere [43].

Western Reserve University also adopted a normally-on JFET with a similar structure, but their research primarily focuses on high-performance ICs. They have achieved a two-stage amplifier exhibiting a low-frequency voltage gain of 69.2 dB at 576°C (merely 3.6 dB degradation compared to 25°C) and a unity-gain frequency of 1.4 MHz [44]. Additionally, an inverter was demonstrated with a gain $>-20$ at 500°C and a $V_{\rm th}$ variation of $-2.3$ mV·°C$^{-1}$ [45].

The aforementioned studies primarily focus on backend process optimization of SiC JFETs to enable operation at elevated temperatures, while no significant changes have been made to the fundamental device architecture. Furthermore, to exploit the low power consumption advantage of complementary logic circuits, Kyoto University proposed an innovative fully-planar SiC complementary JFETs (CJFETs) with lateral channel controlled by side-

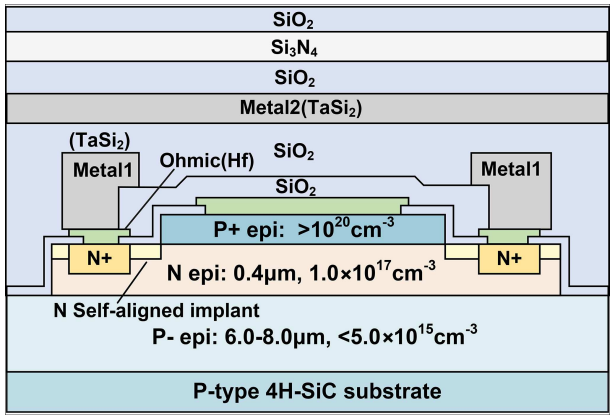


**Figure 6** (Color online) 4H-SiC JFET and two-layer interconnect and dielectric stack [40].

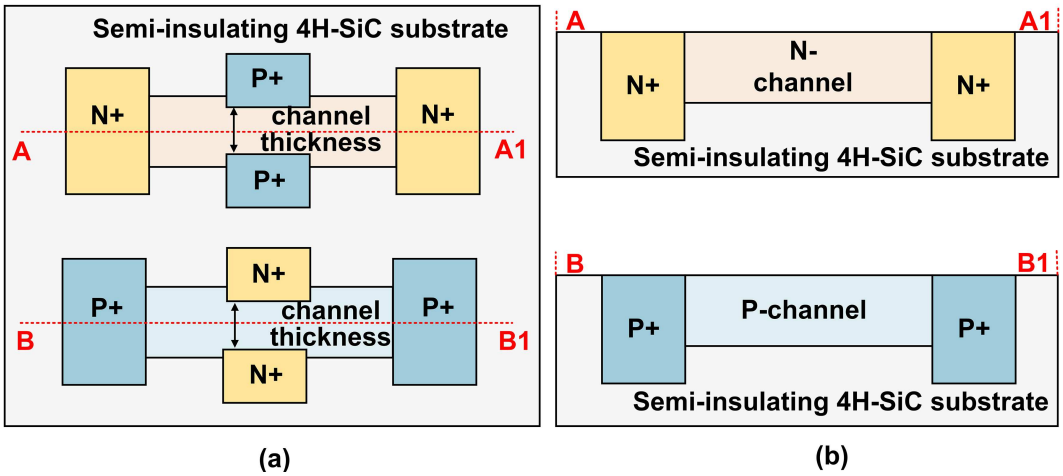


**Figure 7** (Color online) (a) Schematic layouts and (b) cross-section of CJFETs [46, 47].

gates, as illustrated in Figure 7. A high-purity semi-insulating substrate is adopted for inter-device isolation. The channel and side gate were formed by ion implantation at temperatures of 300 and 573 K, with doping concentrations of $5 \times 10^{16}$ and $5 \times 10^{19}$ cm$^{-3}$, respectively [46]. Nitrogen donors or aluminum acceptors can be successfully implanted into semi-insulating SiC wafers, achieving a high electrical activation ratio (>95%) after post-implantation annealing at 1700°C. The $V_{\rm th}$ can be precisely controlled at the mask level by adjusting the channel thickness [47]. The $V_{\rm th}$ of the N-type and P-type JFETs are 0.74 and −0.78 V at room temperature, respectively, and both remain normally-off from RT to 673 K. Additionally, an inverter implemented in this platform operates at a supply voltage as low as 1.4 V, making it highly suitable for low-power circuits. The inverter achieves a $V_{\rm th}$ precisely half of the supply voltage and maintains proper functionality up to 300°C. However, as temperature further increases, the resistivity of the semi-insulating substrate decreases, exacerbating inter-device leakage issues. Thus, this process platform requires additional isolation design for high-temperature operation.

### 2.2.2 *High temperature reliability*

JFETs hold a significant advantage in long-term high-temperature reliability. This stems from the absence of gate oxide reliability limitations (a key weakness of MOSFETs) and their nature as majority-carrier devices (making them less temperature-sensitive than BJTs). This inherent advantage explains why the developmental trajectory of the JFET platform we discussed in Subsection 2.2.1 has consistently been centered on enhancing its capability to withstand prolonged high-temperature operation.

Landmark achievements in the high-temperature characterization of SiC JFET ICs were made by NASA in 2016 and 2017, including a 2196-hour endurance test at 500°C and functional verification at temperatures up to 961°C [42]. It is noteworthy that although the JFET maintains switching functionality at temperatures as high as 961°C, its performance is ultimately constrained by packaging limitations. Beyond 500°C, the leakage currents originating from the packaging become comparable to the device's intrinsic leakage [5]. This clearly indicates

that the high-temperature performance of JFETs is primarily limited by backend-of-line (BEOL) process issues. Consequently, research and development efforts aimed at high-temperature JFET applications have predominantly focused on enhancing the packaging, optimizing ohmic contacts, and improving the dielectric layers.

#### 2.2.3 *Radiation reliability*

NASA also conducted gamma irradiation experiments on their developed operational amplifiers (Op Amps) and ring oscillators. All tested devices demonstrated a total ionizing dose (TID) tolerance exceeding 7 Mrad. Additionally, they performed single-event effects (SEE) tests using heavy ions (from Neon to Gold) on more complex circuits, such as clock circuits and D flip-flops, achieving a maximum linear energy transfer (LET) of 86 $\mathrm{MeV{\cdot}cm^2{\cdot}mg^{-1}}$. No destructive single-event effects, such as burnout or latch-up, were observed. Consequently, the superior radiation tolerance of the SiC JFET has been experimentally verified, which stems primarily from its inherent immunity to gate oxide degradation mechanisms.

#### 2.2.4 *Technical challenges*

Overall, JFETs exhibit lower static power consumption compared to BJTs, but they still face certain challenges and limitations.

(1) Normally-off devices are challenging to implement, usually requiring precise control over both channel thickness and doping concentration.

(2) The circuit design presents significant challenges, stemming from two main factors. First, despite the built-in potential of SiC being three times that of Si, the forward voltage margin remains limited. Second, for normally-on devices, the requirement for a negative gate drive voltage increases design complexity and leads to larger chip area.

(3) The process complexity is high, requiring either etching or the introduction of additional defects or vanadium dopants to form the semi-insulating substrate. Furthermore, for the epitaxial channel structure employed by NASA, the device performance is critically dependent on the uniformity of the channel layer thickness. This imposes a significant challenge for achieving high-quality and highly uniform epitaxial growth processes.

### 2.3 MOSFET-based SiC IC platform

MOSFETs outperform JFETs and BJTs with higher input impedance, lower power consumption and superior scalability, enabling compact, high-speed digital designs [48,49]. Their voltage-controlled operation simplifies driving circuits, while CMOS compatibility allows efficient logic integration. These advantages make MOSFETs dominant in microprocessors, memory, and mixed-signal ICs [50].

#### 2.3.1 *Historical development*

SiC exhibits a striking 10:1 electron-to-hole mobility ratio [51], and thus early MOSFET-based SiC ICs predominantly employed all-NMOS designs due to PMOS fabrication challenges and significantly inferior carrier mobility performance. Depletion-mode and enhancement-mode NMOS, diffusion and polysilicon resistors are utilized as load or pull-up devices in place of PMOS to compose these all-NMOS circuits, including operational amplifiers [52, 53], gate drivers [54–56] and logic circuits [57]. However, all-NMOS ICs suffer from high static power, slower switching and lower noise margins compared to CMOS. This inherent inefficiency of all-NMOS ICs directly led to the development of CMOS technology.

High-performance SiC PMOS devices are essential for implementing SiC CMOS ICs to enable both low static power consumption and complex circuit functionality. In 1995, Cree Research, Inc. demonstrated the first enhancement-mode p-channel 6H-SiC MOSFETs [58]. Building on this breakthrough, a CMOS operational amplifier with an open-loop gain of approximately $10^4$ (80 dB) was subsequently reported in 1996 [59]. Later in 2004, Han et al. successfully fabricated 4H-SiC PMOS, demonstrating significantly lower substrate defect density and higher carrier mobility compared to their 6H-SiC counterparts [60], and then the first SiC CMOS inverter was fabricated successfully in 2006 [61]. These studies [58–61] established the cornerstone for subsequent 4H-SiC IC development.

Later in 2011, Raytheon UK introduced high temperature silicon carbide (HiTSiC), a proprietary 1.2 μm 4H-SiC CMOS process technology [62]. As shown in Figure 8, the architecture employs an N-sub/N-epi layer stack with double-well implantation, utilizing nickel for ohmic contacts to both N+ and P+ doped regions and aluminum for interconnection. To enhance high-temperature reliability, the researchers proposed a plan of replacing aluminum interconnects with refractory metals and optimizing the gate dielectric stack.

Subsequently, their research implemented a dual-polysilicon layer architecture, where the first layer served as gate electrodes while the second layer formed integrated polysilicon capacitors and resistors [63, 64]. These passive

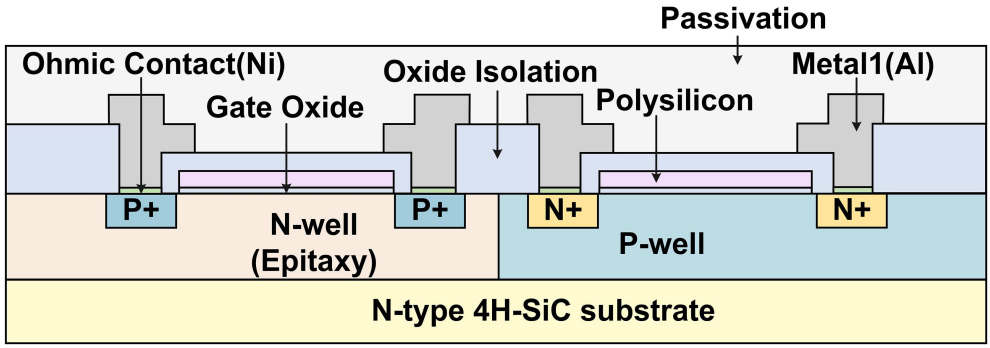


**Figure 8** (Color online) Cross-section of HiTSiC technology [62].

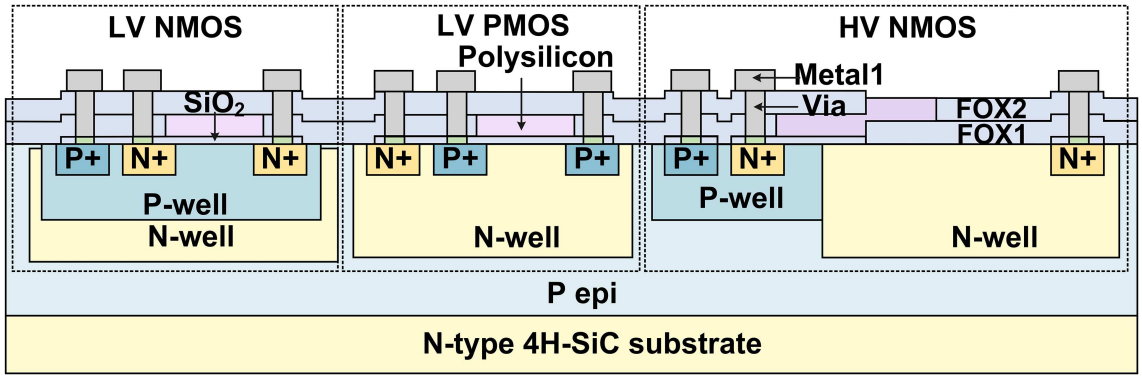


**Figure 9** (Color online) Cross-section of the fabricated LV NMOS, LV PMOS and LDMOS on a P-epi grown on an N+ substrate proposed in [76].

components specifically addressed analog circuit requirements, particularly for autozeroing techniques to compensate for $V_{\rm th}$ instabilities induced by the inherent SiC/$SiO_2$ interface traps under prolonged high-temperature operation [65]. Leveraging this HiTSiC platform, research teams from the University of Arkansas and Ozark Integrated Circuits demonstrated multiple functional blocks including precision comparators [66], 8-bit data converters (both DAC and ADC) [67, 68], current reference circuits [69], gate drivers [70, 71], digital logic [72]. However, the technology's development was abruptly discontinued following the 2018 closure of Raytheon's dedicated SiC CMOS fabrication facility [73], which served as the primary manufacturing base for these integrated circuits. There also emerged some studies on special SiC CMOS structures, like those with recessed channel [74] and mesa etching isolation [75]. However, none of them have become mainstream processes yet.

Next promising CMOS SiC technology candidate after HiTSiC is dominated by the Fraunhofer Institute for integrated systems and devices technology (IISB). In 2019, their collaboration with the University of Arkansas yielded the first demonstrated SiC BCD process platform integrating NMOS, PMOS and lateral diffused MOSFET (LDMOS) devices [76]. As illustrated in Figure 9, this platform features an N-sub/P-epi configuration, triple-well junction structure, and single-layer polysilicon/metal implementation. Notably, it is the first successful fabrication of P-well regions within an N-well architecture in a SiC IC process platform. Six transistor (6T) static random-access memory (SRAM) cell [77] and gate driver [78] are implemented based on this platform. However, the process exhibits two systematic challenges: (1) N-well over-etching leading to elevated P+ contact resistivity (44 m$\Omega\cdot$cm$^2$) compared to N+ contacts in P-well regions (1.7 $\mu\Omega\cdot$cm$^2$), and (2) excessively high $V_{\rm th}$ over $-10$ V in PMOS device due to high doping concentration of N-well. These issues collectively impact device performance and manufacturing yield.

Later in 2022, Delft University of Technology conducted their work upon the state-of-the-art 6 μm SiC CMOS technology developed at Fraunhofer IISB for further improvement [73]. As shown in Figure 10, N-sub/N-buffer/N-epi stack is adopted in this process platform. The PMOS device obtains a reduced $V_{\rm th}$ of $-6.2$ V thanks to the adoption of lightly-doping N-epi layer. Moreover, for low contact resistivity, Ti/Al and Ni/Al are utilized to form ohmic contacts with P+ and N+ regions, respectively. Based on this platform, more complex digital circuits were realized, such as amplifiers (folded cascade, differential) [79], ultraviolet (UV) image sensors [80], temperature sensors [81], quadrant sun position sensors [82, 83], digital logic blocks [73] and on-chip readout systems [80].

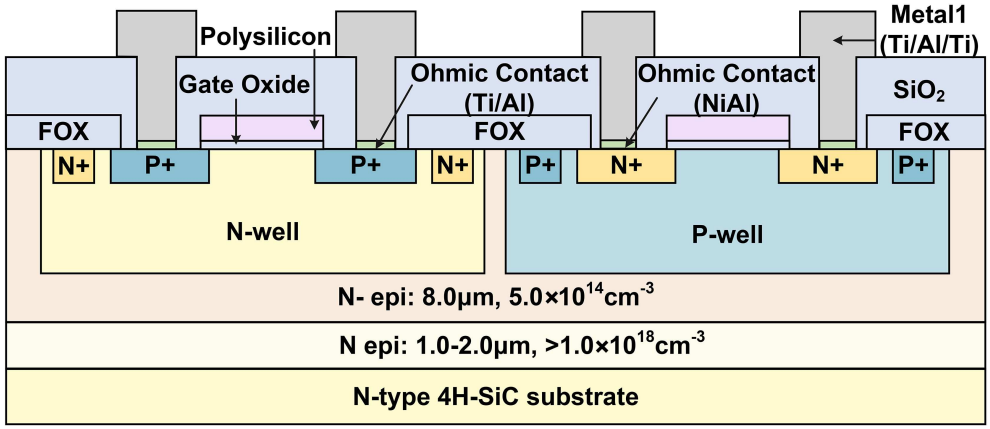


**Figure 10** (Color online) Cross-section of the fabricated LV CMOS on N-epi/N-buffer/N-sub stack proposed by Delft University of Technology [73].

**Table 2** Summary of the SiC CMOS platform.

| | 2011<br>HiTSiC | 2019<br>University of Arkansas<br>& Fraunhofer IISB | 2022<br>Delft University of Technology<br>& Fraunhofer IISB |
|---|---|---|---|
| Refs. | [62–64, 66–72] | [76–78] | [73, 79–81] |
| Epitaxial stack | N-sub/N-epi | N-sub/P-epi | N-sub/N-buffer/N-epi |
| $V_{\rm th}$ (NMOS) | 9 V<br>(extracted from figure) | – | (2.23±0.12) V<br>($W/L$ = 20 μm/6 μm) |
| $V_{\rm th}$ (PMOS) | −10.8 V<br>(extracted from figure) | Over −10 V<br>(extracted from figure) | (−6.25±0.07) V<br>($W/L$ = 80 μm/6 μm) |
| Minimum channel length | 1.2 μm | 1.5 μm [76], 1 μm [77, 78] | 6 μm |
| Circuit types and maximum operating temperature | Precision comparators (450°C) [66], 8-bit data converters (both DAC (400°C) [67] and ADC (200°C) [68]), current reference circuits (540°C) [69], gate drivers (500°C) [70, 71], digital logic (300°C) [72] | 6T-SRAM (300°C) [77] and gate driver (300°C) [78] | Amplifiers (folded cascade, differential) (400°C) [79], ultraviolet (UV) image sensors (200°C) [54], temperature sensors (600°C) [81], quadrant sun position sensors (200°C) [82, 83] and digital logic blocks (200°C) [73] |

Table 2 summarizes the fabrication details and key performance metrics of the SiC CMOS platform discussed above.

### 2.3.2 *High temperature reliability*

Currently, the maximum operating temperature of SiC MOSFET-based process platforms is 500°C [84], and the main limiting factor is the high density of trap states at the $SiO_2$/SiC interface caused by high temperatures. Deterioration of the gate oxide interface leads to mobility degradation and $V_{\rm th}$ drift. The absolute values of $V_{\rm th}$ (NMOS) and $V_{\rm th}$ (PMOS) both decrease with rising temperature, but $V_{\rm th}$ (PMOS) decreases at a slower rate compared to $V_{\rm th}$ (NMOS) due to the lower temperature dependence of hole mobility [61]. Furthermore, the frequency of the ring oscillator increases with rising temperature because of a reduction in the inverter's output impedance resulting from lower $V_{\rm th}$ at higher temperatures [85]. Some special techniques are employed to enhance the temperature stability of CMOS integrated circuits, including the design of auto-zero [63] and the utilization of high-temperature refractory metals such as Ti/Pt for interconnects [84].

### 2.3.3 *Radiation reliability*

Current research about the effects of irradiation on SiC MOSFET-based IC includes analog circuits [6, 86, 87] and logic circuits [88–90]. 4H-SiC transimpedance amplifiers (TIAs) can function normally up to 1.2 MGy [6], while 4H-SiC integrated active pixel sensor (APS) circuits operate reliably at 2 MGy [86], validating the superior irradiation resistance of SiC integrated circuits. Further details on this section will be covered extensively in Section 4.

**Table 3** Comparative summary of BJT-, JFET-, and MOSFET-based SiC IC platforms.

| Key aspect | BJT-based IC | JFET-based IC | MOSFET-based IC |
|---|---|---|---|
| Gate oxide requirement | No | No | Yes |
| Drive method | Current-driven, high static power consumption [91] | Voltage-driven, normally-on devices require negative voltage to turn off, narrow drive voltage range [92] | Voltage-driven, simple and universal drive circuit design |
| Switching speed and loss | Slow switching speed; high switching loss, especially high turn-on loss [93] | Fast switching speed, inferior body diode reverse recovery characteristics; low switching loss | Fast switching speed, low body diode reverse recovery charge; low switching loss |
| Maximum demonstrated temperature | High ($>400^{\circ}$C) | Very high ($>500^{\circ}$C) | Moderate-to-high ($\sim300^{\circ}$C–$400^{\circ}$C) |
| Radiation robustness | Moderate | High | Interface-dependent |
| Static power consumption | High | Low | Very low (CMOS) |
| Complementary logic implementation | Difficult | Challenging | Natural (CMOS) |
| Integration density | Low-moderate | Moderate | High |
| Process compatibility with modern SiC power devices | Limited | Moderate | High |
| Scalability for complex power IC | Limited | Moderate | Excellent |
| Chip area efficiency | Low | Moderate | High |
| Cost | Process complexity is higher than that of Si BJT with multi-layer mesa structure | Process complexity is higher than that of Si JFET, requiring either etching or the introduction of additional defects or vanadium dopants to form the semi-insulating substrate | Yield and cost affected by gate oxide process; normally-off characteristic requires no additional circuitry, resulting in low system design cost |
| Advantages | Gate-oxide-free operation; attractive for harsh-environment basic logic/driver functions | Demonstrated feasibility at very high temperature with more complex interconnect integration | Best path to complex logic/mixed-signal SiC IC integration |
| Limitations | Higher static power and supply voltage; scalability to large-scale integration is challenging | Normally-off realization and drive scheme complexity; BEOL/packaging can limit practical integration | Oxide/interface-induced instabilities and reliability engineering burden; PMOS performance/variability remains a bottleneck |

#### 2.3.4 *Technical challenges*

Currently, the main technical challenges of MOSFET-based IC process platforms are threshold matching and the gate oxide reliability issues arising from the complex $SiO_2$/SiC interface. These aspects will be discussed in detail in Section 4 later and are not elaborated here. Nevertheless, compared to JFET and BJT technologies, MOS still exhibits higher process maturity and circuit design feasibility, making it the relatively preferred process at present.

### 2.4 Comparative perspective on SiC IC integration platforms

While BJT-, JFET-, and MOSFET-based SiC IC platforms have all demonstrated technical feasibility for high-temperature and radiation-tolerant electronics, their suitability for scalable and economically viable monolithic integration differs substantially when manufacturability, chip area efficiency, and cost implications are considered, as summarized in Table 3 [91–93].

BJT-based platforms enabled early high-temperature circuit demonstrations and benefit from oxide-independent operation. However, their relatively high static power consumption and limited integration density typically result in larger chip area and increased thermal management complexity. Furthermore, achieving complementary functionality is nontrivial, increasing process complexity and limiting scalability for large-scale integration.

JFET-based platforms exhibit excellent intrinsic high-temperature robustness due to the absence of gate oxide and majority-carrier conduction. Nevertheless, threshold voltage tuning is less flexible, and complementary device implementation often requires additional process steps or structural complexity. As a result, chip area may increase, and manufacturing flow becomes less aligned with mainstream SiC power device fabrication, potentially impacting cost competitiveness.

In contrast, MOSFET-based platforms leverage mature MOS processing technology and naturally support CMOS architectures, enabling high integration density and reduced static power consumption. Although challenges associated with $SiC/SiO_2$ interface traps and threshold stability remain, MOSFET technology offers better compatibility with existing industrial SiC power device manufacturing lines. This process synergy facilitates improved manufacturability, wafer-level scalability, and cost reduction potential for complex power IC systems.

Therefore, when both device physics and system-level integration factors are considered—including scalability, manufacturability, chip area efficiency, and potential cost—MOSFET-based IC platforms currently represent the most promising pathway toward industrial-scale SiC integration, while BJT and JFET platforms remain advantageous for niche ultra-high-temperature or specialized applications.

## 3 Power IC platform

Besides LV digital and analog circuits, power ICs (PICs) represent another critical development frontier for SiC IC technology. The primary objective is to integrate LV devices (required for control and drive circuits) with

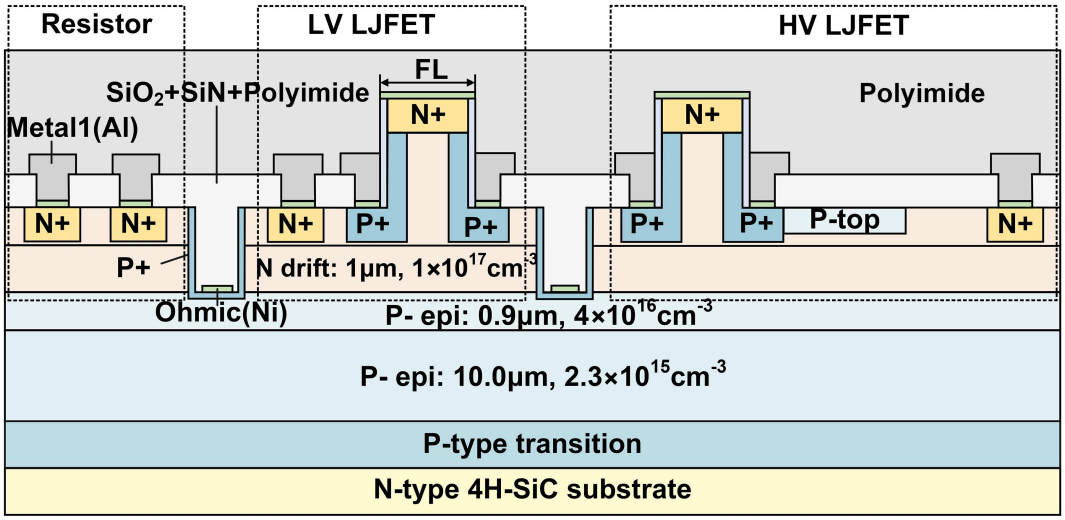


**Figure 11** (Color online) Schematic structure of the VC-LJFET technology platform. Integration of HV and LV JFETs, N-type SiC resistors and implanted trench isolation [94].

HV devices for power processing monolithically, thereby alleviating issues in discrete solutions such as significant interconnect parasitic parameters, bulky system size, and reliability concerns associated with additional wire bonds. By developing an HV and LV integration platform, the number of components, interconnection points, and solder joints in the system can be significantly reduced, thereby achieving high power density, high operating speed, and high reliability.

### 3.1 LV and lateral HV device integration platform

The most common PIC platforms integrate LV circuits with lateral HV power devices, fully leveraging the advantage that all terminals of lateral power devices are located on the top surface. Current PIC platforms are predominantly based on MOSFETs, which primarily rely on the superior voltage handling capability and compatibility with standard IC fabrication processes of LDMOS. There are also a few platforms utilizing JFETs, but virtually none based on BJTs, presumably due to the challenges associated with developing lateral power BJTs.

#### 3.1.1 *JFET-based PIC platform*

In 2008, a vertical-channel JFET structure was proposed in [94], as shown in Figure 11. This LJFET technology platform is proposed by Rutgers University, integrating HV JFETs, LV JFETs and N-type SiC resistors monolithically. Both HV and LV JFETs have vertical channels formed with mesa-etching and self-aligned implantation. For HV JFET, a double-reduced surface field (RESURF) structure comprising a top p-RESURF and bottom P- layer is adopted, realizing a maximum breakdown voltage ($BV$) of 800–1000 V. The power device achieves an excellent figure of merit (FOM) of 17.5 Ω·pF, where FOM is defined as the product of specific on-resistance ($R_{on,sp}$) and output capacitance ($C_{oss,sp}$). This value indicates superior static and dynamic performance characteristics compared to conventional silicon-based power devices. LV JFET differs from HV counterparts mainly in shorter drift length ($L_{drift}$) and removed top p-RESURF, establishing a 4-stage N-type JFET resistor load inverter to drive the HV JFET. Specially, the isolation structure between HV and LV parts is fabricated by 1.7 μm trench etching and ion implantation. The drift layer thickness is designed to be 1 μm, ensuring that the trench isolation can penetrate to the base of the P-type epitaxial layer for effective grounding. The megahertz switching ability of the power IC fabricated is validated at 200 V, 2 A [95].

#### 3.1.2 *MOSFET-based PIC platform*

The advancement of LDMOS serves as the cornerstone of MOSFET-based PIC. Research on SiC LDMOS [96–100] has been reported since 1998 to achieve a better $R_{on,sp}$-$BV$ trade-off. However, these investigations overlooked two critical challenges for PIC, including the process compatibility and the effective isolation between HV and LV SiC devices.

Subsequently, research institutions such as State University of New York Polytechnic Institute increasingly reported the investigation on embedding HV LDMOS into LV SiC CMOS process [101–104]. In 2021, they demon-

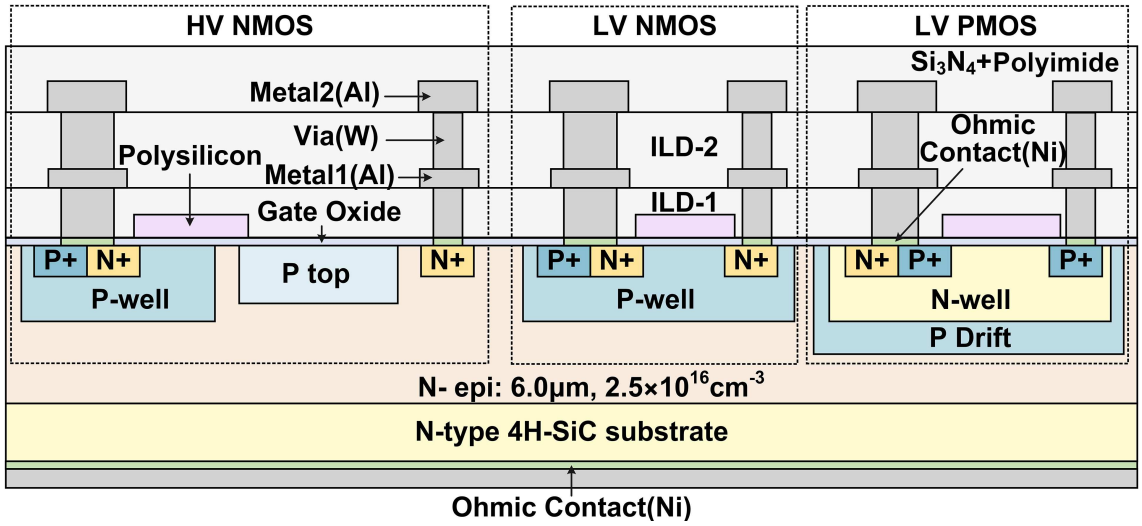


**Figure 12** (Color online) Cross-section of the fabricated HV NMOS, LV NMOS and LV PMOS on an N-epi grown on N+ substrate [101].

strated a process platform monolithically integrating HV LDMOS and LV CMOS [101]. As shown in Figure 12, the platform starts from a 6 μm, 2.5 × $10^{16}$ $cm^{-3}$ N-epi grown on the N+ substrate. 50 nm gate oxide of HV and LV devices is formed simultaneously through high temperature CVD, followed by 180 min annealing in $N_2O$ and $N_2$ atmospheres. For ohmic contacts, a single Ni metal layer is identified to achieve lower contact resistance in both N+ and P+ regions compared to the Ni/Ti metal stack, as validated by the circular transmission line model (CTLM) method. The HV LDMOS in this work incorporates a P-top layer to form a RESURF structure, achieving a $BV$ of 520 V and a $R_{on,sp}$ of 7.3 mΩ·$cm^2$, demonstrating a superior trade-off to prior work [105]. In PMOS, channeling implantation is adopted to form a 2.5 μm deep P-well structure that effectively isolates the N+ source region from the substrate while simultaneously providing essential channel doping compensation for proper $V_{\rm th}$. However, this may introduce new problems, including uncontrollable doping distribution (depth deviation and trailing effect) and deep lattice damage that cannot be repaired by conventional annealing. The $V_{\rm th}$ of NMOS and PMOS are 6 and −10.3 V, respectively. Techniques for balancing the $V_{\rm th}$ of CMOS will be further discussed in detail in Section 4.

Although HV LDMOS and LV CMOS have been fabricated successfully via the same BCD process flow, the critical isolation challenge between HV and LV regions must be resolved to ensure reliable implementation of the power IC process. Hence in their further work [102], an N-sub/P-epi/N-epi stack and P+ isolation well are adopted to realize the isolation between the LV devices and HV LDMOS as shown in Figure 13. The P+ isolation well formed through channeling implantation mentioned in [101] demonstrates a 180 V blocking capability, which needs to be further optimized for enhanced blocking performance in a higher-voltage-level SiC BCD process. Apart from isolation design, the number of metal layers is increased to three for higher reliability and scalability. Digital CMOS ICs such as oscillators and inverters with higher operating frequency and temperature are fabricated on this platform [103].

In their 2022 work [104], three types of edge termination and peripheral designs (as shown in Figure 14) for SiC HV LDMOS were further investigated to obtain higher $BV$. For N-epi/N+ substrate stack, the source-centered architecture effectively terminates the internal electric field, whereas the drain-centered variant necessitates hybrid junction termination extension (JTE) implementation to optimize the edge electric field distribution in HV LDMOS devices, thereby sustaining $BV$ exceeding 500 V. For N-epi/P-epi/N+ substrate stacks, the drain-centered design achieves $BV$ values above 500 V through JTE integration, while the source-centered counterpart attains $BV$ of 400 V via P+ isolation implementation.

Although HV and LV devices can be fabricated simultaneously, HV circuits remained unrealized until the demonstration of a half-bridge driver on a 200 V all-SiC process platform proposed by Southeast University in 2024 [106, 107]. As shown in Figure 15, the process platform includes HV and LV devices such as LDMOS, Diode, NMOS, PMOS, resistor and capacitor. The P-epi/P-buffer/N+ substrate stack is utilized, with experimental verification showing that the P-buffer layer effectively optimizes vertical electric field distribution, resulting in a 212.4% enhancement in vertical breakdown voltage. Consequently, the HV LDMOS achieves a $BV$ of 310 V with merely 4 μm drift region length. Device isolation between HV and LV regions is undertaken by an N-well/P-epi junction, which demonstrates a 356 V blocking capability. Based on the process platform, the half-bridge gate driver, which consists of a high-side driver and a low-side driver, is proposed as shown in Figure 16. The low-side driver is com-

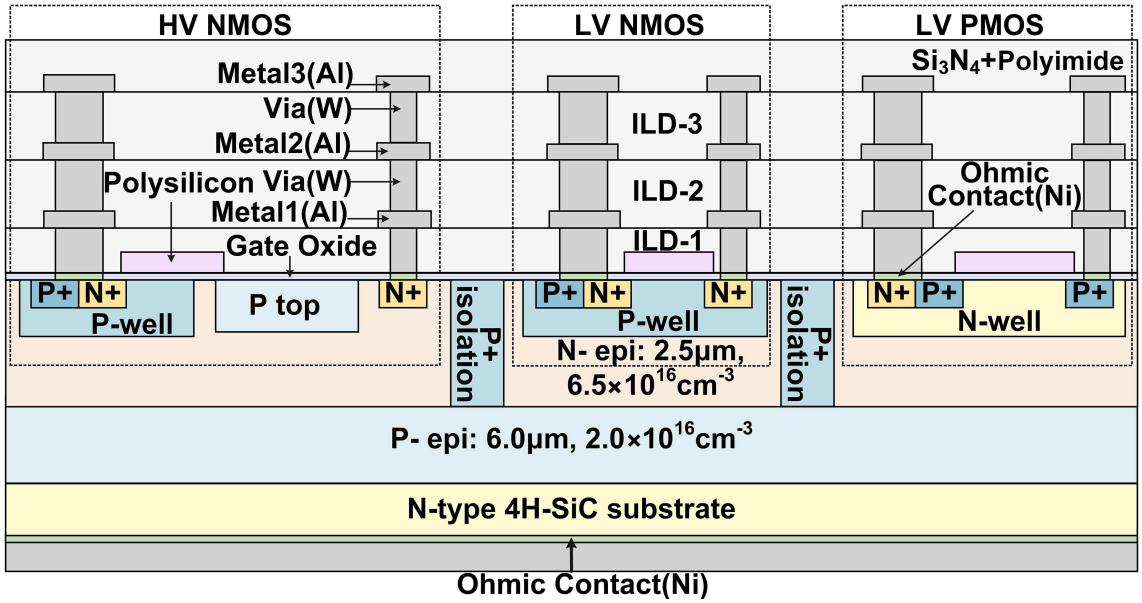


**Figure 13** (Color online) Cross-section of the fabricated HV NMOS, LV NMOS and LV PMOS [102].

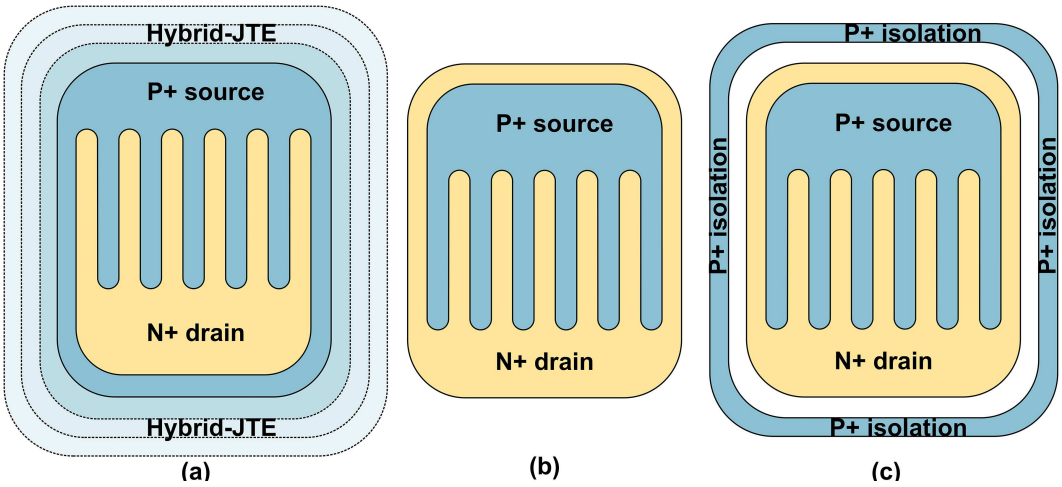


**Figure 14** (Color online) Top view schematic of the (a) drain-centered design with hybrid JTE termination, (b) source-centered design without P+ isolation, and (c) source-centered design with the P+ isolation junction termination [104].

posed of a four-stage CMOS inverter chain, while the high-side driver has three parts: (i) in input stage, a CMOS inverter, (ii) a level-shift circuit and (iii) in output stage, a two-stage high-side inverter chain. The fabricated half-bridge driver can operate normally at 200°C.

Table 4 summarizes the fabrication details and key performance metrics of MOSFET-based LV and lateral HV integration platform.

### 3.2 LV and vertical HV device integration platform

Owing to the mature fabrication process and successful industrialization of SiC vertical double-diffused MOSFET (VDMOS), as well as its superior high-current and high-voltage handling capability compared to LDMOS, a specialized HV and LV compatible process platform has been developed. This platform monolithically integrates vertical power devices with lateral LV circuits. Unlike lateral power devices, vertical devices feature their drain terminal on the substrate's backside. Therefore, the key challenge in such an integration platform lies in effectively isolating LV components from HV interference caused by the backside drain terminal. This section focuses on the isolation structure's fabrication process and blocking capability. This LV + vertical-HV SiC integration is generally intended for a single vertical HV power device, with the lateral LV part providing CMOS-based gate drive (e.g., inverter-chain drivers) and basic protections (over-current/over-temperature). Accordingly, it is not intended to integrate multiple

**Table 4** Summary of SiC MOSFET-based LV and lateral HV integration platform.

| | 2021<br>State University of New York Polytechnic Institute (N-sub/N-epi) | 2021<br>State University of New York Polytechnic Institute (N-sub/P-epi/N-epi) | 2024<br>Southeast University |
|---|---|---|---|
| Refs. | [101] | [102, 103] | [106, 107] |
| Epitaxial stack | N-sub/N-epi | N-sub/P-epi/N-epi | N-sub/P-epi |
| $V_{\rm th}$ (NMOS) | 6 V<br>(extracted from figure) | 5.6 V | 2.5 V |
| $V_{\rm th}$ (PMOS) | −10.3 V<br>(extracted from figure) | −8.5 V | −8.2 V |
| Minimum channel length | 1 μm | 1 μm<br>(0.5 μm for LDMOS) | 2 μm |
| $BV$ (LDMOS) | 520 V | 620 V | 310 V |
| $R_{on,sp}$ (VDMOS) | 7.3 Ω·cm$^2$ | 9.73 Ω·cm$^2$ | – |
| $BV$ (isolation) | – | 180 V | 356 V |
| Circuit types and maximum operating temperature | Ring oscillator<br>(200°C) | Ring oscillator (450°C)<br>and CMOS inverter (400°C) | Half-bridge driver (200°C)<br>and inverter (200°C) |

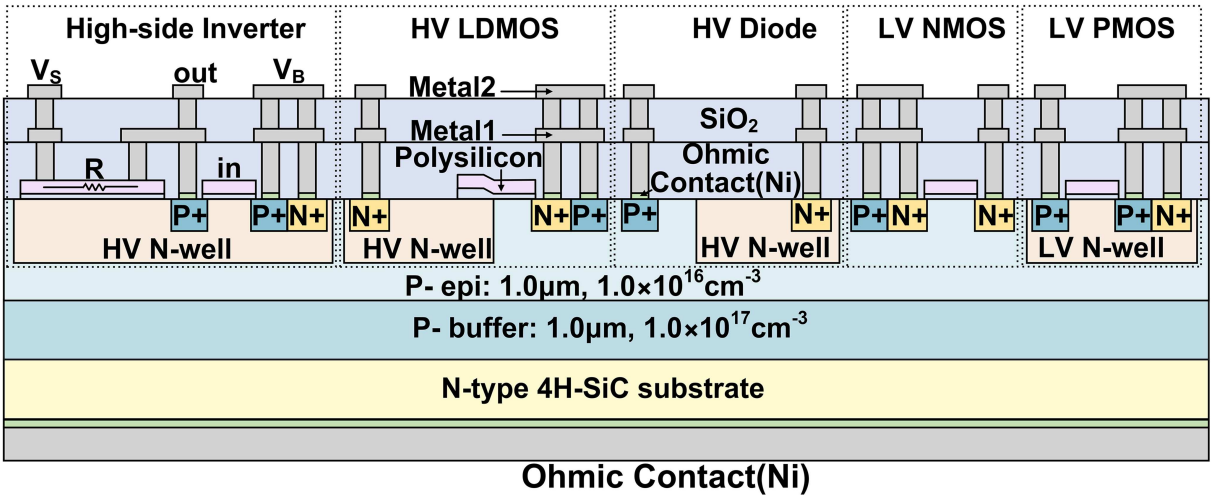


**Figure 15** (Color online) Schematic cross-section of 200 V all-SiC floating gate driver process platform [106].

HV power-stage devices on-chip as in mature Si BCD platforms.

The first demonstration of hybrid monolithic integration in SiC was reported by Wolfspeed in 2014 [108]. As shown in Figure 17, the implemented SiC IC structure integrates a 1200 V-rated vertical power MOSFET (VDMOS) fabricated using a planar gate process with a gate buffer circuit employing NMOS pull-up and pull-down networks that require complementary input signals. Fabricated on a 10 μm-thick N-drift layer (doping concentration: $6 \times 10^{15}$ cm$^{-3}$), the design incorporates an additional deep P-well (distinct from the VDMOS P-wells) surrounding the gate buffer (Figure 18), featuring enhanced depth and elevated bottom doping concentration to enable 20 V gate buffer operation while maintaining isolation from the VDMOS's backside drain potential of 1200 V.

However, the absence of CMOS technology in this implementation necessitates the use of an NMOS pull-up circuit, which reduces the gate buffer's maximum output voltage from VDD to VDD-$V_{\rm th}$ (NMOS). This compromised output swing consequently diminishes the gate drive voltage of the VDMOS, resulting in a significantly higher $R_{on,sp}$ (20 mΩ·cm$^2$) compared to discrete VDMOS (7 mΩ·cm$^2$). To overcome this limitation inherent to NMOS-based control circuits, the adoption of PMOS pull-up devices is recommended, highlighting the critical need for developing CMOS technology on SiC.

The possibility of integrating CMOS gate buffer and 1200 V VDMOS on 4H-SiC was first investigated by Taiwan Tsing Hua University [109]. Compared with [108], the devices in this design are fabricated monolithically without additional process steps or cost. As illustrated in Figure 19, the PMOS is designed in the N-drift region, where both source and drain P+ regions are enclosed by P-well. Notably, excessive PMOS channel length may establish leakage paths between PMOS and VDMOS devices. Furthermore, the elevated substrate potential induces a significant $V_{\rm th}$ shift in PMOS due to pronounced body effect, exacerbating the $V_{\rm th}$ mismatch between NMOS and PMOS,

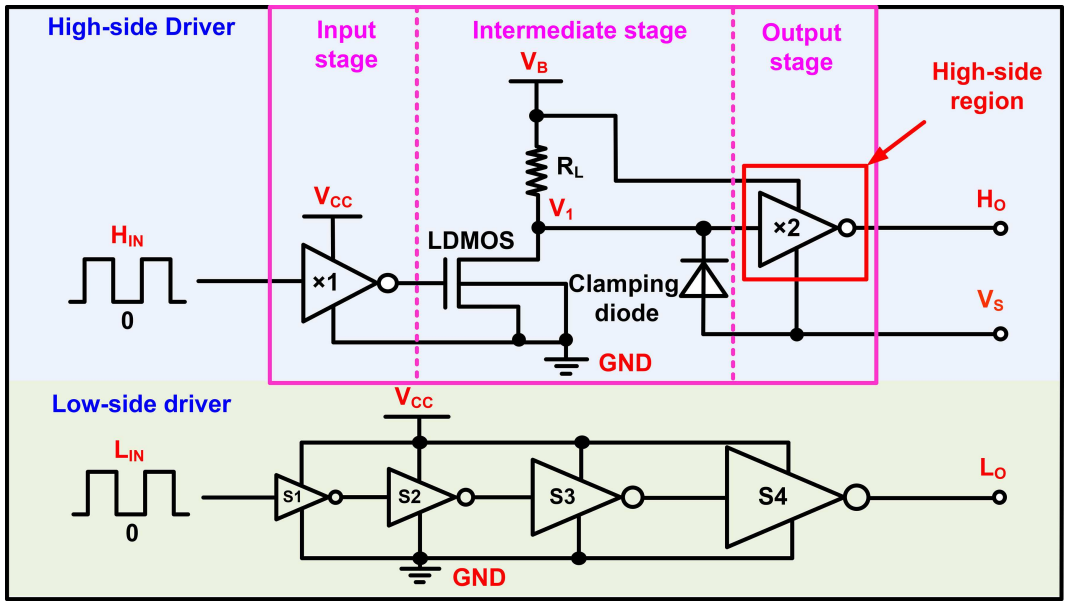


**Figure 16** (Color online) Schematic of the half-bridge driver [107].

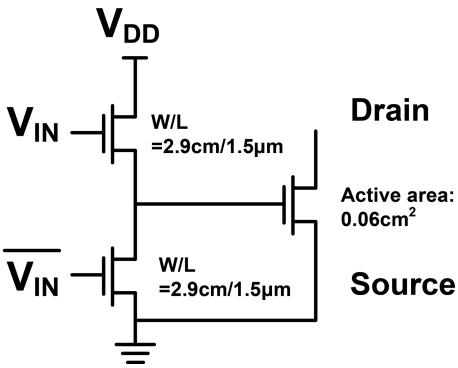


**Figure 17** Equivalent circuit schematic for the integrated device [108].

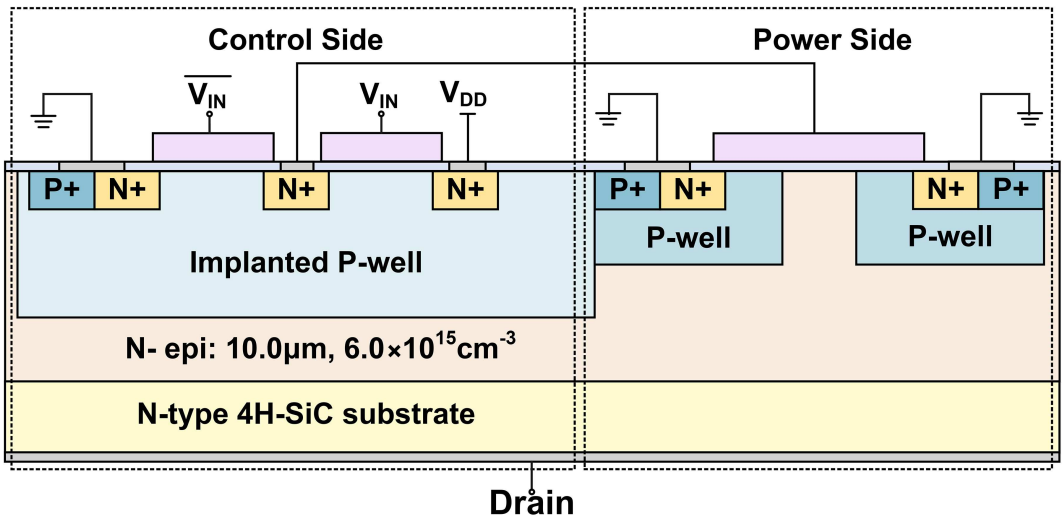


**Figure 18** (Color online) Simplified cross-section of the 4H-SiC power DMOSFET with integrated gate buffer [108].

consequently compromising noise margin.

In Si-technology, the $V_{\rm th}$ mismatch problem can be solved by counter doping [110]. But for SiC, Al+ implantation

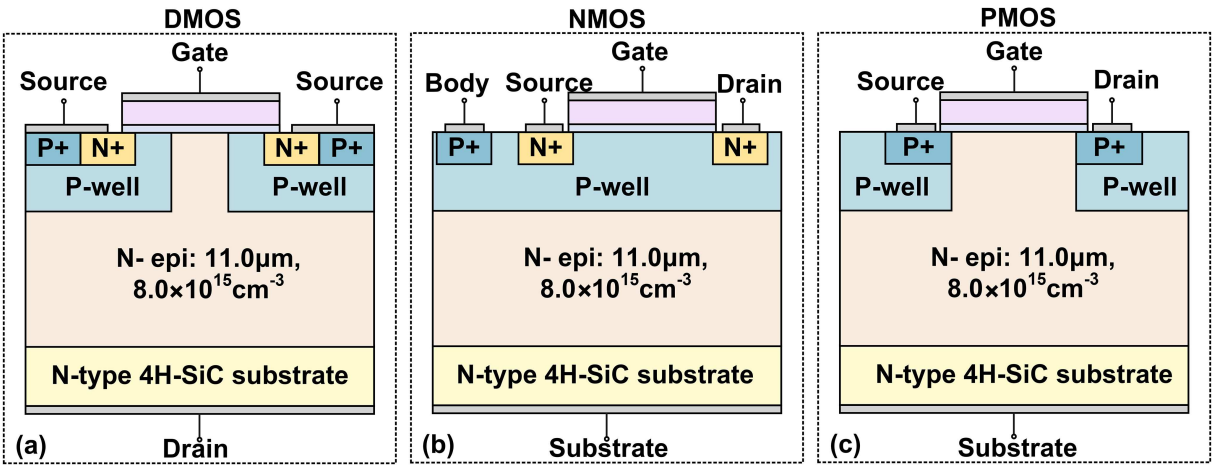


**Figure 19** (Color online) Schematic cross-section of the devices fabricated on a chip in this study. (a) A vertical DMOS cell, (b) an n-channel lateral MOSFET, and (c) a p-channel lateral MOSFET. The substrate electrode is the same as the drain electrode [109].

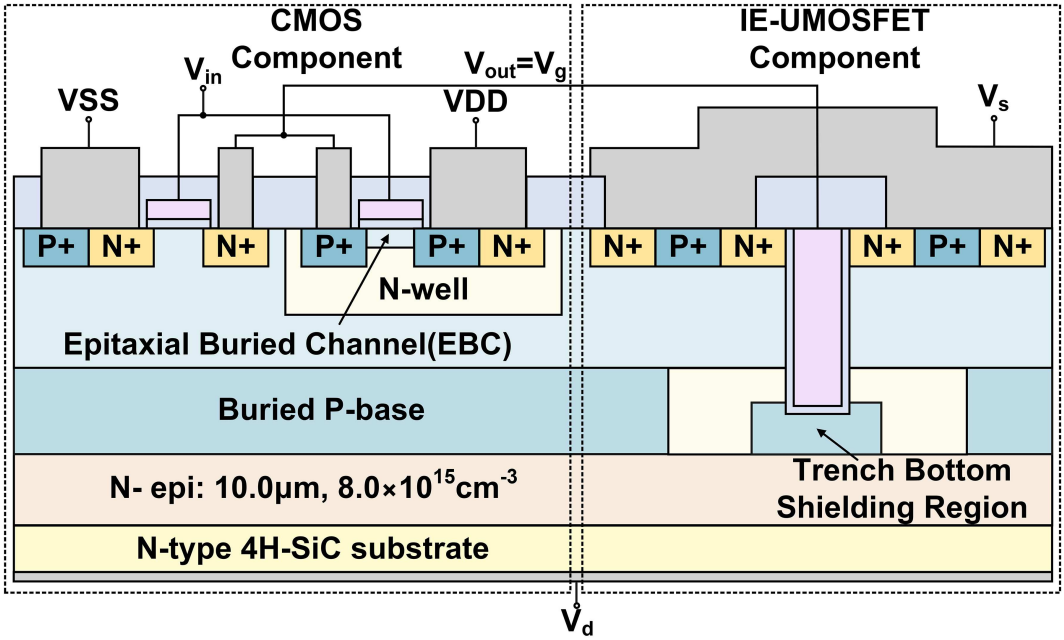


**Figure 20** (Color online) Schematic cross section of the monolithic SiC power IC fabricated in this study [114].

in the N-type channel region of SiC PMOS induces damage and positive charges on the surface of SiC, thus affecting the quality of the gate oxide interface and channel mobility [111–113]. Therefore, the Advanced Power Electronics Research Center (APERC) developed an epitaxial buried channel (EBC) structure by growing a P-epi layer on the p-base epitaxial layer, serving as an implantation-free counter doping layer for PMOS (Figure 20) [114]. This approach effectively reduces the PMOS's $V_{\rm th}$ from $-17.4$ to $-9.3$ V, which achieves a more balanced inverter switching voltage ($V_{sp}$) from 5.2 to 10.3 V (VDD = 20 V), larger noise margin and better-matched CMOS current driving ability. For the power MOSFET, an Implantation and Epitaxial UMOSFET (IE-UMOSFET) architecture is adopted, which features (i) a trench-bottom shielding region that mitigates electric field concentration, and (ii) a buried p-base grown atop the n-drift layer to isolate CMOS circuits from the high drain voltage of the IE-UMOSFET. This SiC IC demonstrates 1500 V blocking capability while maintaining the integrated CMOS functionality.

However, a potential problem of such an isolation method is the high cost and unpopularity of the P-type SiC epilayer growth process. Hence a new isolation scheme was introduced by Taiwan Yang Ming Chiao Tung University [115,116]. As shown in Figure 21, the isolation architecture employs vertically stacked P-iso buried layers beneath NMOS/PMOS regions combined with side P-well isolation, creating a robust isolation barrier between LV CMOS devices and the VDMOS structure. The P-iso structure is able to sustain a reverse voltage of over 800 V. It is comparable to the blocking ability of VDMOS and makes them compatible on a monolithic SiC IC. Furthermore,

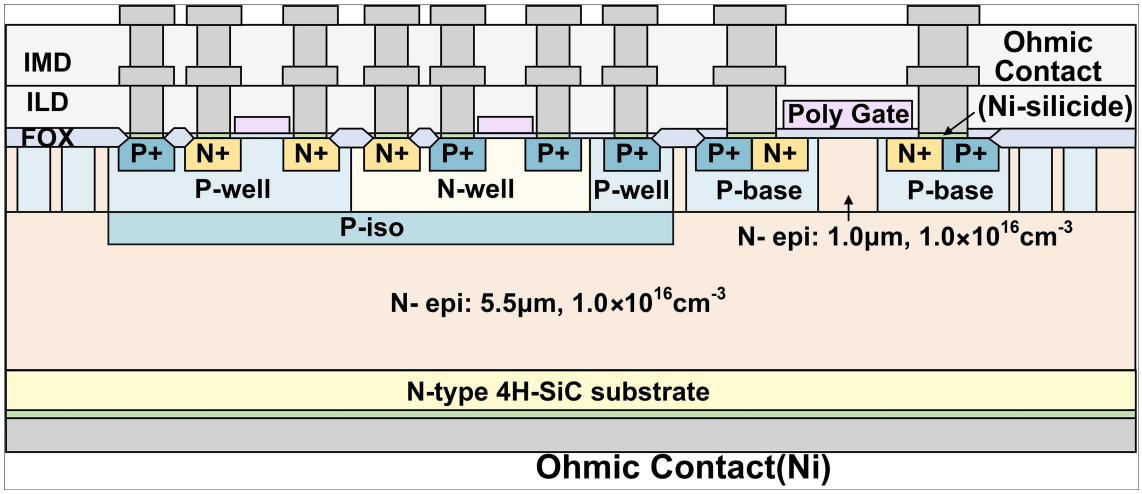


**Figure 21** (Color online) Schematic structure of the CMOS + VDMOSFET integrated circuits [115, 116].

**Table 5** Summary of MOSFET-based LV and vertical HV integration platform.

| | 2014 Wolfspeed | 2021 Taiwan Tsing Hua University | 2021 Hitachi | 2022 Taiwan Yang Ming Chiao Tung University |
|---|---|---|---|---|
| Refs. | [108] | [109] | [114] | [115, 116] |
| Epitaxial stack | N-sub/N-epi | N-sub/N-epi | N-sub/N-epi/ P-base/P-epi | N-sub/N-epi |
| $V_{\rm th}$ (NMOS) | – | 3.5 V (25°C) | 9.5 V | 1.5 V |
| $V_{\rm th}$ (PMOS) | – | −7.7 (25°C) | −6.8 V | −7 V |
| Minimum channel length | 1.5 μm | 2 μm | 1 μm | 0.8 μm |
| LV circuit | NMOS inverter | CMOS inverter, ring oscillator | CMOS inverter | Level shifter, 6-stage inverter gate driver |
| $BV$ (VDMOS) | – | 1200 V | 1200 V | 700 V |
| $R_{on,sp}$ (VDMOS) | 7 mΩ·cm$^2$ | – | – | 10 mΩ·cm$^2$ |
| $BV$ (isolation structure) | 1200 V | Severe body effect when $V_{sub}$ = 800 V | 1500 V | 800 V |

it is validated that higher voltage application can also be realized by the P-iso structure with lighter-doped and thicker epilayer. As shown in Table 5, the fabrication and performance details of vertical MOSFET-based integration research [108, 109, 114, 115] are compared, and the scheme in [114] is the most promising technology route in current vertical integration.

## 4 Technical challenges of MOSFET IC

As we established earlier, MOSFET-based integration platforms are expected to emerge as the dominant technology in the future considering the maturity of circuit design and fabrication processes. Thereby, this work will further explore key technical challenges in advancing MOSFET integration platforms, namely $V_{\rm th}$ matching between NMOS and PMOS devices and irradiation reliability.

### 4.1 Matching $V_{\rm th}$ of CMOS

The typical $V_{\rm th}$ observed in SiC PMOS tends to be higher than that of their NMOS counterparts, which can be explained with the $V_{\rm th}$ expression in (1). $\phi_{MS}$ represents the metal work function difference between SiC and polysilicon. $Q_{ox}$ encompasses charges such as mobile ions, fixed oxide charge, oxide trapped charge and interface trapped charge.

$$V_{\rm th} = \phi_{MS} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_A(2\phi_{Fp})}{C_{ox}} + 2\phi_{Fp}. \tag{1}$$

In (1), the first two terms are referred to as the flat-band voltage ($V_{FB}$) and are primarily responsible for the $V_{\rm th}$ mismatch between NMOS and PMOS devices.

On the one hand, the wider bandgap of SiC, relative to silicon, results in a significantly larger difference in the $\phi_{MS}$ of PMOS and NMOS devices when employing the same gate material (e.g., n-poly). This inherent difference in $\phi_{MS}$ directly translates to a greater absolute disparity in the $|V_{\rm th}|$ of NMOS and PMOS.

On the other hand, the interface trap density ($D_{it}$) at the SiC/$SiO_2$ interface ($10^{11}$–$10^{12}$ defects·$eV^{-1}$·$cm^{-2}$) is substantially higher than that at Si/$SiO_2$ interface ($10^{9}$–$10^{10}$ defects·$eV^{-1}$·$cm^{-2}$) [117]. This elevated $D_{it}$ contributes significantly to $Q_{ox}$ in (1), thereby exacerbating the imbalance between $V_{\rm th}$ (NMOS) and $V_{\rm th}$ (PMOS).

However, the design of CMOS digital integrated circuits fundamentally depends on the complementary characteristic of NMOS and PMOS. Mismatches in their $V_{\rm th}$ and current-driving capabilities can reduce noise margins and even introduce timing skew and glitches due to unbalanced turn-on conditions. Moreover, the excessively high $V_{\rm th}$ of PMOS makes it challenging to scale down the operating voltage level (e.g., from 10 to 5 V) of SiC CMOS circuits, thereby hindering the achievement of lower power consumption and higher integration density.

Primary pathways for improving NMOS and PMOS matching in integrated circuits are discussed as follows.

#### 4.1.1 *P-doped polysilicon*

Considering that electron mobility is higher than hole mobility in polysilicon, n-doped polysilicon is widely used in SiC CMOS technology. However, p-doped polysilicon is utilized specifically here to balance the $V_{\rm th}$ of NMOS and PMOS. It is identified that with p-doped polysilicon, the $V_{\rm th}$ of both NMOS and PMOS shifts in the forward direction [118], as shown in Table 6.

In (1), the expression of $\phi_{MS}$ is

$$\phi_{MS} = \frac{W_{Poly} - W_{SiC}}{q}. \tag{2}$$

$W_{Poly}$ and $W_{SiC}$ represent the work function of polysilicon and silicon carbide, respectively. The work function of p-doped polysilicon is higher than that of n-doped polysilicon (see Figure 22), thus shifting the $V_{\rm th}$ in the forward direction [119]. However, the adjustment range of $V_{\rm th}$ via this method is constrained by the bandgap of polysilicon, resulting in limited effectiveness.

#### 4.1.2 *Ultra-thin gate oxide*

In Hitachi's 2023 work, NMOS and PMOS with 8-nm gate oxide achieve satisfactory $V_{\rm th}$ matching, as shown in Table 6 [120]. This is because smaller oxide thickness leads to higher $C_{ox}$ in (1), which effectively lowers $V_{\rm th}$ (PMOS). However, this method imposes stringent requirements on process capability and thus cannot yet act as a universal approach.

#### 4.1.3 *Channel counter doping*

Channel counter doping may form a buried channel or accumulation channel, relying on the thickness of the compensated layer. Figure 23 illustrates the operating principle of a MOSFET with a buried channel [113]. Taking NMOS as an example, when $V_g$ is smaller than $V_{\rm th}$, a pinch-off happens between the depletion region of the MIS structure and the depletion region of the buried channel-bulk P-N junction, thereby turning off the MOSFET; see Figure 23(a). When $V_g$ exceeds $V_{\rm th}$, a neutral channel as Figure 23(b) exists between these two depletion regions, allowing the conductance of carriers here [121]. In this case, the conducting path is transferred from the surface to the bulk. As $V_g$ further increases, an accumulation-mode channel may form at the SiC/$SiO_2$ interface, as depicted in Figure 23(c). Additionally, counter doping can directly create a depletion-mode MOSFET with accumulation channels, where carrier mobility is limited by interface traps [122].

Typically, channel counter doping is realized through implantation. For NMOS, counter doping reduces $V_{\rm th}$ and enhances carrier mobility [113, 121–123], as interface scattering is mitigated with a conducting path transferred inside.

Whereas, this is not the case for PMOS. In APERC's 2012 work, $V_{\rm th}$ and channel mobility remain almost unchanged after $Al^+$ implantation in the channel region. This is attributed to the poor dopant activation rate and conducting ability of the PMOS neutral channel in this work. Later in 2019, Matthaeus Albrecht's team successfully reduces the $V_{\rm th}$ of PMOS through channel implantation [124]; see Table 6. More balanced CMOS characteristics increase the $V_{sp}$ of the inverter from 0.45 to 1.5 V, enabling the circuit to operate with a 5 V supply voltage up to 400°C. Also, in their further work, the operational amplifier's common-mode input range and open-loop gain are enhanced with improved NMOS/PMOS matching.

**Table 6** Summary of CMOS matching techniques. The units of $\mu_{fe}$, $V_{\rm th}$, and $T_{ox}$ are $\rm cm^2{\cdot}V^{-1}{\cdot}s^{-1}$, V, and nm, respectively. N stands for NMOS and P stands for PMOS. The subscripts 1 and 2 represent the characteristics of the original and improved devices, respectively. The data marked with an asterisk (*) are extracted from the figure. ESR stands for extrapolation in the saturation region, and ELR stands for extrapolation in the linear region. BC stands for buried channel (channel counter doping).

| Ref. | $V_{\rm th(N)1}$ | $V_{\rm th(N)2}$ | $\mu_{fe(N)1}$ | $\mu_{fe(N)2}$ | $V_{\rm th(P)1}$ | $V_{\rm th(P)2}$ | $\mu_{fe(P)1}$ | $\mu_{fe(P)2}$ | Epi stack | $T_{ox}$ | $V_{\rm th}$ extraction method | $V_{\rm th}$ adjustment method |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [114] | 9.5 | – | 15.8 | – | −17.4 | −9.3–−6.8 | 7.7 | 11 | N-sub/P-epi | – | – | EBC |
| [118] | 2.44 | 3.03 | – | – | −6.57 | −5.77 | – | – | N-sub/P-epi | – | ESR | P-doped polysilicon ultra-thin gate oxide |
| [120] | – | 2.6 | – | 18.2 | – | -2.4 | – | 2.12 | N-sub/N-epi | 8 | – | |
| [113] | 15* | 0.3* | 1.5 | 68 | −7.5* | −7.5* | 15 | 14* | N-epi for PMOS; P-epi for NMOS | 45 | ELR | BC |
| [122] | 1.8 | 0.3 | 45 | 140 | – | – | – | – | P-epi | 40 | ESR | BC |
| [123] | 6* | 3* | 2 | 20 | – | – | – | – | N-sub/P-epi | 36 | ESR | BC |
| [124] | – | 1.4 | – | 21 | −5 | −3.6 | 11.8 | 10.2 | N-sub/N-epi | 30 | – | BC & retrograde P-well |
| [125] | – | – | – | – | −5.5* | −5* | 15* | 15* | N-epi for original device; P-epi for improved device | 42 | – | retrograde N-well on P-epi |

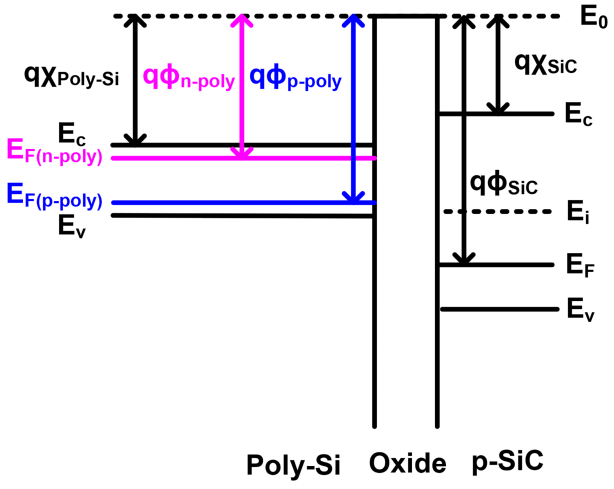


**Figure 22** (Color online) Energy band diagram of a system comprising N+/P+ poly gate, oxide layer and SiC.

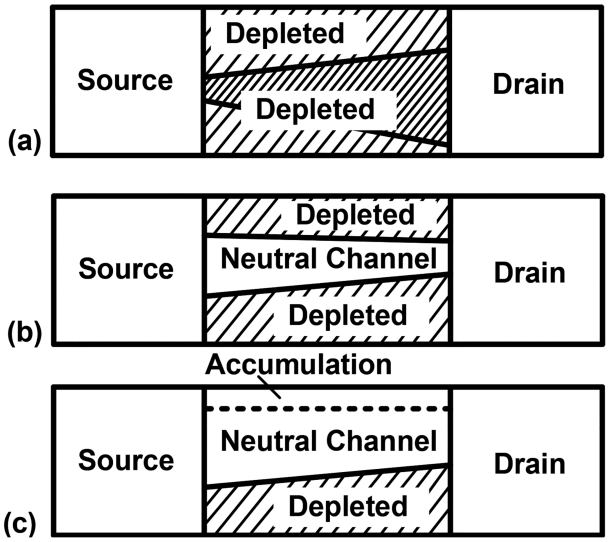


**Figure 23** Schematic diagram of the buried-channel MOSFET at different gate biases: (a) off-state, (b) conduction in the buried channel layer away from the MOS interface, and (c) conduction through the accumulated layer parallel to the buried channel layer.

However, the channel mobility is slightly reduced after channel implantation due to interface states and fixed charges induced by $Al^+$ implantation process [124]. Therefore, as we mentioned before in Section 3, APERC's work adopts an EBC process, where epitaxial growth replaces implantation to realize channel counter doping, avoiding the damage caused by ion bombardment. Both $V_{\rm th}$ and channel mobility of PMOS are improved in this work, at the cost of process complexity [114].

Another approach of PMOS counter doping employs a retrograde N-well formation through a single $N^{2+}$ high-energy implantation; thus n-doping is performed in regions outside the channel area. $V_{\rm th}$ and mobility of PMOS comparable to those on N-epitaxy were successfully achieved on P-epitaxy through this method [125]; see Table 6. A similar retrograde P-well formed through multiple $Al^+$ implantation for NMOS is also applied in [124].

The above discussion involves only intrinsic CMOS mismatch arising from the definition of $V_{\rm th}$. When integrating HV and LV devices into the same process platform, the challenge in achieving matching $V_{\rm th}$ lies in the contradictory relationship between reducing the $V_{\rm th}$ of PMOS and realizing outstanding isolation between HV and LV regions. Although the N-epi/N-sub stack enables favorable $V_{\rm th}$ matching (see Table 6), it suffers from higher complexity in achieving isolation of HV to LV regions. Conversely, the P-epi/N-sub stack affords significantly simpler high-to-low voltage isolation, but it inevitably exhibits elevated PMOS $V_{\rm th}$ due to the high concentration of doped Nitrogen in the background doping of P-type epitaxial layer growth [126] and the consequent requirement for compensatory high-dose N-well implantation for PMOS.

In order to eliminate this conflict, a 4H-SiC integration process platform with novel architectures is proposed in this paper, which features an N-epi/P-epi/P-buffer/N-sub stack and isolation structure (shown in Figure 24). Optimizing the $V_{\rm th}$ of PMOS can be efficiently achieved through N-epitaxial implementation, which reduces channel doping concentration to $1 \times 10^{25}$ $\rm cm^{-3}$ and delivers a 37.8% $V_{\rm th}$ reduction for PMOS, as shown in Figure 25(a). For the isolation between HV and LV regions, an N-epi/P-epi/N-sub stack and P-type isolation trenches extending into the P-epi layer are adopted. This novel configuration simultaneously achieves 215 V punch-through voltage ($PTV$) and 1351 V isolation breakdown voltage ($BV_{iso}$), as validated in Figures 25(b) and (c). Consequently, the architecture successfully reconciles CMOS $V_{\rm th}$ matching with robust HV/LV isolation, enabling critical advances in high-voltage SiC integrated circuit development.

### 4.2 Radiation reliability

The wide bandgap of SiC confers inherent resistance to impact ionization under radiation, positioning SiC ICs as a highly promising technology for radiation-hardened applications. Among various SiC device platforms, SiC MOS ICs are generally favored for circuit design, owing to the design convenience offered by their voltage-controlled operation and mature complementary compatibility. However, the gate oxide in SiC MOSFETs presents a unique sensitivity to radiation. Therefore, gaining a definitive understanding of the radiation response of SiC MOSFET-

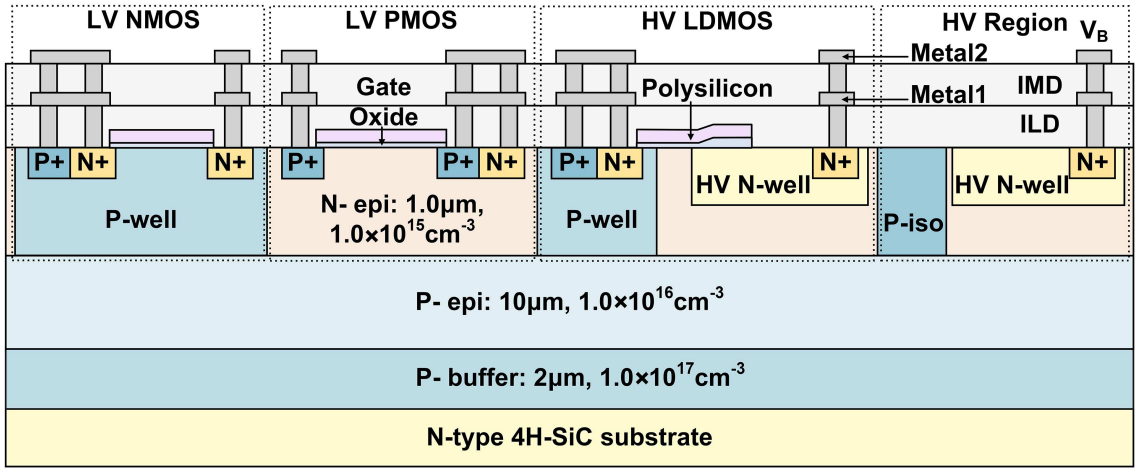


**Figure 24** (Color online) Schematic cross-section of the proposed all-SiC integration process platform with multiple epitaxy layers and isolation wells.

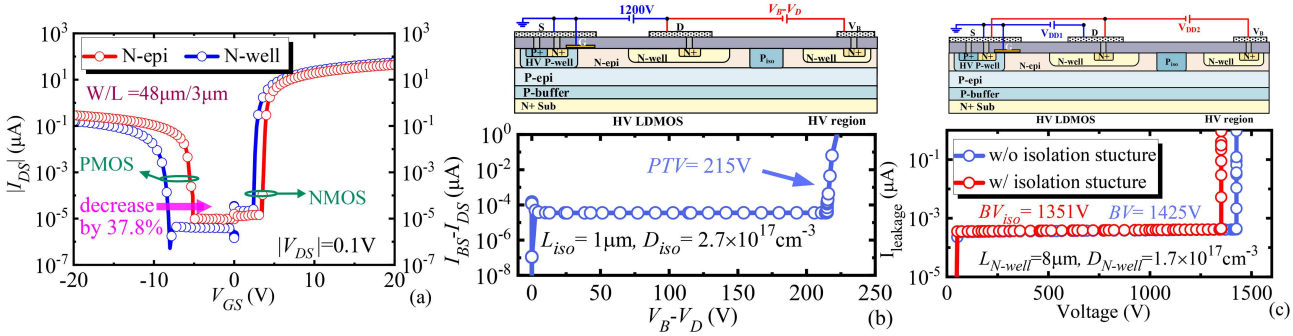


**Figure 25** (Color online) (a) Transfer characteristic curves of NMOS and PMOS. Simulated results of (b) the $PTV$ and (c) the $BV_{iso}$.

based ICs is of critical importance. Primary failure mechanisms of SiC integrated circuits under TID irradiation are shown as follows.

(1) $V_{\rm th}$ shift and mobility degradation: Radiation-induced negative $V_{\rm th}$ shifts ($\Delta V_{\rm th}$) and deterioration of mobility in pMOSFETs, resulting in degradation of circuit gain and output range [6, 87].

(2) Leakage current: Parasitic transistor activation is due to charge accumulation in field oxide layers or inversion-layer electron leakage paths under polysilicon gates and VDD metal layers on P-epitaxial surfaces, leading to functional degradation in logic circuits; see Figure 26(a) [88].

To address the degradation caused by mechanism (1), thin gate oxide and interface optimization are implemented. Thin gate oxide layers (25 nm [87] and 8 nm [6]) mitigate $\Delta V_{\rm th}$, combined with NO passivation to suppress interface trap generation. For mechanism (2), field plates connected to p+ isolation regions are proposed to alleviate electric fields in field oxide layers [87]. Additionally, floating p+ ion implantation structure is introduced to block leakage paths [6]; see Figure 26(b) [82].

For single-event irradiation, its mechanism involves radiation-generated electron-hole pairs that, under applied bias, undergo directional drift to elevate leakage current. Increased leakage current subsequently triggers parasitic transistor activation, culminating in destructive latch-up. A 3-step mechanism of single-event burnout (SEB) effect for a SiC inverter is discussed in Figure 27(a). After irradiation, leakage paths shown in step 2 are introduced, which finally bring about parasitic latch-up with the topology illustrated in step 3 [89]. For SEB effect suppression, a novel structure incorporating floating N+ rings and P+ stripes is implemented as shown in Figure 27(b). This design prevents activation of parasitic NPN/PNP transistors while effectively blocking leakage current paths [90].

### 4.3 Other challenges and development directions for SiC integration

Beyond threshold-voltage stability and radiation-related issues, several additional challenges are central to practical SiC integration platforms. These include (i) high-temperature BEOL/interconnect and packaging limits (metallization stability, diffusion, dielectric reliability), (ii) ohmic contacts and dopant activation, particularly for P-type

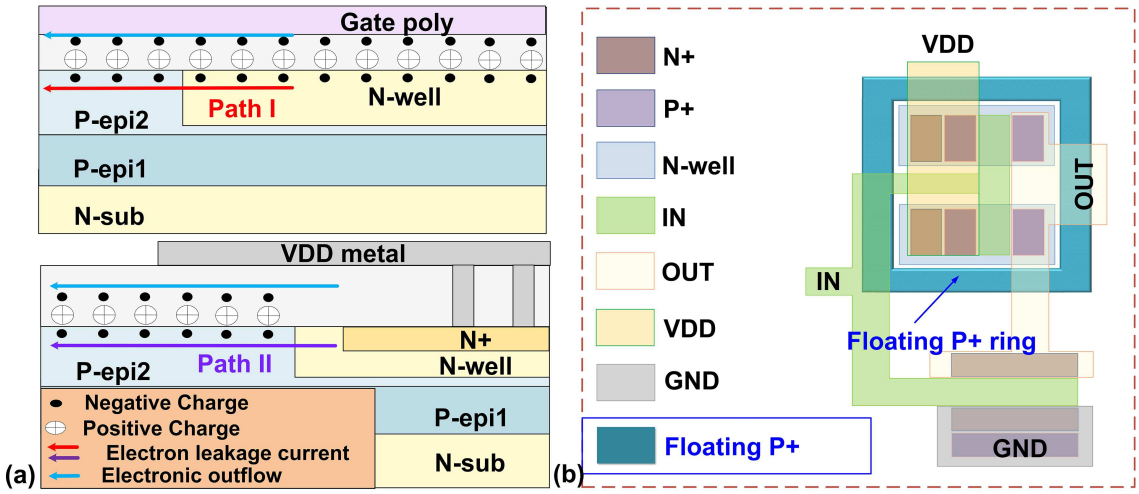


**Figure 26** (Color online) (a) Two leakage paths induced by positive charge in inverter; (b) TID reinforced inverter.

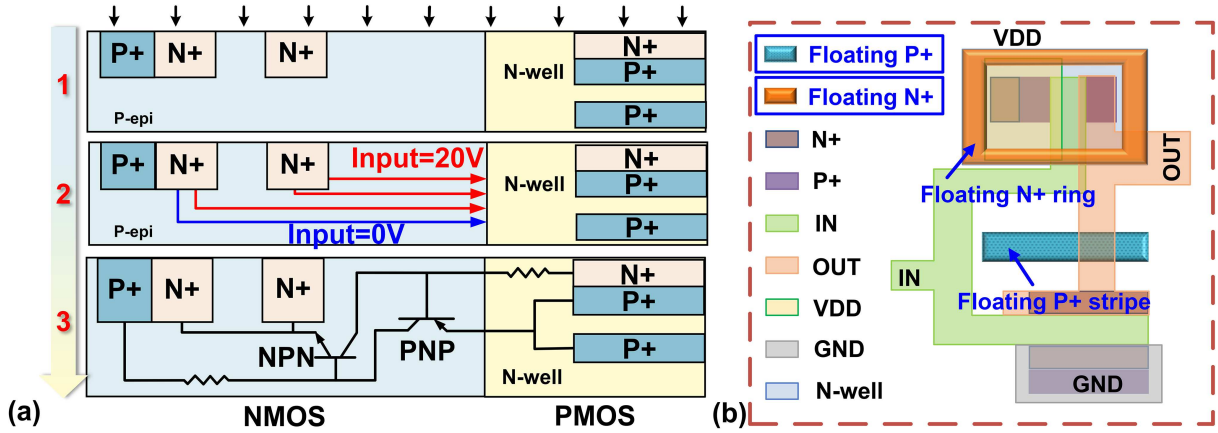


**Figure 27** (Color online) (a) The 3-step mechanism of the SEB effect for the inverter; (b) SEB-reinforced inverter.

regions, with stable low contact resistance over temperature, (iii) device isolation and parasitic effects for power IC integration (deep isolation, edge termination area overhead, and latch-up/parasitic conduction mitigation), (iv) process variability and yield (epi uniformity, defectivity, parameter spread, and manufacturable process windows), (v) electro-thermal coupling and hot-spot management under high power density, and (vi) design enablement, including accurate compact models, temperature-aware PDKs, and layout rules for reliable circuit design. Correspondingly, the main development directions are toward (a) more manufacturable SiC CMOS/BCD platforms with balanced n/p devices, (b) improved gate-stack/interface engineering and reliability screening, (c) scalable deep isolation/termination modules compatible with cost targets, and (d) a mature modeling/PDK/design ecosystem to accelerate complex mixed-signal and power-control IC integration.

## 5 Conclusion

This work systematically reviews the evolution and current status of SiC IC platforms, covering both LV ICs and power ICs. It delineates the specific technical challenges of BJT, JFET, and MOSFET technologies, along with the drivers for inter-device iteration, ultimately establishing MOSFET-based platforms as the most promising. Furthermore, pivotal technical challenges in scaling MOSFET-based platforms are investigated, namely $V_{\mathrm{th}}$ matching between NMOS and PMOS and radiation reliability issues.

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