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Recent advances in ultralow-power and high-gain technologies based on subthreshold Schottky-barrier thin-film transistors

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Abstract Ultralow-power thin-film electronics are increasingly needed for wearable, implantable, and distributed sensing systems, where devices must operate with minimal energy while providing reliable signal amplification. This review aims to clarify how subthreshold Schottky-barrier thin-film transistors can meet these requirements and how the field has evolved across different material and fabrication platforms. We summarize recent progress in oxide, organic, and two-dimensional semiconductor devices, compare their key electrical characteristics, and examine representative circuit demonstrations for amplification and biosensing. Studies show that operating these transistors close to the off state can greatly reduce static power consumption while preserving high gain and stable current control, making them attractive for flexible and biointegrated systems. However, device variability, contact reproducibility, printing accuracy, and long-term operational stability remain barriers, albeit surmountable, to large-scale use. We conclude that further advances in material design, hybrid manufacturing, circuit architecture, and biocompatible integration will be essential for translating this device concept into practical post-Moore sensing technologies.

Keywords Schottky barrier, thin-film transistors, ultralow-power consumption, high-gain amplification, flexible bioelectronics

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1 Introduction

With the rapid development of wearable electronics, the Internet of Things (IoT), and implantable devices, there is an increasing demand for devices suitable for large-scale deployment, particularly with low power consumption, large-area integration, flexibility, and biocompatibility. Unlike conventional thin-film transistors (TFTs), primarily used as pixel switches in display backplanes, emerging systems often need to operate on deformable substrates, in proximity to soft biological tissue, or under constrained power and thermal budgets. These systems are required to detect weak physiological, chemical, or environmental signals. Consequently, devices must simultaneously achieve low-voltage operation, ultra-low static power consumption, sufficient analog gain, mechanical compliance, and large-area manufacturability [1–6]. In implantable systems, these requirements become even more stringent, as devices must also satisfy additional constraints on miniaturization, wireless communication, and long-term reliability [7–13]. TFTs are therefore well-suited for such applications [14], as they can be fabricated uniformly over glass, plastic, and other unconventional substrates at relatively low processing temperatures and costs [4]. More importantly, TFTs are not limited to a single semiconductor material system. Oxide semiconductors, organic semiconductors, and emerging low-dimensional semiconductors each offer distinct trade-offs in terms of mobility, leakage current, optical transparency, solution processability, mechanical flexibility, and low-temperature fabrication. Amorphous oxide semiconductors, exemplified by indium gallium zinc oxide (IGZO), have enabled transparent flexible TFTs applicable to scenarios that are challenging for conventional silicon-based electronics [15–17]. Organic TFTs excel in solution processability and mechanical flexibility, yet their non-ideal charge transport, contact effects, and disorder-induced parameter variations remain significant challenges [18]. Despite their compatibility with flexible electronics and large-area manufacturing platforms, conventional TFT operation exhibits certain limitations in

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weak-signal front-end circuits. Achieving ultra-low static power requires devices with low leakage and operating currents, while high-gain amplification depends on how large are the transconductance and output resistance. In typical TFTs, power consumption, gain, bias conditions, and device geometry are strongly coupled, making simultaneous optimization challenging. Moreover, high-mobility oxide TFTs can suffer from bias stress-induced instability and defect-related threshold voltage shifts, further constraining their application in long-term low-power sensing circuits [19].

Schottky-barrier thin-film transistors (SB-TFTs) provide an alternative device-design strategy for addressing the aforementioned limitations of conventional TFTs in low-power analog front-end circuits. Unlike conventional TFTs, in which the drain current is mainly controlled by modulation of the channel conductance, the operation of SB-TFTs strongly relies on gate-controlled carrier injection at the source Schottky barrier. In the near-off state or deep-subthreshold regime, the source barrier can effectively suppress the standby current. Under appropriate bias conditions, however, gate-induced modulation of the barrier width, local band bending near the metal/semiconductor interface, and carrier transmission probability can enable effective signal amplification at very low current levels. As a result, when the device operates in a contact-injection-limited regime, SB-TFTs can potentially exhibit high output resistance, high intrinsic gain, and reduced dependence on channel geometry. These characteristics make them attractive candidates for low-power analog front-end circuits. In recent years, preliminary progress has been made in SB-TFTs based on oxide, organic, and two-dimensional (2D) semiconductor platforms. Early studies on IGZO SB-TFTs demonstrated that in amorphous oxide semiconductors, ultralow power consumption and high intrinsic gain can be achieved through source Schottky barrier engineering and gate-modulated carrier injection, while maintaining compatibility with large-area oxide TFT technologies. Subsequently, printed organic SB-TFTs extended this concept to solution-processable and mechanically flexible electronics, indicating that printed devices can also potentially achieve high gain and ultralow power operation. This is particularly significant because printed electronics often suffer from device-to-device dimensional variations and process-induced nonuniformity, making a channel-geometry-insensitive operating mechanism highly valuable. In recent years, monolayer MoS_2 subthreshold Schottky-barrier transistors have demonstrated that 2D materials can exploit source Schottky barrier engineering for injection-controlled operation. The atomically thin channel provides strong electrostatic control, suggesting potential value of this device concept for short-channel, low-power device design [20–22]. These material systems should not be interpreted as a simple hierarchy of performance, but rather as complementary platforms for different device-design requirements.

As illustrated in Figure 1, oxide-based SB-TFTs inherit the full technical maturity of the mainstream industrial oxide TFT platform, and inherently deliver ultralow off-state leakage, exceptional across-panel electrical uniformity, native optical transparency, and full process compatibility with existing large-area display manufacturing lines. These inherent advantages collectively enable good uniformity, highly repeatable large-area fabrication yield, and substantially higher technology readiness level for practical system integration. Notwithstanding these merits, bias-stress-induced threshold voltage drift and localized trap-related instability still remain as core technical concerns that require targeted mitigation for long-term continuous operation [19, 20]. Printed organic SB-TFTs feature inherent advantages in solution-processable printing, low-temperature fabrication, exceptional mechanical flexibility, and conformable biosignal acquisition, making them highly suitable for low-cost, large-area flexible electronics and wearable health monitoring scenarios. However, their device variability, operational reliability, and long-term stability remain strongly sensitive to active-layer morphological uniformity, printing process precision, and Schottky contact interface consistency. While these properties render printed organic SB-TFTs uniquely competitive for emerging flexible and conformal application paradigms, their widespread industrial deployment still demands systematic, iterative optimization of printing protocols and interface engineering strategies [18, 21]. In sharp contrast, SB-TFTs built on 2D semiconductors are defined by their atomically thin channel geometry, exceptional electrostatic gate control, intrinsic short-channel scaling capability, and highly tunable Schottky contact engineering, which collectively enable unprecedented source-barrier modulation efficiency in deeply scaled short-channel device architectures. Nevertheless, ubiquitous atomic-scale lattice defects, spatially inhomogeneous metal-semiconductor interfaces, and extreme environmental susceptibility still impose fundamental constrains on device batch-to-batch reproducibility and long-term operational stability, rendering their wafer-scale practical integration far less mature than their oxide and organic counterparts at the current stage of development [22].

This review focuses on recent advances in ultralow-power and high-gain technologies based on SB-TFTs, with an emphasis on their device characteristics, fabrication strategies, and potential applications. We systematically compare different SB-TFT in terms of performance metrics and process-related advantages, and further discuss their prospects in emerging fields such as biosensing, wearable, and implantable systems, including printed flexible electronics. First, the fundamental operating principles of SB-TFTs are introduced, followed by a comparison of key performance parameters across different material platforms. Subsequently, circuit-level applications and

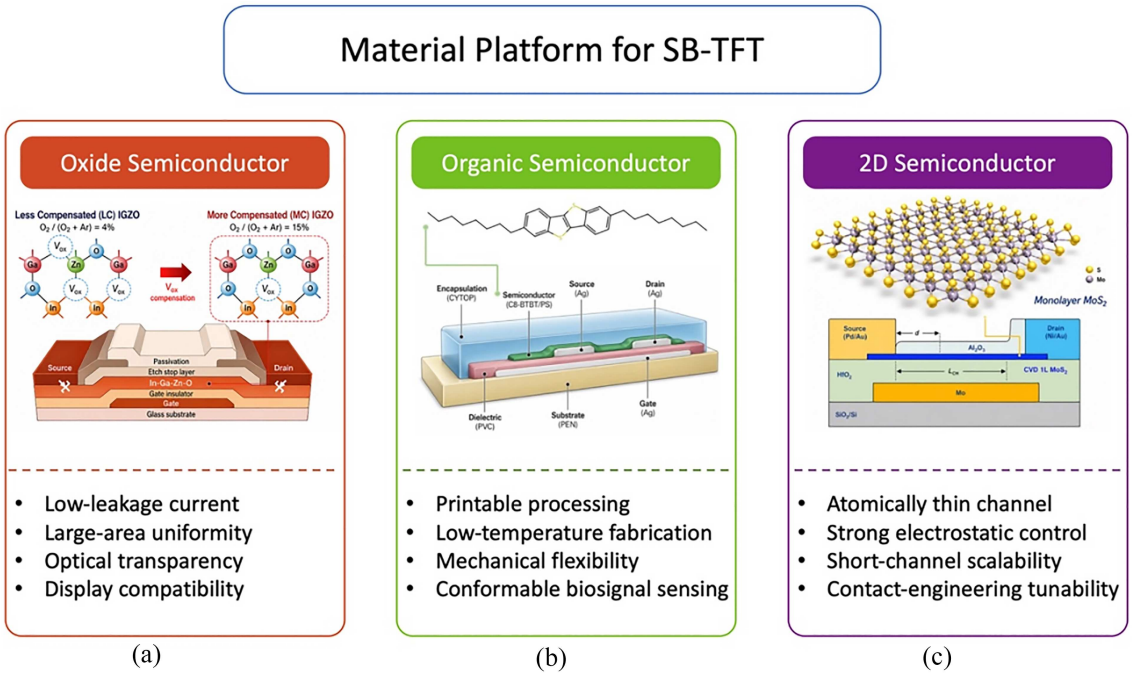

Figure 1 (Color online) Material platforms for Schottky-barrier thin-film transistors (SB-TFTs). Representative device concepts based on (a) oxide semiconductors, (b) organic semiconductors, and (c) two-dimensional (2D) semiconductors, illustrating the three major material routes for developing SB-TFTs. This figure is adapted from [20–22].

representative demonstrations of SB-TFTs are summarized, with an emphasis on their advantages for system integration. The current challenges facing SB-TFT technology are then examined, particularly the oxide and organic semiconductor platforms. Finally, promising directions for future research are discussed and recommended.

2 Fundamental operating principles of deep subthreshold SB-TFT

2.1 Device structure and conduction mechanism

In conventional TFTs, an ohmic contact between the semiconductor and the source/drain electrode is typically required to achieve efficient current driving and an ideal linear operation region [23, 24]. Ohmic contacts minimize contact resistance, ensuring high-performance operation in the active region. In a metal-semiconductor contact, when the metal work function φ_M is larger than the semiconductor electron affinity χ_s, electrons transfer from the semiconductor to the metal. This induces a depletion layer and band bending at the interface, giving rise to a Schottky barrier $\varphi_{B0} = \varphi_M - \chi_s$. This barrier hinders electron injection from the metal into the semiconductor. For conventional TFTs, this barrier leads to higher contact resistance, restricted current drivability, poorer transconductance and frequency response. However, Lee et al. [20] took the opposite approach in their study by exploiting Schottky barrier in oxide TFTs. They deposited an IGZO active layer using sputtering under a high oxygen partial pressure, effectively compensating oxygen vacancy defects and shifting the Fermi level downwards. This achieved Schottky contacts with the source/drain electrodes. Biasing the devices in the deep subthreshold regime (near the off state) yielded an ultra-low static power consumption below 1 nW, an intrinsic gain exceeding 400 that is independent of bias and channel length, and inherent immunity to short-channel effects. This groundbreaking work shows that Schottky contacts are not a hindrance but rather a key enabler for building high-performance, ultra-low-power transistors.

The current conduction mechanism of SB-TFTs can be elucidated by analyzing the energy band diagrams of the source Schottky junction under different gate voltages. Figures 2(a) and (b) show the band diagrams of a SB-TFT at a given gate-to-source voltage ($V_{\rm GS}$) under different drain-to-source voltage ($V_{\rm DS}$) with respect to the transition voltage ($V_{\rm tran}$). When $V_{\rm DS} < V_{\rm tran}$, there is a relatively high Schottky barrier at the drain junction (Figure 2(a)). Electron collection from the semiconductor into the metal is primarily governed by thermionic emission (TE), and only a few high-energy electrons are capable of surmounting the barrier into the conduction band. Thermionic field emission (TFE) is negligible due to the wide depletion region. When $V_{\rm DS} > V_{\rm tran}$, the drain current ($I_{\rm DS}$) becomes

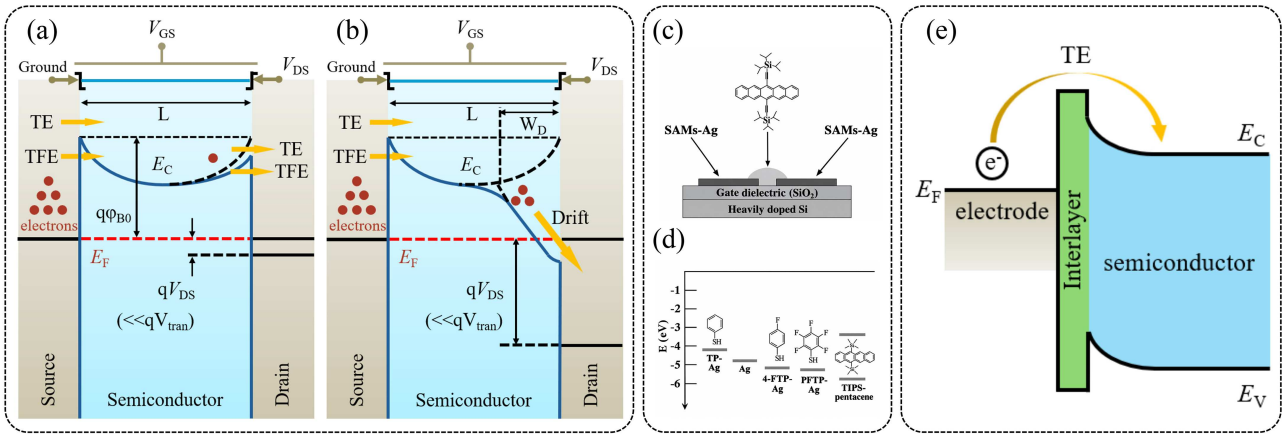

Figure 2 (Color online) Band diagram of a Schottky-barrier thin-film transistor (SB-TFT) when (a) $V_{DS} < V_{tran}$ and (b) $V_{DS} > V_{tran}$. Here V_{DS} and V_{tran} denote the drain-to-source voltage and the transition voltage, respectively. (c) Geometry of a bottom-contact organic thin-film transistor (OTFT) with TIPS-pentacene as the active layer. (d) Energy level alignment of TP-Ag, pristine Ag, 4-FTP-Ag, PFTP-Ag electrode, and TIPS-pentacene. (e) Band diagram of a metal-barrier interlayer-semiconductor (MBIS) junction. This figure is adapted from [25].

firmly saturated because of the reverse-biased Schottky diode at the source (Figure 2(b)). This regime satisfies the condition of $L \gg W_D$ (with L the channel length and W_D the depletion width at the drain), suggesting a negligible image-charge effect from the drain to source. Thus, the Schottky barrier lowering at the source is mainly a function of V_{GS} modulating the current density. The current rises exponentially with V_{GS}, enabling a rapid transition from the off state to the on state. Operating in the deep near-off regime, the SB-TFT leverages its source Schottky barrier to suppress channel current and realize ultra-low power consumption. The Schottky barrier fully screens drain voltage perturbations, pushing output resistance $r_0 = \partial V_{DS}/\partial I_{DS}$ to near-infinity, while transconductance g_m scales exponentially with V_{GS} in the subthreshold regime. The two exponential terms cancel out in their product, making intrinsic gain $A_i = g_m \cdot r_0$ entirely gate-bias independent and determined solely by fundamental material parameters. This yields an ultra-high, operation-stable intrinsic gain unachievable in conventional ohmic-contact TFTs. While state-of-the-art conventional oxide TFTs have indeed delivered an ultra-low off-state current, their standard ohmic source/drain contacts impose a limitation on high-gain performance. The relatively small barrier height and width allow drain voltage perturbations to influence channel characteristics, resulting in monotonic increase in off-state current with drain bias. This suppresses the intrinsic output resistance r_0 in the saturation regime.

2.2 Material engineering for optimal Schottky contacts

Achieving stable, tunable, and near-ideal Schottky contacts is the key to the excellent performance of SB-TFTs. The barrier height often deviates from the Schottky-Mott prediction because of unavoidable interface defect states and Fermi-level pinning [26–28]. To address this, researchers have developed a variety of material engineering strategies to control the height and uniformity of the Schottky barrier, such as oxygen vacancy engineering, self-assembled monolayer (SAM) modification, and insertion of a wide-bandgap interlayer. These three strategies will be discussed separately in the following.

2.2.1 *Oxygen vacancy engineering*

In oxide semiconductors (e.g., In_2O_3, ZnO, and IGZO), oxygen vacancies act as the dominant shallow donor defects, and their concentration directly determines the carrier concentration and the position of the Femi level. A high oxygen vacancy concentration leads to a high electron concentration and a Fermi level close to the conduction band minimum, which makes ohmic contact formation easy. In contrast, a reduced oxygen vacancy concentration results in a significantly lower electron concentration and a Fermi level that shifts downward the intrinsic level, which favors Schottky barrier formation. Tuning the oxygen vacancy concentration therefore switches the contact type between the electrode and the oxide semiconductor, offering a simple route to Schottky-barrier TFTs that does not rely on metal work function. Lee and Nathan compensated oxygen vacancies by using high oxygen partial pressure during IGZO sputtering, forming Schottky source/drain contacts that yielded ultra-low power consumption and extremely high gain [20]. Huang et al. [29] stacked atomic-layer deposition (ALD) and sputtered IGZO to significantly reduce the vacancy concentration, achieving SB-TFT with very low saturation voltage and high field-effect mobility.

However, this approach is only applicable to oxide systems. Although the process is simple and compatible with conventional TFT fabrication, precisely controlling the oxygen vacancy concentration remains a challenge. Moreover, oxygen vacancies have been demonstrated to be mobile within the semiconductor, and therefore the long-term stability of this strategy still needs to be verified.

2.2.2 *SAM modification*

In organic thin-film transistors (OTFT), SAM modification of electrodes is an effective strategy for tuning the anchoring properties. As shown in Figures 2(c) and (d), SAM molecules with appropriate anchoring groups can stably absorb onto the electrode (Ag) surface, forming a uniform and ordered SAM structure [25]. The terminal functional groups of the SAM, which possess strong electronegativity, generate a dipole pointing from the metal toward the semiconductor, thereby increasing the effective work function of the metal, reducing the injection barrier for majority carriers, and increasing that for minority carriers. The introduction of the SAM layer can also modify the electrode surface energy, optimizing the crystallization behavior of the organic semiconductor. Han et al. [30] used 3-fluoro-4-methoxythiophenol SAM to modify gold electrodes in OTFTs. The strong dipole moment of the SAM increased the metal work function, effectively suppressed minority carrier injection for low leakage and stable operation, while not affecting majority carrier injection. Zhong et al. [31] employed fluorinated silane to modify ITO electrodes in transparent OTFTs, raising the ITO work function from 4.61 to 5.13 eV, which closely approaches the HOMO level of IDT-BT (5.1 eV). The contact resistance dropped from >1 MΩ to <100 kΩ, and the mobility improved by an order of magnitude.

SAM modification is an interface engineering strategy that tunes the metal work function, thereby effectively suppressing minority carrier injection, lowering contact resistance, and enhancing mobility. However, SAM molecules are susceptible to oxidation, desorption and molecular rearrangement, all of which lead to long-term instability. Moreover, the process is highly sensitive to metal-surface cleanliness and uniformity, resulting in poor reproducibility and non-uniform contact properties.

2.2.3 *Insertion of a wide-bandgap interlayer*

Inserting an atomically thin wide-bandgap material between the metal and the semiconductor is another effective strategy for tuning the Schottky barrier. As shown in Figure 2(e), the wide-bandgap material itself possesses a high conduction-band minimum or valence-band maximum, forming a metal-barrier interlayer-semiconductor (MBIS) structure upon insertion. The series barrier effectively raises the total effective barrier height and widens the barrier width, thereby suppressing off-state current and increasing the output resistance. Furthermore, the interlayer prevents direct contact between the metal and the semiconductor, avoiding damage to the semiconductor channel from high-energy particles or chemical reagents, and it also reduces the formation of interface dangling bonds and defect states, thus suppressing Fermi-level pinning. Wang et al. [32] used a ∼4 nm-thick Ga_2O_3 layer, naturally oxidized on the surface of eutectic gallium-indium (EGaIn) liquid metal electrodes, as a barrier insertion layer to construct an MBIS junction. This Ga_2O_3 layer not only increased the barrier height but also achieved an atomically sharp interface via van der Waals contact, raising the intrinsic gain from ∼10 to 1000 [32]. Li et al. [33] employed an AlO_x insertion layer in IGZO SB-TFT. By controlling the AlO_x thickness, they increased the Schottky barrier of the Cu/IGZO contact from 0.61 to 0.85 eV. Combined with a source hybrid contact design, the saturation current was two orders of magnitude higher than that of a pure Schottky barrier device, and an intrinsic gain exceeding 1500 was achieved at a gate voltage of 10 V.

The insertion of a wide-bandgap interlayer is accompanied by several critical challenges. The most stringent requirement is the precise control of its thickness. An overly thin interlayer tends to suffer from incomplete coverage and pinholes, failing to establish an effective barrier or suppress Fermi-level pinning, and thus the off-state leakage remains inadequately blocked. Conversely, an overly thick interlayer exponentially reduces the carrier tunneling probability, causing a sharp drop in on-state current and severely degraded drive capability.

2.3 Comparative analysis of device performance

Table 1 summarizes key performance parameters of SB-TFTs, including oxide (In_2O_3, IGZO), organic (C_8-BTBT) and 2D material (MoS_2). All n-type devices exhibit positive threshold voltage (e.g., (2.1±1.9) V for In_2O_3, ∼2 and ∼1.6 V for IGZO, and 0.9 V for MoS_2), in clear contrast to the negative threshold voltage typically found in ohmic-contact n-type TFTs, demonstrating that the Schottky contact shifts threshold voltage in the positive direction. Where operating voltage is reported, they are consistently lower than the threshold voltage (e.g., <2 V for In_2O_3 and <1 V for IGZO), confirming deep-subthreshold operation, a regime that conventional ohmic-contact

Table 1 Summary of key performance parameters of SB-TFTs with different channel materials.

Channel material	V_{th} (V)	Operating voltage (V)	SS (mV/dec)	Intrinsic gain	Power consumption	Reference
In_2O_3	2.1±1.9	<2	102	792	46.3 μW/cm^2	[34]
IGZO	∼2	–	–	1562	–	[33]
IGZO	∼1.6	<1	280	∼450	<1 nW	[20]
C_8-BTBT	−0.01	–	60.2	∼1100	<1 nW	[21]
C_8-BTBT	–	–	84.2	13500	–	[35]
MoS_2	0.9	–	70	>2400	0.17 nW	[22]

TFTs cannot access. The subthreshold swing is remarkably small: 102 mV/dec for IGZO, 60.2 and 84.2 mV/dec for C_8-BTBT and 70 mV/dec for MoS_2, with some approaching the theoretical limit and reflecting steep switching. The most significant advantages over ohmic-contact TFTs appear in intrinsic gain and power consumption. The intrinsic gain of SB-TFTs is two to three orders of magnitude higher than that of ohmic-contact TFTs, while their power consumption is at the nanowatt level, far below that of ohmic-contact TFTs. These results clearly demonstrate that the advantages for ultralow-power, high-gain analog applications.

3 Circuit-level applications and demonstrations

3.1 Display circuits and high-gain amplifier circuit

3.1.1 *AMOLED pixel driving circuit*

The uniformity of active-matrix organic light-emitting diode (AMOLED) displays critically depends on the threshold-voltage stability of the driving transistor. Huang et al. [36] revealed that IGZO source-gated transistors (SGTs) are much less sensitive to variations in trap states within the channel layer than conventional IGZO TFTs. When the tail-state density was varied, the maximum threshold-voltage shift of the IGZO SGT was only approximately 15% of that observed in the conventional IGZO TFT, thereby maintaining stable OLED luminance. This work demonstrates that the incorporation of IGZO SGTs into AMOLED pixel circuits is a promising strategy for improving display uniformity. Drury et al. [37] further investigated, through simulation, the influence of source-gate overlap capacitance in SGTs on current-mode pixel driver circuits. As shown in Figure 3, unlike conventional TFTs, SGTs can achieve an appropriate balance between drive current and dynamic response when a deliberate source-gate overlap of approximately 5–10 μm is introduced. Moreover, this overlap capacitance can serve as part of the pixel storage capacitance and therefore does not significantly increase the overall pixel area, while also providing enhanced tolerance to geometrical process variations. Further advances in pixel architecture include the development of a 4T1M2C AMOLED pixel circuit based on a multimodal transistor (MMT). By exploiting the dual functionality of the MMT as both an analog driving element and a digital switching device, the circuit enables threshold-voltage compensation, low-power operation, and improved display uniformity. This work creatively applies MMTs to AMOLED driving circuits and reduces the required number of TFTs. Nevertheless, the circuit still faces challenges such as relatively high leakage current and limited stability at low gray levels. Even so, it provides a valuable research direction for future flexible display technologies [38].

3.1.2 *High-gain amplifier circuit*

Although high voltage gain in conventional large-area thin-film electronics typically requires complex multistage cascades or carefully biased circuits, recent studies have shown that unipolar SGTs can achieve high gain with simplified circuit designs. For example, a polysilicon common-source amplifier using SGTs and a zero-V_{GS} active load achieved a gain of 49 dB in a compact two-transistor configuration, and this concept was further extended to current mirrors, temperature-tunable circuits, and pressure/pulse sensing applications [39, 40]. These results highlight the advantages of SGTs for low-complexity analog circuits, although relatively high supply voltages and limited bandwidth remain key challenges.

Therefore, optimizing low-voltage operation, gain, and stability through device-structure design and contact engineering is essential for advancing SGT/TFT analog circuits. Current efforts can be broadly categorized into source-barrier engineering and contact-interface engineering [41]. The former reduces output conductance and improves gain and uniformity by modulating the source Schottky barrier and local electric field. For instance, Hemmi introduced a field-plate structure into printed organic SGTs, achieving a single-stage gain of 700 V/V, although low-voltage weak-signal amplification remains limited [42]. Sporea et al. [43] transformed polysilicon TFTs into source-contact-controlled devices through contact-barrier engineering, thereby improving device uniformity.

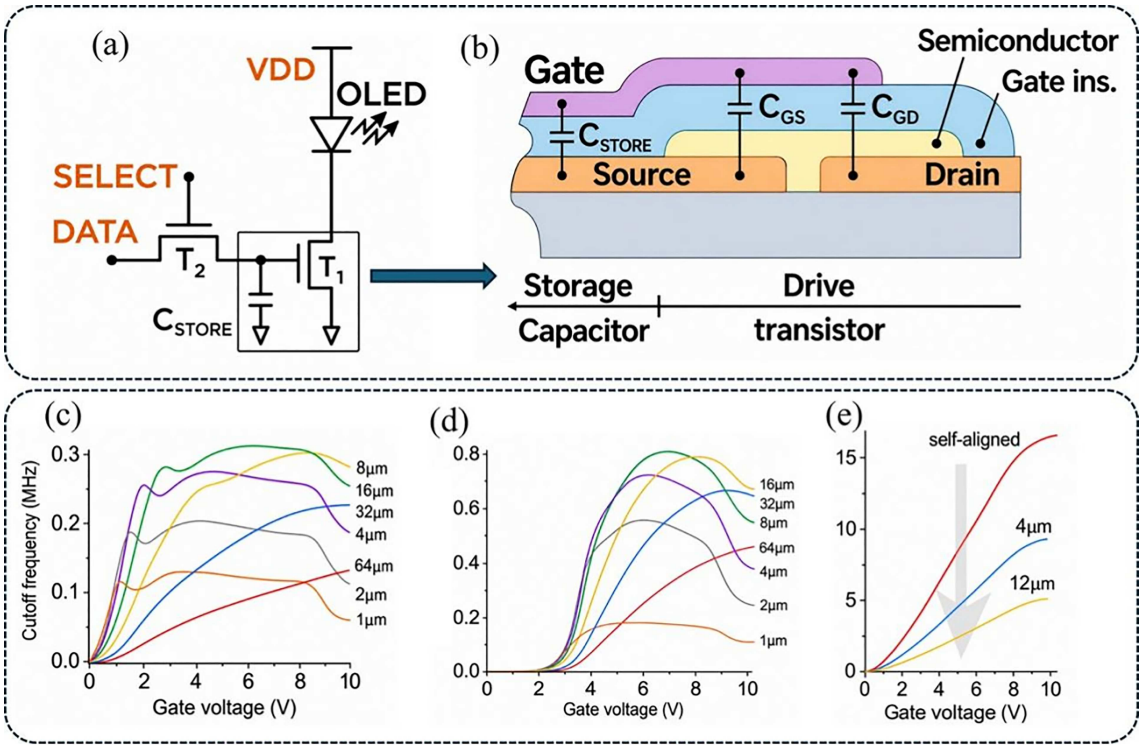

Figure 3 (Color online) (a) Simple two-transistor-one-capacitor active-matrix organic light-emitting diode (2T-1C AMOLED) pixel: T1 drive transistor, source-gated transistor (SGT), T2 switch transistor, and storage capacitor (C_{STORE}). (b) Cross-section of the selected area in (a). Calculated cut-off frequency (f_T) and its dependence on gate bias and source-gate overlap for (c) an a-Si:H SGT with source contact work function WF = 4.67 eV, (d) a poly-Si SGT with WF = 4.67 eV, (e) hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) with ohmic contacts. This figure is adapted from [37].

In contrast, contact-interface engineering focuses on constructing low-defect, low-damage, and well energy-aligned metal/semiconductor interfaces. Shi et al. [35] achieved near-ideal vdW Schottky-Mott contacts in blade-coated C_8-BTBT single-crystal films, leading to a low subthreshold swing, high intrinsic gain, and high amplifier gain. Wang et al. [32] constructed a vdW metal-barrier interlayer-semiconductor interface using a Ga_2O_3 barrier layer, improving intrinsic gain and stability. Kim et al. [44] introduced a PEI interlayer at the Al/Cu_2O contact, enhancing mobility, on/off ratio, and subthreshold swing, and further demonstrated an IGZO/Cu_2O complementary inverter. Overall, contact and barrier engineering provide effective routes toward high-gain, low-power TFTs, but low-voltage operation, large-area uniformity, and long-term reliability still require further optimization.

3.2 Sensor applications

3.2.1 *Flexible sensor application*

In flexible sensor applications, low power consumption, high sensitivity, mechanical flexibility, and long-term stability are key targets for thin-film transistor development. Baek et al. [45] first addressed pressure sensing by employing deformable source/drain electrodes and subthreshold operation, enabling pressure-dependent contact resistance modulation shown in Figures 4(a)–(c) and thereby realizing low-power, highly sensitive electronic-skin arrays. Subsequently, Nathan et al. developed all-inkjet-printed organic thin-film transistors, demonstrating a low-cost fabrication route compatible with textile weaving and fiber wrapping shown in Figures 4(d) and (e), which provides a technological basis for wearable sensor arrays [46]. Further progress was achieved with surface-doped organic-crystal SGTs, where the synergy between surface doping and the source-gated architecture improved mobility, operational stability, and resistance to bending/stretching deformation [47]. In addition, intrinsically stretchable subthreshold organic transistors exploited temperature-dependent hopping transport to realize skin-conformable, low-power temperature-sensing arrays [48]. Overall, these studies have advanced flexible sensors from individual sensing units toward low-power, high-gain, integrable, and stable wearable systems, although challenges remain in device uniformity, large-area manufacturing, long-term mechanical fatigue, and reliability under complex operating environments.

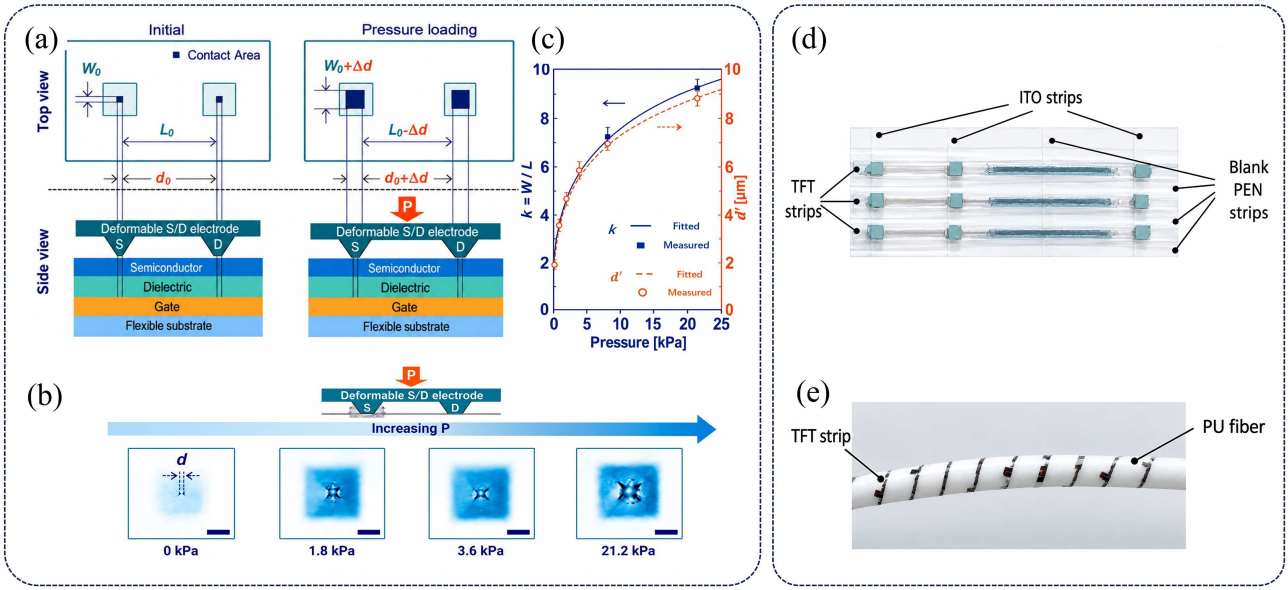

Figure 4 (Color online) (a) Side/projected-view schematic diagram of the pressure-sensitive contact transistor (PCT) showing parameter changes upon pressure loading. (b) Microscopic images of the contact area between deformable S/D electrodes and semiconductor under applied pressure (scale bar = 10 μm). (c) Contact length d and corresponding channel geometrical parameter $k = W/L$ change with applied pressure; bars: ±1 s.d., $n = 3$. (d) Photo of the weaved strip organic thin-film transistors (OTFTs) with interconnections using indium tin oxide (ITO) strips and Ag paste. (e) Photo of the coiled OTFTs around a stretchable polyurethane (PU) fiber. This figure is adapted from [45, 46].

3.2.2 *Biosensor applications*

In biosensor applications, both SGTs and SB-TFTs have been employed as front-end amplifiers for weak physiological signals. Zhou et al. [49] developed solution-processed IGO-based SB-TFTs in which the Schottky barrier was tuned by adjusting the In/Ga cation ratio and the source-metal work function. The resulting devices achieved high intrinsic gain and low power consumption, enabling direct amplification of EOG and ECG signals and integration with a PPG sensor for cuffless blood-pressure monitoring. The experimental demonstration is shown in Figure 5. Zhuang et al. [50] reported metal-oxide SGTs based on an In_2O_3/In_2O_3:PEI homojunction, where PEI modulated source-region depletion and the contact barrier, leading to low saturation voltage, low power consumption, and high-gain inverters for EOG signal detection. Owing to their relatively simple fabrication, both approaches are promising for wearable health monitoring, although their stability, reliability, and system-level integration still require further validation.

3.2.3 *Gas-sensor applications*

In gas-sensor applications, Schottky contacts and barrier modulation provide a promising route toward low-power, room-temperature detection. Huang et al. [51] modulated surface states in a-IGZO through localized UV treatment, forming asymmetric Schottky barriers in an Au/a-IGZO/Au metal-semiconductor-metal structure and enabling self-powered ozone sensing at zero bias. Ghosh et al. [52] employed Pd-Ti/ZnO Schottky-contact TFTs, where hydrogen adsorption lowers the barrier height and modulates the drain current, allowing room-temperature hydrogen detection. Both approaches feature simple device structures, low power consumption, and room-temperature operation. However, response/recovery speed and long-term reliability remain to be improved. Future work may combine interface modification with on-chip integration to develop low-power, multi-gas intelligent sensing systems.

3.3 Optoelectronic device

3.3.1 *Organic thin-film phototransistors and low-power circuit applications*

Organic thin-film phototransistors and their low-power circuit applications represent an important extension of SGT research. For example, solution-processed polymer SGTs and DNTT-based organic source-gated phototransistors can achieve high photo-to-dark current ratios under low-bias or even zero-gate-bias conditions, highlighting their potential for low-power photo-sensing [38, 53]. MoO_3-doped pentacene devices further combine material doping with the suboptimal-SGT architecture to enhance ultraviolet response while substantially reducing power consumption [54]. In addition, as shown in Figure 6, IGZO/DNTT complementary inverters demonstrate that such devices

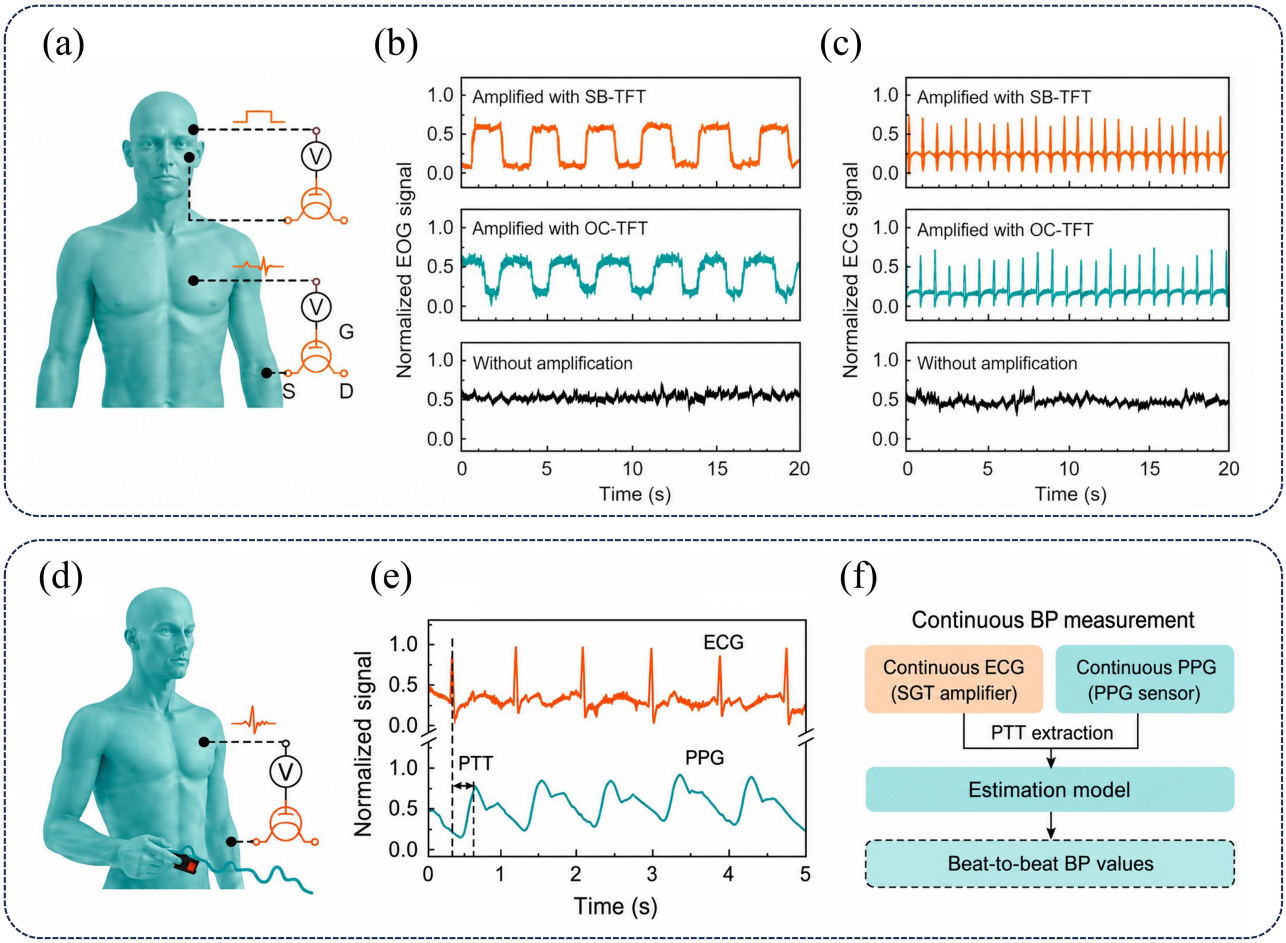

Figure 5 (Color online) (a) Schematic of the thin-film transistor (TFT)-based amplification circuit for electrooculogram (EOG) and electrocardiogram (ECG) acquisition. Commercial gel electrodes were used to acquire the electro-physiological signals. (b) EOG and (c) ECG signals amplified with the SB-TFT (top), the OC-TFT (middle), and without amplification (bottom). (d) Working principle of the ECG/photoplethysmography (PPG)-based blood pressure (BP) measurement system. Schematic of the measurement layout integrating the SB-TFT amplifier and a commercial PPG sensor. (e) Representative simultaneously recorded ECG and PPG signals with definition of the pulse transit time (PTT) marked. (f) Diagram of the continuous BP estimation process based on extracted PTT values. This figure is adapted from [49].

can be extended beyond photodetection to high-gain signal amplification and readout circuits. More importantly, because DNTT is highly photosensitive, the trip point of the complementary inverter can be modulated by incident light intensity, providing a hardware basis for low-power photosensitive logic circuits [55]. However, the stability of organic materials remains a key challenge; future work should therefore focus on large-area printing processes and complementary integrated-circuit design.

3.3.2 *Low-dimensional material photodetectors*

Owing to their intrinsically low free-carrier concentration and high surface-to-volume ratio, one-dimensional semiconductors can deliver excellent low-power detection performance when combined with Schottky-depletion mechanisms. Researchers constructed a p-type SGT using sulfur-rich-shell GeS nanowires and Al contacts, and first employed it as a photodetector, where the source Schottky barrier enabled low saturation voltage and pW-level power consumption [56]. This concept was further extended to n-type CdS nanobelt SGT phototransistors. By selecting high-work-function Ni electrodes, Wang et al. [57] formed a Schottky barrier at the CdS source contact, achieving ultralow power consumption together with high responsivity and detectivity. This work fills the gap in n-type SGT photodetectors and offers a possible route toward low-power complementary optoelectronic circuits.

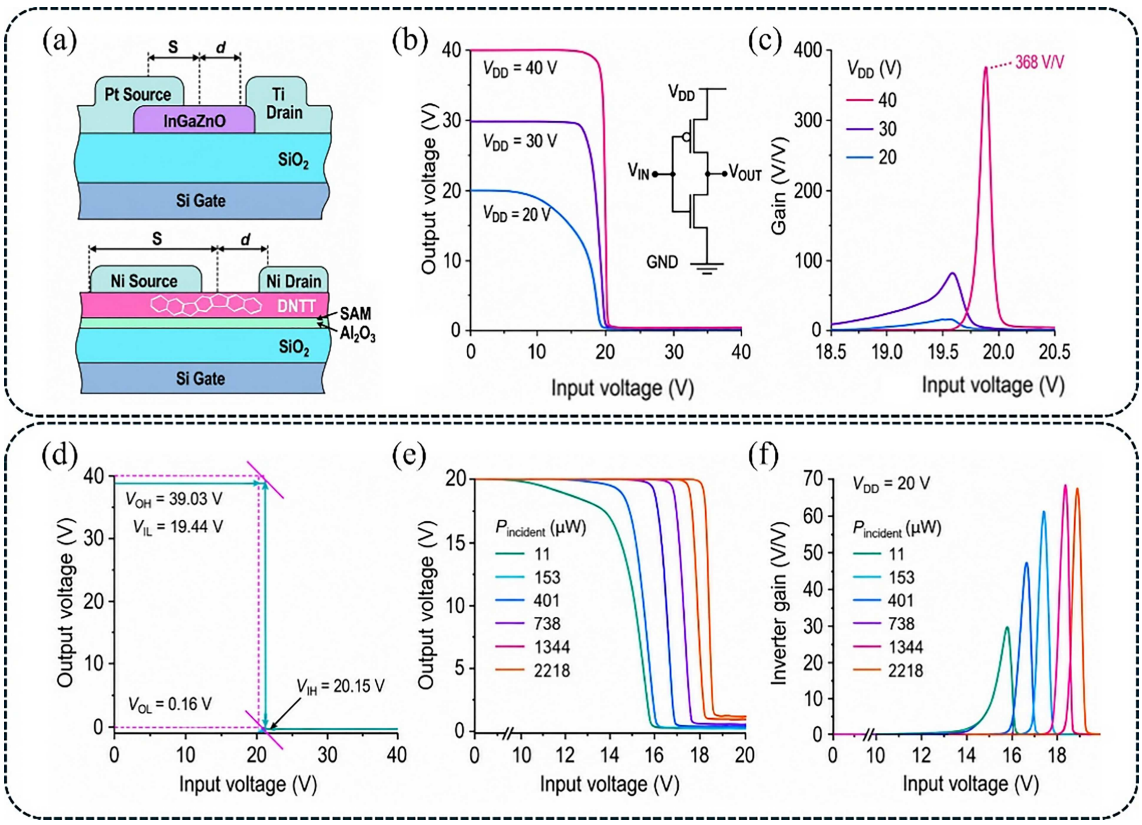

Figure 6 (Color online) (a) Staggered-electrode thin-film source gated transistors (SGTs) made with indium gallium zinc oxide (IGZO) and dinaphtho [2,3-b:2',3'-f]thieno [3,2-b]thiophene (DNTT); (b) inverter transfer curves at several power supply voltages, V_{DD}, with circuit diagram inset; (c) the voltage gain; (d) the output voltage of the inverter circuit in (a) shown for the region of interest around the switching voltage with noise margin calculation for the inverter operating at V_{DD} = 40 V; (e) inverter transfer characteristic under different illumination intensities; (f) inverter gain under different illumination intensities. This figure is adapted from [55].

3.4 Thin-film neuromorphic and neurochemical detection

In recent years, SB-TFTs have shown unique advantages in neuromorphic computing and neurochemical sensing. He et al. [58] first realized the conversion from "silent synapses" to functional synapses by combining Ag/IGZO Schottky contacts with a chitosan electrolyte double layer. Chen et al. [59] introduced Ag/PDVT-10 Schottky source contacts in organic synaptic transistors to suppress channel current, reducing the energy consumption of a single synaptic event to approximately 480 fJ while achieving high accuracy in handwritten-digit recognition. Cha et al. [60] formed Schottky barriers between Hf-ZnO and Cr/Au electrodes; by combining a wide-bandgap Hf-ZnO channel, trap states in the oxide dielectric, and current limitation by a load TFT, they achieved fW-level power consumption and systematically analyzed the trade-off between programming speed and retention time. Furthermore, Barua et al. applied Schottky-barrier IGZO TFTs to dopamine detection, where deep-subthreshold operation enabled high intrinsic gain and ultralow power consumption, together with high sensitivity, a low detection limit, and partial regeneration capability [61, 62]. Overall, these studies offer low power consumption, high sensitivity, simple device structures, and potential for both synaptic emulation and biosensing. However, challenges related to ion migration, trap-state instability, drift in liquid environments, device uniformity, and array integration remain to be addressed. Future research should focus on stable barrier modulation, long-term reliability, multifunctional integration, and system-level applications.

4 Technological outlook, challenges, and future directions

4.1 Oxide semiconductors

Material defects are among the key factors limiting both performance enhancement and reliability optimization in oxide semiconductor devices. This section focuses on oxygen vacancies and contact-interface defects, systematically analyzing their impact on device electrical characteristics and bias-stress stability. These defects not only influence

critical parameters of individual devices, such as threshold voltage, subthreshold swing, and contact resistance, but may also amplify device-to-device variability during large-area array integration and mass fabrication. Therefore, for SB-TFTs, defect regulation constitutes a critical technical challenge that must be overcome to enable practical applications.

First, oxygen vacancies are among the dominant intrinsic defects in oxide semiconductors [63]. They exert a significant influence on the device performance of SB-TFTs. Oxygen vacancies can modulate the band bending at metal/semiconductor contacts, the distribution of interface defect states, and Fermi level pinning, thereby altering the effective Schottky barrier height. When the concentration of oxygen vacancies becomes excessively high, the interfacial carrier density increases and defect-assisted tunneling is enhanced, leading to a reduction of the effective Schottky barrier and causing the contact behavior to approach ohmic characteristics [64]; conversely, when the oxygen vacancies concentration is insufficient, the number of donor-state electrons decreases, resulting in a reduced on-state current. Previous studies have shown that oxygen vacancies can significantly affect Fermi-level pinning and the distribution of defect states in oxide semiconductors. Consequently, the actual Schottky barrier height often deviates from the ideal value predicted solely from the metal work function and the semiconductor electron affinity [65]. Moreover, in practical devices, the non-uniform distribution of oxygen vacancies can induce variations in key parameters among devices from the same batch, thereby reducing device uniformity [66, 67]. These considerations indicate that precise control of oxygen vacancies is essential for achieving SB-TFTs with high performance and excellent uniformity. In addition, the metal/semiconductor contact interface represents another critical factor governing the characteristics of SB-TFTs. In practice, the metal/semiconductor contact interface does not fully conform to the ideal Schottky-Mott model. Interfacial chemical reactions, oxygen vacancies accumulation, metal-induced gap states, and local redox processes can all cause Fermi-level pinning, leading to a Schottky barrier height that deviates from the ideal value [64, 68]. For instance, in Pt/a-IGZO contacts, metal deposition followed by thermal treatment can induce changes in the interfacial chemical state, thereby significantly modulating the Schottky barrier height [68]. Furthermore, in n-type oxide semiconductors, surface electron accumulation layers and interfacial oxygen vacancies can also hinder the formation of high-quality rectifying contacts [69]. Therefore, non-uniformities in the chemical states and electronic structure of the contact interface can result in variations in local barrier height and width, as well as carrier-injection pathways, thereby significantly affecting device uniformity.

From a long-term stability perspective, oxygen vacancies and their associated sub-gap states, together with the evolution of the metal/semiconductor contact interface, are key factors governing electrical parameter drift in oxide semiconductors. These defects undergo dynamic charge trapping and de-trapping under operating conditions such as bias stress and illumination, gradually driving the device away from its initial operating state. This manifests as continuous threshold voltage drift, on-state current degradation, and overall deterioration of output characteristics [70, 71]. Meanwhile, this charge redistribution, dominated by defect states, exhibits pronounced time dependence, leading to gradual device performance degradation and thereby limiting reliability under long-term continuous operation [72]. Therefore, long-term stability becomes particularly critical in SB-TFT devices. Since the barrier height at the contact interface is crucial for carrier injection, any redistribution of oxygen vacancies or reconfiguration of interface states during prolonged operation can induce barrier fluctuations, leading to instability in intrinsic gain. This highlights a key physical origin that limits long-term stable device operation.

4.2 Organic semiconductors

For organic SB-TFTs, the influence of grain boundaries on device performance and device-to-device uniformity is particularly pronounced. Owing to the intrinsically weak van der Waals interactions governing intermolecular packing in organic semiconductors, solution-processed thin films typically exhibit kinetically driven crystallization, leading to the formation of multiple nucleation sites under rapid solvent evaporation or local supersaturation conditions. Subsequently, grains with different crystallographic orientations undergo competitive growth during film formation, leading to the formation of orientationally discontinuous grain boundary regions at their interfaces [73]. Accordingly, grain boundaries can be regarded as structurally disordered regions governed by film formation kinetics, whose density, misorientation angles, and spatial distributions are strongly dependent on the specific deposition conditions [74].

Atomic-scale simulations indicate that grain boundaries in small-molecule organic semiconductors can introduce localized electronic trap states, thereby significantly affecting charge transport. Shallow-level traps generally enable reversible carrier trapping and de-trapping under external electric fields, thermal excitation, or illumination, whereas deep-level traps lead to long-lived charge localization states that act as strong scattering centers, thereby significantly impeding charge transport [75]. Meanwhile, Hall effect measurements in polycrystalline organic semiconductors further demonstrate that grain boundaries disrupt coherent carrier transport, leading to a Hall mobility

lower than the field-effect mobility, thereby evidencing transport dominated by strong static disorder and carrier localization effects [76]. Grain-boundary-induced local disorder can modulate carrier mobility, threshold voltage, and subthreshold characteristics by altering the density of states distribution and the effective carrier delocalization length [77]. Because grain boundary resistance is strongly dependent on the grain boundary misorientation angle, even subtle variations in grain boundary density and orientation distribution among devices can lead to significant dispersion in mobility, turn-on voltage, contact resistance, and output current [73]. In addition to its impact on bulk transport, grain boundaries located near the source contact can further modulate the local potential landscape and trap occupation states in the source-proximal region, thereby influencing carrier injection and the effective Schottky barrier in SB-TFTs. Furthermore, grain-boundary-induced charge trapping leads to threshold voltage shift under bias stress, an effect that becomes more pronounced with increasing grain boundary density, thereby further exacerbating device-to-device variability in operational stability [74]. Process factors can further amplify the aforementioned grain boundary effects. The formation of solution-processed thin films is highly sensitive to droplet spreading dynamics, contact line motion, solvent evaporation rate, substrate surface energy, and local temperature fields. These coupled process dependencies lead to spatial variations in crystal nucleation sites, grain size, molecular orientation, and grain boundary density [78], thereby ultimately affecting device uniformity.

Variations in printed feature dimensions and fabrication-induced defects remain key challenges for the large-scale integration of organic SB-TFTs. Inkjet printing offers advantages including low cost, additive patterning, and compatibility with flexible substrates; however, it generally remains inferior to conventional photolithography in terms of pattern resolution, droplet volume control, and film uniformity. Although inkjet-printed OTFTs have demonstrated a range of device and integrated circuit functionalities, reliability studies consistently indicate that array yield, device performance distribution, and fabrication-induced defects remain critical challenges for large-scale manufacturing [79, 80]. For organic SB-TFTs, the channel-length insensitivity can partially mitigate the impact of channel length variations on the drain current; however, incomplete semiconductor coverage, contamination in the contact region, or local film thickness nonuniformity may still degrade the Schottky barrier, leading to increased leakage current or even device failure. Therefore, the fabrication of organic SB-TFTs still requires high-resolution patterning and stringent defect control. Related studies have shown that high-resolution patterning techniques used in nanoscale flexible OTFTs, self-aligned OTFTs, nanoimprinted OTFTs, and high-frequency OTFTs can effectively reduce dimensional variations while simultaneously improving device density and frequency response [81–83].

4.3 2D semiconductors

Owing to their atomic-scale thickness and dangling-bond-free surface, 2D materials exhibit interfacial electronic behavior that is fundamentally distinct from that of conventional oxide and organic semiconductors. First-principles studies indicate that Schottky barriers are commonly formed at monolayer MoS_2-metal interfaces, primarily arising from the combined effects of interfacial electric dipoles and metal-induced gap states (MIGS). These interface states introduce a high density of electronic states within the bandgap and lead to partial Fermi level pinning [84]. Therefore, early studies on 2D material devices were primarily focused on reducing contact barriers to achieve near-ohmic transport. However, Liu et al. [22] demonstrated a stable and tunable SB-TFT architecture based on a 2D MoS_2 system, in which a dual-gate electric field modulates the source-side carrier injection barrier, making current transport dominated by the source barrier and thereby maintaining high output resistance and high intrinsic gain even under short-channel conditions. Likewise, intrinsic defects in 2D materials can significantly affect SB-TFT performance. In 2D semiconductors such as TMDs, intrinsic point defects, including sulfur/selenium vacancies, interstitial atoms, and substitutional impurities, are ubiquitously present. These defects introduce localized states within the bandgap, modulate the Fermi level position, and perturb carrier transport pathways, thereby leading to pronounced device-to-device variations in threshold voltage, mobility, and subthreshold swing [85]. Furthermore, defects not only influence static transport characteristics but also govern the time-dependent behavior of devices. During carrier transport, defect states act as charge trapping and de-trapping centers, giving rise to pronounced hysteresis and threshold voltage drift. In addition, they introduce non-radiative recombination pathways, which degrade the photoresponse and long-term device stability [86]. Furthermore, the contact behavior between 2D semiconductors and metal electrodes is governed by the combined effects of Fermi level pinning and interface state inhomogeneity. Vacancies and adsorbed impurities further modulate the local work function distribution, leading to significant dispersion in contact resistance and thereby dominating overall device performance variability [87].

Owing to the absence of bulk screening in 2D materials, the effects of atomic-scale defects and interface states on device characteristics are further amplified. Meanwhile, their fully exposed surfaces render them highly susceptible to environmental perturbations, as oxygen, water molecules, and illumination can preferentially interact with defect sites, leading to slow oxidation, adsorption-induced doping, or even structural degradation [88]. In SB-TFTs, defects

significantly modulate the source-side barrier, thereby impacting device uniformity and long-term stability. This indicates that while 2D SB-TFTs offer the advantages of high gain and low power consumption, they simultaneously impose stricter controllability requirements on material defect distribution and interface engineering.

4.4 Future directions

Building on the preceding discussion of material-specific challenges in SB-TFTs, further performance improvements require a systematically coordinated optimization across multiple interdependent levels, including semiconductor/metal interface engineering, process integration compatibility, device- and circuit-level co-design, and long-term operational stability under application-relevant stress conditions. Accordingly, future research efforts are expected to concentrate on the following four key directions.

At the material level, the performance of SB-TFTs is primarily governed by two coupled processes: carrier injection across the metal-semiconductor contact, which is controlled by the effective Schottky barrier height and strongly influenced by Fermi-level pinning and interfacial states; and carrier transport within the semiconductor channel, which is determined by the intrinsic carrier mobility and further degraded by scattering from structural defects, disorder, and grain boundaries. Therefore, in low-power high-frequency applications, optimizing channel conductivity or reducing contact resistance alone is generally insufficient, as these approaches tend to selectively improve either carrier transport or injection, and thus cannot simultaneously optimize injection efficiency and high-speed device response, which are intrinsically coupled through the overall device electrostatics and parasitic-limited switching dynamics. To address these challenges, narrow-bandgap organic and oxide semiconductors provide a promising material pathway for SB-TFTs. In such systems, improved energetic alignment between the metal Fermi level and semiconductor transport levels can reduce the effective Schottky barrier height, particularly under conditions of moderate Fermi-level pinning, thereby facilitating carrier injection, lowering operating voltage, and improving turn-on characteristics. Concurrently, narrower bandgap systems often exhibit modified electronic density-of-states distributions and reduced energetic disorder, which can mitigate trap-assisted carrier localization and support more efficient charge transport. Consequently, the effective carrier mobility is enhanced, which, together with improved contact injection, contributes to higher high-frequency performance. Nevertheless, the realization of these advantages critically depends on effective suppression of both bulk and interfacial defect states, with interfacial traps playing a dominant role in determining device stability. Otherwise, increased disorder and imperfect interface formation can enhance trap-assisted charge trapping and de-trapping processes, thereby degrading bias stability and long-term operational reliability.

At the process level, self-aligned architectures, nanoimprint lithography, high-resolution photolithography, and three-dimensional integration provide complementary routes for controlling critical device and interconnect geometries during scaling. These techniques enable improved definition of channel length and contact alignment, reduction of short-channel effects, and enhanced interconnect engineering in vertically or laterally integrated structures, which collectively contribute to improved device scalability, reduced device-to-device variability, and enhanced electrical uniformity. Accordingly, hybrid processing strategies combining printing and photolithography should be further explored to balance the trade-off between patterning resolution, throughput, and process compatibility. In parallel, three-dimensional integration offers a viable route to extend functional density beyond planar scaling constraints. Overall, these approaches are expected to improve the trade-off landscape among device density, array yield, and system-level integration complexity under practical fabrication constraints [81, 82, 89].

At the circuit architecture level, the performance of SB-TFT-based circuits is governed not only by the device-level characteristics such as transconductance and static power consumption, but also by the limited circuit-level functional diversity achievable under low-voltage operation. This constraint restricts the extent of in-circuit signal processing, which in turn maintains a dependence on external amplification, filtering, and communication modules at the system level, leading to increased power consumption and architectural complexity. Accordingly, deep-subthreshold operation can be exploited to develop low-voltage mixed-signal circuits, where signal amplification and basic logic functions are co-designed within a constrained operating regime, subject to inherent trade-offs among gain, noise, and speed. In addition, threshold-tunable device architectures enable reconfigurable local preprocessing functions, supporting the integration of sensing, amplification, and signal conditioning at the circuit level and offering a route toward multi-stage system integration [79, 90].

Finally, in the context of biointegrated and physiological sensing applications, SB-TFT-based devices may be adapted through appropriate material selection and encapsulation engineering to achieve mechanical compliance and, in certain implementations, transient functionality. Such systems are particularly relevant for implantable or epidermal physiological monitoring and bioelectronic interfacing. The key design requirements include biocompatibility, mechanical compliance, and operational stability under physiological conditions, with specific emphasis

depending on whether long-term implantable or transient operation is targeted [91]. Meanwhile, environmental factors such as mechanical deformation, humidity, perspiration, and physiological fluids can induce performance drift and accelerate degradation processes, thereby posing significant challenges to device reliability [92]. Advances in transient electronics, stretchable semiconductor platforms, and flexible sensing systems provide important design principles for mechanically compliant and environmentally robust device architectures [93–96].

5 Conclusion

This review systematically summarizes recent advances in SB-TFT technology based on subthreshold operation and Schottky barrier engineering. By operating in the near-off regime, such devices achieve a reduced dependence on geometry and bias conditions, enabling relatively high transconductance and low static power consumption under specific operating conditions, thereby partially alleviating the trade-off among power consumption, gain, and process compatibility in conventional thin-film transistors. With the continued development of different material systems, including oxide semiconductors, organic semiconductors, and 2D materials, SB-TFTs have been progressively expanded in terms of material selection and process implementation, and have demonstrated potential applications in wearable sensing, bioelectrical signal amplification, and flexible electronic systems. However, their further large-scale application remains primarily limited by key issues such as metal-semiconductor interface defect control, device-to-device variability, and long-term operational stability. Future progress is expected to rely on coordinated advances in material engineering, hybrid fabrication processes, and circuit architecture design, thereby improving device performance and system reliability and enabling broader application in low-power distributed electronic systems.

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Profile of Arokia NATHAN



Professor Arokia NATHAN is a leading scholar and technologist in thin-film transistors (TFTs), large-area and flexible electronics, display technologies, and sensor systems. He is currently a distinguished chair professor in the School of Information Science and Engineering at Shandong University, where he joined as a full-time faculty member in July 2021. His research output includes more than 600 technical publications and several books, together with a substantial portfolio of patents. Over a research career spanning more than three decades, his work has connected fundamental thin-film device science and compact modeling to circuit design, manufacturing, and system integration. His contributions have supported the development of commercial OLED displays, high-resolution imaging systems, large-area touch and force sensors, and emerging low-power electronic platforms.

Nathan received the B.Eng. (Hons) degree in Communications Engineering, Leeds, UK in 1981 followed by the M.Sc. and Ph.D. degrees in Electrical Engineering from the University of Alberta, Canada, in 1984 and 1988, respectively. Subsequently, he worked at LSI Logic in the United States and at the Institute of Quantum Electronics, ETH Zurich, Switzerland, before joining the University of Waterloo in Canada. At Waterloo, he held the DALSA/NSERC Industrial Research Chair in Sensor Technology and a Canada Research Chair in Nanoscale Flexible Circuits, and established the Giga-to-Nanoelectronics Centre to promote interdisciplinary research across materials, devices, circuits, and systems. In 2006, he joined the London Centre for Nanotechnology at University College London as the Sumitomo Chair of Nanotechnology. He moved to the University of Cambridge in 2011 as Professor of Photonic Systems and Displays. He is currently a Graduate Tutor and Bye Fellow at Darwin College.

Nathan has worked extensively on TFTs based on hydrogenated amorphous silicon, amorphous oxide semiconductors, and organic semiconductors, including carrier transport, instability mechanisms, parameter extraction, and compact modeling. He led the development of compact models for multiple TFT material systems and promoted their use in electronic-design-automation tools for circuit simulation and process diagnostics. His research has addressed low-temperature device fabrication, integration on glass and flexible substrates, low-voltage and subthreshold operation, heterogeneous integration, and large-area sensing and imaging architectures.

In display electronics, Nathan has investigated the effects of TFT parameter variations, threshold-voltage drifts, and non-uniformities in active-matrix systems. Through IGNIS Innovation, which he founded in 2000 and where he served as Chief Technical Officer, he directed the development of compensation technologies that monitor and correct drive-TFT variations and differential OLED ageing. Related inventions were adopted in commercial display platforms. His work on large-area electronics has also extended to high-resolution image sensors, three-dimensional touch and force sensing, digital microfluidics, and sensor interfaces designed for very low power consumption.

Nathan has consistently pursued the translation of academic research into engineering practice. He has founded or co-founded technology companies including IGNIS Innovation, Cambridge Touch Technologies, ACXEL Tech, Cam-XT Solutions, and VISBAN Networks. These activities have covered compensated OLED backplanes, multi-force touch interfaces, active-matrix digital microfluidics, TFT compact-modeling software, and large-area radio-frequency systems.

He has also contributed extensively to research training and professional service. Nathan has supervised more than 60 doctoral students, more than 50 master's students, and over 30 postdoctoral researchers, and has delivered numerous invited lectures and IEEE Distinguished Lectures. He has held leadership and editorial roles within the IEEE Electron Devices Society and related IEEE communities. His contributions to TFT technology and flexible electronics have been recognized by the Royal Society Wolfson Research Merit Award and the 2020 IEEE Electron Devices Society J. J. Ebers Award. He is a Fellow of the IEEE, IET, SID, and NAI, and was elected a Fellow of the Royal Academy of Engineering in 2022 and the Canadian Academy of Engineering in 2023. He received the Chinese Government Friendship Award in 2024, and was elected a Foreign Member of the Chinese Academy of Sciences in 2025.

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