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PKP: open-source compact models and predictive PDK for GAA technology

Baokang PENG[1], Feiyu TENG[2], Guoyao CHENG[1], Heng WU[2], Lining ZHANG[1,3*], Runsheng WANG[2,3] & Ru HUANG[2,3]

[1]*School of Electronic and Computer Engineering, Peking University, Shenzhen 518055, China*
[2]*School of Integrated Circuits, Peking University, Beijing 100871, China*
[3]*Institute of Electronic Design Automation, Peking University, Wuxi 214072, China*

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Beyond the 3-nm node, the integrated circuit (IC) technology roadmap has transitioned to nanosheet (NS) gate-all-around field-effect transistors (GAAFETs), establishing design-technology co-optimization (DTCO) as the dominant paradigm for optimizing power, performance, and area (PPA). Effective DTCO relies on credible device/circuit views packaged into a process design kit (PDK), allowing designers to freely navigate the full digital flow [1]. Although commercial PDKs are essential to the semiconductor industry, their strict confidentiality renders them inaccessible to most academic groups, impeding reproducible research and the early exploration of design enablement at cutting-edge nodes. To bridge this gap, we propose physics integrated models (PHIMOs) and the Peking University Predictive PDK (PKP) for NS GAAFET technology. The device and interconnect design rules align with advanced node specifications (e.g., contacted gate and metal pitches), with the essential models extracted from calibrated numerical technology computer-aided design (TCAD) simulations. PKP3 (the PKP for 3-nm GAAFET technology) supports standard-cell layout and timing/power characterization, enabling an end-to-end digital design flow.

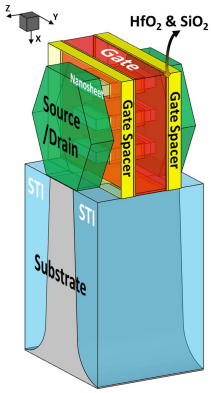
Technology descriptions. Following public NS integration disclosures, we employ a mainstream three-stack NS structure for the front-end-of-line (FEOL), as illustrated in Figure 1(a). Specifically, the device incorporates an inner spacer (ISP) along with key mid-of-line (MOL) features such as the contact (CT) and via-to-gate contact, aligning with state-of-the-art NS integration schemes.

The initial process scope targets a mainstream front-side power delivery network, aligning with standard digital design toolchains to ensure baseline compatibility and ease of adoption. For the back-end-of-line (BEOL) stack, copper is adopted as the primary interconnect metal. Local routing layers (M0–M3) employ EUV-based self-aligned patterning, whereas upper metal layers maintain 193i-friendly pitches. The FEOL and MOL features are co-optimized to support six-track single-height cells (with optional double-height configurations for complex sequential cells), ensuring robust pin accessibility on M0/M1/M2 and accurate extraction under tight routing constraints.

Model overview. At the center of CMOS PDKs are compact models and their corresponding parameter sets, representing semiconductor devices, especially transistors. For GAAFETs, these models must address new requirements that were not present in FinFET generations. A key feature of the GAAFET is its relatively flexible channel width compared with that of FinFETs. This flexibility introduces a unique width-dependence for carrier mobility and short channel effects. A further scaling of the NS thickness will trigger significant quantum confinement [2] and self-heating effects [3]. Another significant change is induced by the NS-stack ISP, which affects the parasitic components [4]. These new features pose potential challenges to compact modeling efficiency and accuracy.

The PHIMO series was developed to address these challenges. One specific model for NSs, PHIMO-NS, that integrates the physics-based modules, including the core, self-heating and parasitic modules [2–4] was developed in collaboration with industry partners. Simultaneously, the fusion modeling strategy [5] was proposed to overcome parameterization complexities. Fundamentally, the approach combines physics modules with tiny neural networks (NNs) for mathematical fitting and smoothing. For example, while the formulation of threshold voltage (V_{th}) roll-off under short-channel effects is retained, the geometry-dependent coefficients (traditionally described by semi-empirical fitting or binning) are replaced by a tiny NN. While the classical physics-based model will be available in commercial SPICE simulators, the fusion model is featured in this initial release for DTCO applications. Model parameters are extracted using the Python-implemented model through backpropagation training. These are subsequently calibrated against TCAD simulations using the device (Figure 1(b)). A single parameter set can accurately reproduce global I-V and C-V characteristics across a wide geometry range (covering a gate length (L_g) of 16–100 nm and variable NS width, from 10 to 40 nm) owing to the power of fusion modeling, which eliminates the need for the conventional multiple-bin approach. As shown in Figure 1(c), the model result correlates excellently with the simu-

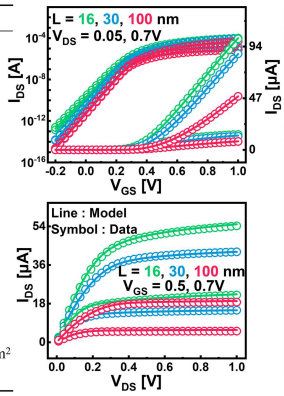
* Corresponding author (email: eelnzhang@pku.edu.cn)



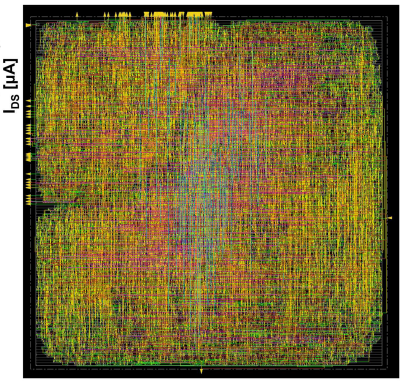
(a)

Parameter	Default value
Contacted gate pitch (CGP)	48 nm
Gate length (L_g)	16 nm
Nanosheet thickness (T_{NS})	5 nm
Suspension thickness (T_{SUS})	10 nm
Nanosheet width (W_{NS})	21 nm
Inner spacer length (T_{ISP})	6 nm
Gate spacer length (L_{SP})	7 nm
S/D extension length (L_{SD})	9.5-10 nm
Equivalent oxide thickness (EOT)	1.07 nm
n-type S/D doping ($N_{S/D\text{-}NMOS}$)	1×10^{20} cm^{-3}
p-type S/D doping ($N_{S/D\text{-}PMOS}$)	5×10^{20} cm^{-3}
Channel doping ($N_{channel}$)	5×10^{15} cm^{-3}
Contact resistivity (ρ_c, NMOS/PMOS)	2.2/2.0×10^{-9} Ω·cm^2
Supply voltage (V_{DD})	0.7 V

(b)



(c)



(d)

Figure 1 (Color online) (a) Schematic of the structure of the GAAFET device; (b) key device parameters; (c) comparison between the PHIMO model and TCAD simulation results; (d) layout view of the RISC-V core.

lation data. Four V_{th} options are provided, each featuring a simplified statistical feature of five corners. Layout-dependent effects strongly tied to the Si process are generally ignored in predictive PDKs.

PDK features. Most core PDK components are integrated into PKP3, including compact models, design rules, parasitic technology files, parameterized cells (PCells), and a standard-cell library. Parasitics are modeled using a layer-aware technology file that enables high-fidelity extraction. The extractor generates distributed $\{R', C'\}$ ladders for signal nets, incorporating coupling to adjacent tracks and underlying gates via lateral and vertical components. Power rails reside in-cell, M0/M1 provides pin access and local routing with H/V staggering, and the single diffusion break separates adjacent diffusion regions and enables legal abutment. The template respects the exact horizontal gate pitch and local-interconnect pitches, ensuring that cell instances remain pin-accessible during detailed routing.

In this release, the standard-cell library and the static random-access memory (SRAM) bit-cell are designed within a unified NS framework. The standard cells adopt six-track single-height layouts, where the number of stacked NSs (nominally three) and the drawn L_g are fixed by the design template. Dummy gates are inserted at cell boundaries, and a gate-cut layer is adopted to ensure isolation and termination definition. Approximately 50 cell types across multiple drive options are incorporated. For the SRAM bit-cell, dedicated layout rules following standard industrial practice are implemented to minimize the footprint, whereas SRAM-specific V_{th} options are provided to mitigate standby leakage.

To further evaluate the PDK at the block level, these standard cells were integrated into a complete physical implementation flow, which includes floorplanning, power mesh generation, placement, clock tree synthesis (CTS), and routing. Block-level resistance-capacitance (RC) extraction and static timing analysis were performed on the generated design exchange format (DEF) to evaluate the PPA across various process, voltage, and temperature corners using a cache-less RISC-V core as a benchmark. At the super-low-V_{th} typical-typical corner, the core achieves a clock frequency of 2.7 GHz, power consumption of 3.77 mW, and a total area of 678 μm^2; the physical layout is illustrated in Figure 1(d).

Application. PKP3 supports the Cadence Virtuoso design environment. Once installed, users can perform schematic and layout designs, pre- and post-layout simulations using Spectre with the compact model and parasitics. RC extraction generates standard parasitic exchange format (SPEF) files with layer-accurate coupling. Liberty NLDM/ECSM are characterized against the same decks, ensuring that implementation and analysis correlate without bias. Generally, complete views (models, rules, Library Exchange Format/DEF/tech files, Liberty and reference decks) are provided, and an end-to-end digital flow (from register-transfer level through synthesis, place-and-route, parasitic extraction, timing/power analysis, and physical verification) is fully supported.

Access methods. The PKP3 package is available via the webpage: https://pkp.pkueda.org.cn. Models with the Verilog-A implementation are incorporated in the package. Rule decks are provided separately with an authorization-based policy.

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