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2D fluorophlogopite mica as van der Waals dielectrics for high-breakdown-strength field-effect transistors

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Abstract Insulators with high relative permittivity (ε_r) and wide band gaps have proven to be essential components in both electronic and optoelectronic device configurations. With two-dimensional van der Waals (2D vdW) semiconductors emerging as prospective candidates for more-Moore scaling, the heterogeneous integration of insulators with 2D vdW semiconductors has been recognized as a critical pathway toward next-generation nanoelectronics. However, the trade-off between ε_r and bandgap in traditional oxide insulators (i.e., SiO_2, Al_2O_3, ZrO_2, HfO_2, TiO_2, etc.) and the unavoidable interface defects that arise when contacting 2D vdW semiconductor channels introduce significant challenges for advancing 2D material-based devices. Here, we report fluorophlogopite mica (FL mica) as an outstanding dielectric with a 2D vdW layered structure, an ultra-large breakdown strength (45 MV/cm), and a ε_r of ∼6. The all-in-vdW field-effect transistors (FETs) with MoS_2 as the channel and FL mica as the gate dielectric show a low subthreshold swing (SS) of ∼55 mV/dec at 160 K. In addition, theoretical simulations demonstrate significant influences of ε_r and interface defects on the performance of MoS_2-based FETs. These results indicate that FL mica, owing to its low cost, easy availability, and superior dielectric performance, would be a promising 2D dielectric to accelerate progress in 2D material-based applications.

Keywords two-dimensional material, fluorophlogopite mica, van der Waals contact, field-effect transistor

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1 Introduction

As silicon-based semiconductor devices continue to evolve toward greater miniaturization and higher integration for advanced computing, device dimensions have approached the nanoscale, where quantum effects dominate. To control the electric field and thus fully realize the functionalities of (opto)electronic devices, dielectrics are indispensable components in device configurations such as the field-effect transistor (FET) and the floating-gate transistor [1, 2]. To keep pace with device scaling, dielectric thickness has been reduced, rendering traditional SiO_2 no longer suitable as an effective gate dielectric at the nanoscale because of excessive leakage current associated with its ε_r (∼3.9). Consequently, many efforts have focused on mitigating device failure at the nanoscale, including establishing new device configurations (i.e., FinFET, gate-all-around) and the development of high-κ dielectrics that enable reliable operation at reduced dimensions [3, 4]. In recent years, several metal oxides (i.e., ZrO_2, HfO_2, Ta_2O_5, La_2O_5, TiO_2, etc.) have been gradually developed and applied as dielectrics because of their relatively high ε_r. However, a trade-off between ε_r and bandgap in these metal oxides can cause hidden leakage problems when using the aforementioned high-κ metal oxide dielectrics [5–9]. More importantly, the nonlayered structure of many metal oxides and deposition processes inevitably introduces a high density of interface defects, which can strongly degrade device performance.

The advent of two-dimensional van der Waals (2D vdW) materials offers a promising route not only for more-Moore scaling but also for improved contact and interface engineering owing to their atomic thickness, novel physical

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properties, and unique vdW layered structure [10]. To date, 2D vdW semiconductors have matured from microscale individual devices to wafer-scale production [11–13]. At the same time, interest in dielectrics compatible with 2D vdW semiconductors has grown rapidly [14–26]. Therefore, it is important to identify 2D vdW dielectrics that combine a large bandgap with high breakdown strength, which is an important prerequisite for fully exploiting the application potential of 2D vdW materials in devices.

Herein, we report fluorophlogopite mica (FL mica) as an outstanding dielectric with a 2D vdW layered structure, ultra-large breakdown strength (45 MV/cm), and a ε_r of $\sim$6. As a synthetic member of the mica family (aluminosilicates), the intentional addition of Fluorine atoms in FL mica synthesis provides improved thermal stability and corrosion resistance compared with other micas [27, 28]. Compared with natural mica crystals (i.e., muscovite), FL mica offers advantages including higher purity, an atomically flat surface, and greater flexibility due to its synthetic production [29]. By using FL mica as a gate dielectric, we fabricated 2D-MoS_2-based FETs that exhibit a low subthreshold swing (SS) of $\sim$55 mV/dec at 160 K and a high on/off ratio of $\sim 10^5$. These results indicate that FL mica, with low cost, easy availability, and strong dielectric performance, is a promising 2D dielectric that enriches investigations on 2D vdW dielectrics and advances 2D-material-based applications.

2 Methods

2.1 Device fabrication

FL mica single crystals with different sizes (1 cm × 1 cm, 2 cm × 2 cm, 2 inch) and MoS_2 single crystals were purchased from Hefei Kejing Materials Technology Co., Ltd. In the preparation of the FET device, MoS_2 single crystals were mechanically exfoliated using 3M tape and then dry-transferred from the tape to a 2 cm × 2 cm Si/SiO_2 substrate using polydimethylsiloxane (PDMS). After photolithography, source and drain electrodes were deposited on the patterned MoS_2 nanoflakes by thermal evaporation. Subsequently, FL mica bulk crystals were mechanically exfoliated using 3M tape. Samples were picked up using PDMS from regions of the tape covered with FL mica nanosheets of varying thickness. Using a high-precision two-dimensional material transfer platform system and an optical microscope, FL mica nanosheets with suitable thickness and lateral size were selected on the PDMS. The transfer platform was used to slowly lower the PDMS and stack the FL mica onto the MoS_2 two-terminal device on the Si/SiO_2 substrate. Finally, a gold ribbon was dry-transferred onto the FL mica to form a top gate electrode and build the whole FET structure. The silicon of the Si/SiO_2 substrates used here is p-type doped with a resistivity of 0.05–0.2 Ω·cm. The thickness of the SiO_2 layer is 300 nm. For device testing, we used a top-gate structure and grounded the bottom silicon of the supporting Si/SiO_2 substrate.

2.2 Sample characterization

Atomic force microscopy (AFM; Nanoscope IIIa, Bruker & MFP-3D Origin, Oxford) was used to characterize the morphology of FL mica nanoflakes. For high-resolution transmission electron microscopy (HRTEM) and energy-dispersive X-ray spectroscopy (EDS), FL mica single crystals and FET devices were cut by focused ion beam (FIB) and examined by transmission electron microscopy (TEM; FEI Talos F200X). X-ray diffraction (XRD) spectra were collected with a D8 ADVANCE X diffractometer (Bruker). Raman spectra were obtained using a confocal micro-Raman spectrometer (InVia, Renishaw) with a 532 nm excitation laser. Photoluminescence (PL) spectra for FL mica were obtained using a PL infrared spectrometer (80v, Bruker). The dielectric properties of FL mica nanoflakes were measured using conductive AFM (C-AFM) modes on the AFM systems listed above. The electrical properties of the FET devices and the dielectric performance of metal-insulator-metal (MIM) samples were measured with a semiconductor device parameter analyzer (B1500A, Keysight). Low-temperature measurements of the FET devices were performed in a liquid helium-free magnet cryogenic system (TeslatronPT, Oxford).

2.3 Numerical calculations

After obtaining transfer curves ($I_{\rm ds}$-$V_{\rm g}$) using the semiconductor device parameter analyzer (B1500A, Keysight), the SS was extracted from the steep rise region of the transfer curve, which is also recognized as the subthreshold region. SS is calculated as $SS = {\rm d}V_{\rm g}/{\rm d}(\log I_{\rm ds})$, where $V_{\rm g}$ is the gate voltage as the horizontal coordinate and $I_{\rm ds}$ is the source/drain current as the vertical coordinate.

2.4 Density functional theory (DFT) calculations

Electronic structure calculations were performed using the Vienna Ab initio Simulation Package (VASP) [30,31] with the projector augmented-wave method. The Perdew-Burke-Ernzerhof (PBE) generalized gradient approximation (GGA) [32] was used for the exchange-correlation functional. The plane-wave cutoff energy was set to 500 eV, and self-consistent calculations were converged until the total energy change was less than 1×10^{-5} eV. To account for van der Waals interactions, a dispersion-corrected DFT approach was employed [33]. All structures were fully relaxed until the Hellmann-Feynman force on each atom was less than 0.01 eV/Å. Because GGA-PBE underestimates semiconductor band gaps, the hybrid HSE06 functional [32] was used in our calculations to obtain the band structure. Transport simulations of MOSFETs were performed using the Atomistix ToolKit 2019 package [34, 35] within a DFT framework coupled to the nonequilibrium Green's function (NEGF) formalism. The boundary condition in the gate direction was set to Neumann (the derivative of the electrostatic potential, i.e., the electric field, is zero at the boundary). Technology computer aided design (TCAD) simulations were used as a supplement to the DFT calculations; these show that, even with a substrate present in the theoretical simulation, the gate electric field can be effectively depleted due to the natural n-type characteristics of MoS_2, resulting in almost no electric field or voltage drop in the substrate. DFT and TCAD simulations show consistent trends (Figure S1). For device modeling, we use the international technology roadmap for semiconductors 2028 (ITRS 2028) edition because it is directly related to sub-5 nm gate lengths and generally imposes stricter criteria than later versions. An ideal rectangular continuum metal gate was used in the device model. The real-space mesh cutoff was set to 125 Ha. We adopted GGA and the PBE functional [36]. The drain current was determined at a given supply voltage of 0.64 V, specified by the ITRS requirement for low-power (LP) and high-performance (HP) applications in the sub-5 nm gate-length region.

3 Results and discussion

FL mica crystalizes in a triclinic lattice with $P1$ space group (a = 5.29 Å, b = 5.30 Å, c = 10.16 Å) and adopts a vdW layered structure along the c direction, with a monolayer thickness of 9 Å (Figures 1(a) and (b)). Analogous to muscovite, FL mica belongs to the large silica-aluminum family of mica with the chemical formula $KMg_3AlSi_3O_{10}F_2$; its crystals contain six elements: K, Mg, Al, Si, O, and F (Figure S2). Unlike muscovite, FL mica is a completely synthetic crystal in which the hydroxyl groups of muscovite are replaced by Fluorine in the lattice, improving mechanical properties and thermodynamic stability compared with natural muscovite [37]. Besides, because of mature production processes and diverse sizes (Figure S3), FL mica has been adopted as a popular substrate for chemical vapor deposition (CVD). FL mica provides an ideal platform for the preparation of new 2D materials because of its atomically flat vdW surface, stability at elevated temperatures, and high strength with considerable flexibility.

Just as graphene and MoS_2 were used experimentally as lubricants before they were widely appreciated as 2D vdW semiconductors, FL mica has excellent potential as a vdW dielectric, in addition to serving as a quality epitaxial substrate. The vdW layered structure of FL mica indicates mechanical exfoliation to obtain 2D nanoflakes. Experimentally, large-area FL mica nanoflakes with ultrathin thickness can be easily obtained on arbitrary substrates by mechanical exfoliation and dry transfer using tape and PDMS (Figure 1(c)). This ease of exfoliation can be attributed to the low calculated cleavage energy of FL mica (∼26 meV/$Å^2$) (Figures 1(d) and S4), which is comparable to graphene, hBN, MoS_2, and Bi_2OSe_5 [38–40].

The single-crystalline nature and vdW layered structure of exfoliated FL mica nanoflakes were confirmed by HRTEM after FIB sample preparation. Cross-sectional high-angle annular dark field scanning TEM (HAADF-STEM) images show (100) planes with a vdW gap (Figures 1(e) and (f)) and (010) planes (Figure 1(g)), which correspond to two perpendicular sides of the crystal flake. Selective-area electron diffraction (SAED) patterns along the [001] and [010] directions verify the superior single-crystal quality of the exfoliated FL mica flakes (Figures 1(h) and S5).

To analyze FL mica structure and properties further, we carried out spectroscopic characterizations. In the XRD spectrum, the characteristic peaks with consistent spacing correspond to the different crystal faces of the FL mica along the vdW stacking direction (Figure 2(a)). Using Bragg's law ($2d \sin\theta = n\lambda$), the characteristic peak of (001) corresponds well to the monolayer thickness (∼9 Å) characterized by AFM. By resolving the core electron energies, X-ray photoelectron spectrum (XPS) confirms the presence of the six constituent elements in FL mica nanosheets (Figure 2b), and the elemental ratios match the theoretical stoichiometry. The PL spectra show that FL mica exhibits strong photoluminescence in the visible-near-infrared range with pronounced thickness dependence: thin

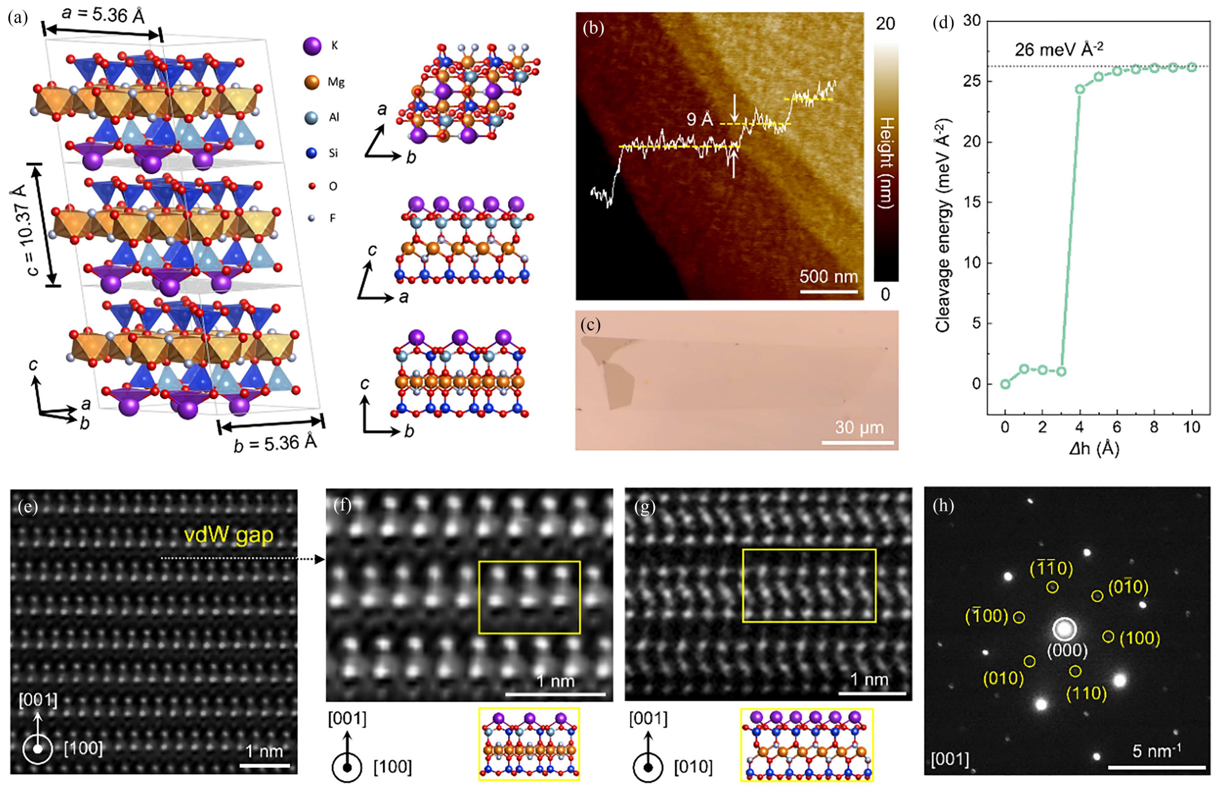

Figure 1 (Color online) Crystal structure and characterization of Fluorophlogopite mica (FL mica). (a) Crystal structure of FL mica with vdW gaps indicated by gray planes and atomic configurations along three principal crystallographic directions; (b) monolayer thickness of FL mica characterized by atomic force microscopy (AFM); (c) optical micrograph of a mechanically exfoliated FL mica nanoflake with a large area and thin thickness; (d) calculated cleavage energy of FL mica ($\sim$26 meV/Å^2); (e) high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of an exfoliated FL mica nanosheet, showing a vdW layered structure; the vdW gap is indicated by a white dotted line; (f) magnified region of (e) with the corresponding atomic configuration below; (g) HAADF-STEM image of the (010) plane; (h) selected-area electron diffraction (SAED) pattern along the [001] direction.

samples (thickness $<$ 30 nm) show stronger peaks at shorter wavelengths (556 and 602 nm), while thicker samples exhibit stronger luminescence at longer wavelengths (712 and 748 nm, merging in a peak at 720 nm), which are shown in Figures 2(c) and (d). This behavior may be attributed to vacancy-related defect states arising from the complex composition of FL mica; the thickness dependence is consistent with transitions involving defective energy levels. In addition, it is noteworthy that FL mica shows rich information in Raman spectra, with five characteristic peaks of 100.8, 197.6, 276.1, 318.0, and 490.7 cm^{-1} (Figure 2(e)). The absorption spectrum indicates negligible absorption from the ultraviolet to the mid-infrared range (Figure 2(f)). First-principles calculations yield a large bandgap of $\sim$5.72 eV for FL mica (Figure 2(g)), consistent with the observed ultra-large breakdown strength.

To evaluate the dielectric performance of FL mica, mechanically exfoliated FL mica nanosheets were dry-transferred onto Au-coated substrates (on Si/SiO_2) for conductive AFM (C-AFM) characterization. The Au-coated substrate was connected to the measurement platform via a conductive connection; a negative bias was applied to the conductive probe to drive electron flow from the C-AFM tip through the dielectric layer to the Au-coated substrate, which is schematically described in Figure 3(a). For an FL mica nanosheet with a hierarchical structure ranging from monolayer to multilayer, C-AFM maps show that even an FL mica monolayer behaves as an insulating layer up to an applied voltage of 2 V (Figures 3(b) and (c)). We measured tip I-V curves at 9 randomly selected monolayer locations and 33 bilayer locations by ramping the applied voltage from 0 to 10 V (Figure 3(d)). The results indicate highly uniform crystal quality and dielectric behavior: breakdown voltages are relatively stable, with typical monolayer breakdown $\sim$4.5 V and bilayer breakdown $\sim$6.5 V, corresponding to a maximum local breakdown strength on the order of $\sim$45 MV/cm. Using a metal-insulator-metal (MIM) structure on sapphire substrates, we estimated the permittivity of FL mica nanosheets based on a parallel plate capacitor model (Figures 3(e) and (f)). Capacitance-frequency (C-F) and capacitance-voltage (C-V) measurements from different devices yield an average $\varepsilon_{\rm r}$ of 6.09 (Figures 3(g) and (h)).

The favorable dielectric properties and facile preparation of large-area nanoflakes motivate the use of FL mica as a gate dielectric in low-dimensional microelectronic devices. We fabricated 2D FETs in which an exfoliated

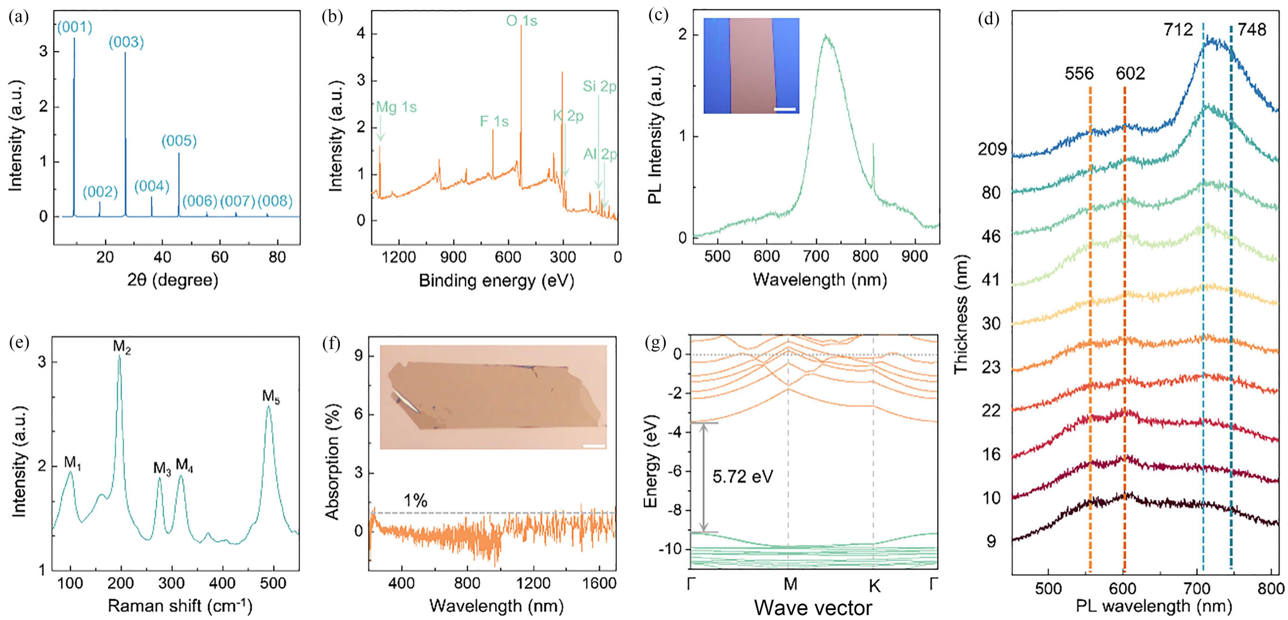

Figure 2 (Color online) Spectroscopic characterization of FL mica. (a) X-ray diffraction (XRD) spectrum of FL mica; equally spaced characteristic peaks correspond to a series of (001) facets. (b) X-ray photoelectron spectroscopy (XPS) of FL mica. (c) Photoluminescence (PL) spectrum of an exfoliated FL mica nanosheet with a characteristic peak near 720 nm. Inset: photograph of the tested sample (thickness of ∼300 nm). Scale bar: 10 μm. (d) Thickness-dependent PL spectra of FL mica showing two characteristic groups of peaks. (e) Raman spectrum of FL mica with five characteristic peaks. (f) Absorption spectrum of FL mica, showing negligible absorption from the ultraviolet to the mid-infrared range. Inset: photograph of the tested sample. Scale bar: 10 μm. (g) Theoretically calculated electronic band structure of FL mica, showing an ultra-large bandgap of ∼5.72 eV.

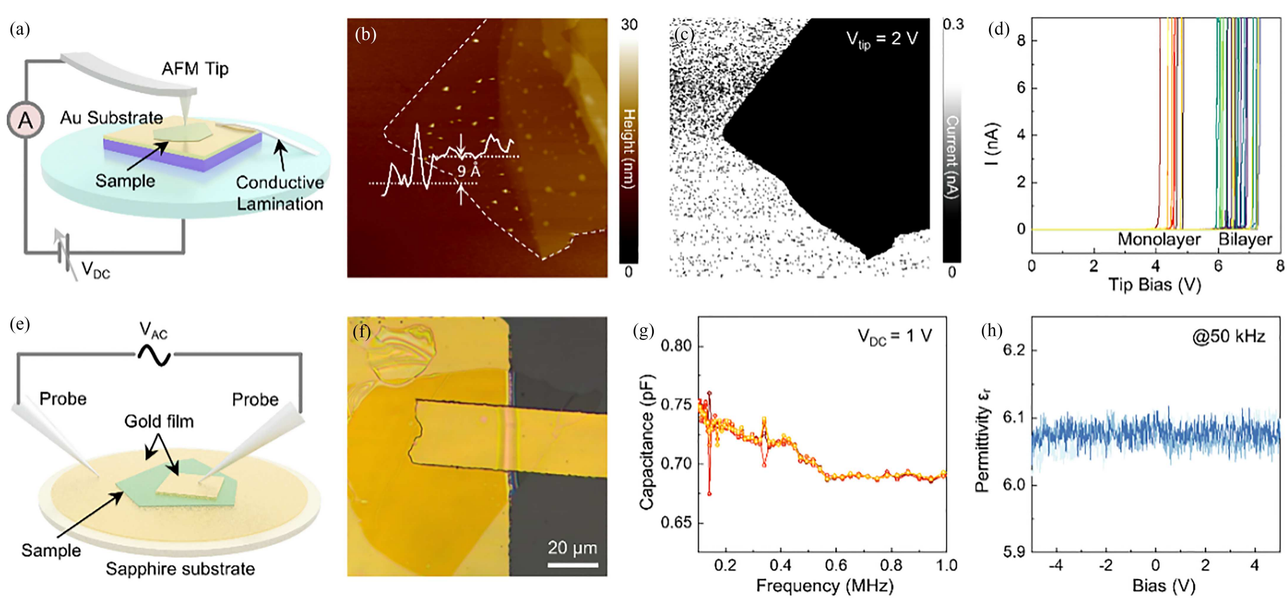

Figure 3 (Color online) Dielectric characterization of FL mica. (a) Schematic of conductive atomic force microscopy (conductive AFM, C-AFM) measurement using a conductive tip to collect tip-substrate current signal. (b) Topography of an exfoliated FL mica nanosheet with hierarchical thickness. (c) C-AFM current map at the same location as (b). (d) Tip current-voltage (I-V) curves measured by C-AFM at randomly selected monolayer and bilayer locations. (e) Schematic of the metal-insulator-metal (MIM) structure characterization based on a parallel plane capacitor geometry. (f) Optical photograph of the MIM device in which an FL mica nanosheet is sandwiched between top and bottom gold electrodes. (g) Frequency-dependent capacitance measurements from five MIM samples with different FL mica thicknesses. (h) Capacitance-voltage (C-V) measurements of MIM samples at a constant frequency of 50 kHz.

MoS_2 nanosheet serves as the channel semiconductor and an exfoliated FL mica is dry-transferred as the top-gate dielectric. The device schematic structure and optical microscopic photograph are shown in Figures 4(a) and (b). Cross-sectional TEM characterization of the device suggests that the 2D vdW heterojunction formed by vdW stacking provides improved interlayer contact, facilitating exploitation of the channel and dielectric prop-

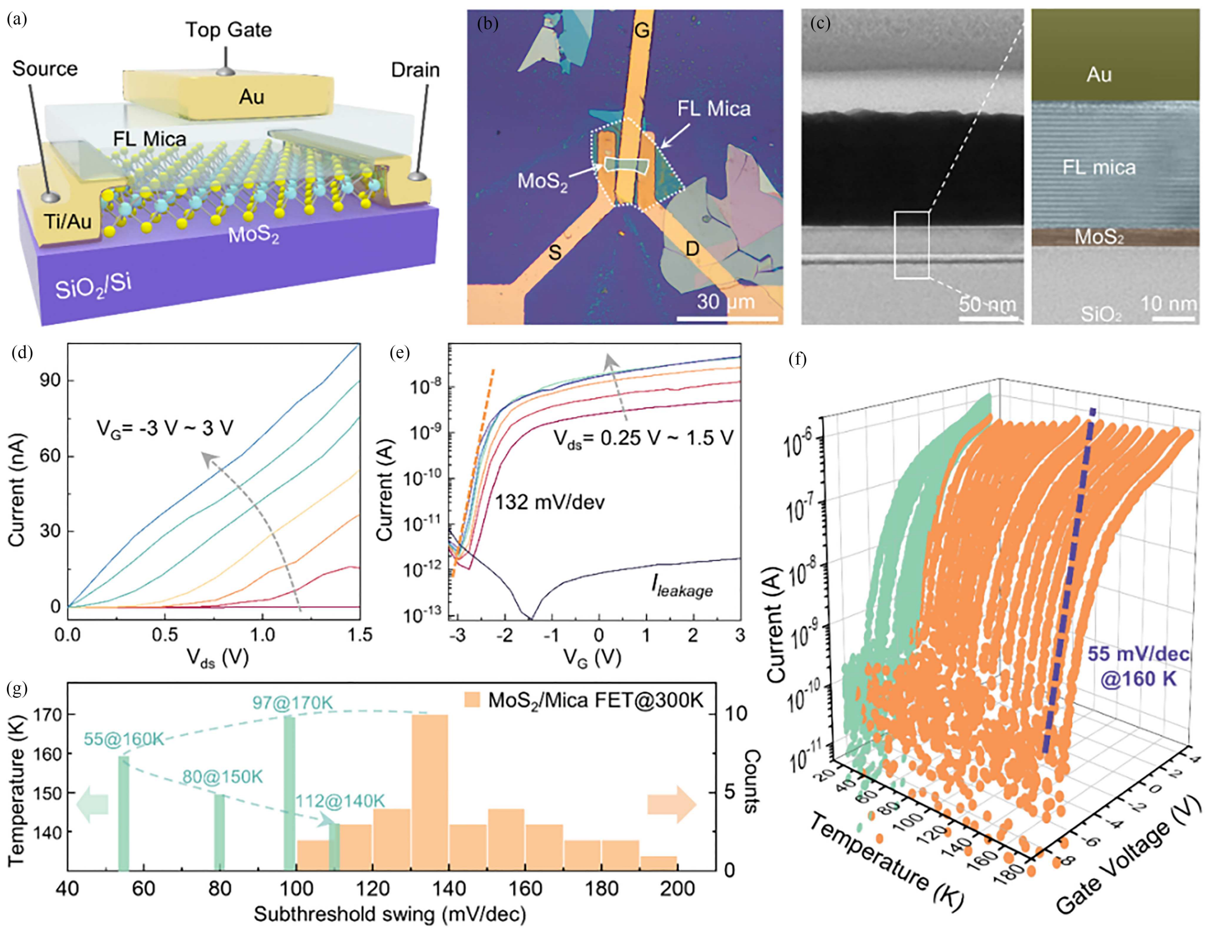

Figure 4 (Color online) Electrical transport characterization of field-effect transistors (FETs) formed by a MoS_2 channel and FL mica gate dielectric. (a) Schematic of the vdW heterostructure FET; (b) optical micrograph of the FET device; (c) cross-sectional TEM image showing the atomic configuration of the heterostructure FET; (d) output curves (I_{ds}-V_{ds}) of the FET device; (e) transfer curves (I_{ds}-V_g) of the FET device at room temperature; (f) temperature-dependent transfer curves of the FET, showing minimal SS of 55 mV/dec at 160 K (green curves are projections of the orange curves); (g) statistical plots of SS values for multiple FETs (yellow curves) and the variation of SS with different temperatures (green curves).

erties (Figures 4(c) and S6). Room-temperature output and transfer curves (Figures 4(d) and (e)) demonstrate effective gate control of channel current, including very low leakage current (~1 pA) and a SS ~132 mV/dec. In high-voltage transfer-curve tests, FL mica employed in 2D MoS_2 transistors exhibits a high breakdown strength of ~29.2 MV/cm (Figure S7); the slight difference between this transistor-based value and C-AFM local measurement (~45 MV/cm) can be attributed to local fluctuations in FL mica performance and differences in measurement geometry. Low-temperature transport measurements reveal a nonmonotonic temperature dependence of SS: as temperature decreases, SS first decreases and then increases, reaching a minimum value of ~55 mV/dec at 160 K (Figure 4(f)). Lower temperature reduces phonon scattering from the lattice thermal vibrations, so the scattering due to ionized impurities in the semiconductor and dielectrics becomes comparatively more important and can dominate mobility at low temperatures. Sulfur vacancy defects in MoS_2 and point defects in FL mica can enhance ionized impurity scattering and thus limit mobility at a relatively low temperature (i.e., below 160 K); this interpretation is generally consistent with the experimental trends. By statistically analyzing multiple devices, we find that a representative room-temperature SS value of ~130 mV/dec is reasonable for the structures studied. The interface trap density (Dit) between the MoS_2 channel and the gate dielectric FL mica can be estimated based on the SS to verify the reliability of the vdW contact. The Dit can be calculated by the equation: $SS = (kT/q) \cdot \ln(10) \cdot (1 + \frac{C_{\rm dep}+q\cdot {\rm Dit}}{C_{\rm ox}})$, where T is the absolute temperature, k is the Boltzmann constant, $C_{\rm ox}$ represents the dielectric capacitance ($C_{\rm ox} = \varepsilon_{\rm ox} \cdot \frac{\varepsilon_0}{t_{\rm ox}}$, where $t_{\rm ox}$ is the thickness of gate dielectric), and q denotes the elementary charge. In the specific device, the FL mica has a $\varepsilon_{\rm r}$ of 6.09 and a thickness of 30 nm, with a gate dielectric capacitance of 1.977×10^{-7} F/cm^2. Since the 2D semiconductor channel thickness is less than 10 nm, the depletion layer capacitance $C_{\rm dep}$ could be negligible. From this relation, we extract Dit $\approx 1.44 \times 10^{12}$ eV/cm^2.

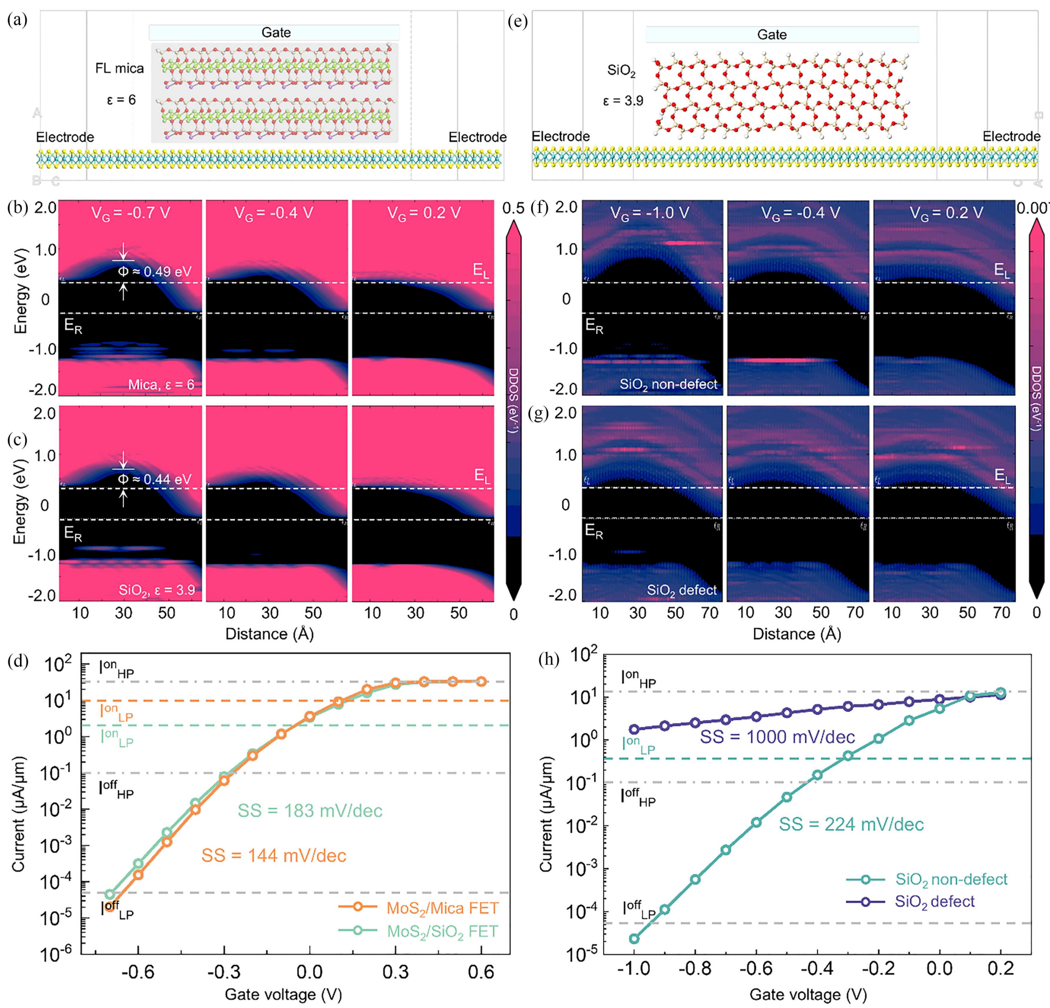

Figure 5 (Color online) Theoretical simulations of electrical performance for monolayer MoS_2-based FETs with different gate dielectrics. (a) Schematic of the FET model based on the FL mica/MoS_2 vdW heterostructure. PLDOS for electrons in (b) FL mica/MoS_2 and (c) SiO_2/MoS_2 configurations, respectively. E_L: energy level of the left electrode; E_R: energy level of the right electrode; Φ: potential barrier. (d) Simulated transfer curves for FETs using pseudo-FL mica and pseudo-SiO_2 gate dielectrics to examine the influence of ε_r on device performance. (e) Schematic of the FET model based on SiO_2/MoS_2 heterostructure. PLDOS spectrum of electrons in (f) non-defect SiO_2/MoS_2 and (g) defect-SiO_2/MoS_2 configurations, respectively. (h) Simulated transfer curves of the FET by using true atomic structures of SiO_2 with and without defects as gate dielectrics to examine the influence of dielectric defects on FET performance. Gray dashed lines and colorful dashed lines (i.e., orange, green, and purple) are indicated standards of ITRS 2028 and the open-state current of corresponding devices, respectively. I^{on}: open-state current; I^{off}: off-state current; HP: high performance; LP: low power.

The temperature dependence of SS shown in Figure 4(g) (green bars) is reproducible across devices and provides insight into low-temperature transport in 2D-materials FETs.

To further understand how 2D vdW dielectrics affect fully 2D FET performance from first principles, we conducted DFT-based simulations to compare MoS_2 devices with FL mica and with silicon dioxide as the gate dielectric layer (Figure 5(a)). Theoretical optimization suggests an energetically favorable contact configuration for FL mica on MoS_2 (Figure S8). In the 2D-MoS_2 FET model, the effect of ε_r on the gate control capability and transport properties of monolayer MoS_2 FETs is analyzed, in which the gate dielectric is assigned different ε_r, 6 for FL mica and 3.9 for SiO_2, respectively. The projected local density of states (PLDOS) as a function of gate voltage (Figures 5(b) and (c)) indicates that the band structure of MoS_2 is modulated more strongly with an FL mica dielectric than with SiO_2. Consequently, the current increases faster with gate voltage for the FL mica case (Figure S9), yielding a simulated SS of ∼144 mV/dec—consistent with experimental results and meeting the standards of international technology roadmap for semiconductors 2028 (ITRS 2028) (Figure 5(d)). These simulations highlight the general principle that, under ideal conditions, a higher ε_r always improves gate control. However, that conclusion assumes an ideal, defect-free interface.

In practice, many interfacial problems arise when combining nonlayered dielectrics such as SiO_2 with atomically thin MoS_2 channels to form a metal-oxide-semiconductor structure. We compared device models with passivated, defect-free SiO_2 and models with SiO_2 containing interface defects on a monolayer MoS_2 channel (Figure 5(e)). The simulations show that defect-induced local charge and screening severely weaken the gate control capability of the FET by shielding the gate electric field (Figures 5(f) and (g)). As a result, for an atomically thin 2D vdW semiconductor, dangling bonds on nonlayered dielectrics surface and fabrication-induced defects can dramatically degrade FET performance—for example, increasing SS from $\sim$224 mV/dec to $\sim$1000 mV/dec in the defective models (Figure 5(h)). For large-scale integration of 2D vdW semiconductors, dielectrics that form vdW contacts (i.e., layered dielectrics) are promising candidates to preserve gate control and support continued device scaling.

4 Conclusion

This study demonstrates that FL mica is a promising insulator for 2D electronics, combining a ε_r of 6 with an ultra-large breakdown strength (45 MV/cm, locally measured). The mature production processes, low cleavage energy, ideal van der Waals (vdW) layered structure, and favorable dielectric properties make FL mica a strong candidate for large-scale 2D vdW integration. Experimentally, the FET based on exfoliated MoS_2 with FL mica exhibits robust gate control capability ($SS \approx 132$ mV/dec at room temperature and a minimum $SS \approx 55$ mV/dec at 160 K). Theoretical modeling shows advantages of FL mica relative to SiO_2, which has a smaller ε_r of 3.9 and a nonlayered structure. The calculated results also reveal that the interface contact of gate dielectric and channel material would exert a critical influence on transistor performance. Therefore, FL mica, as a newly recognized dielectric, not only introduces an important member to the family of vdW layered dielectrics, but also offers new possibilities for 2D vdW integration as well as the construction of micro/nano-devices.

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Supporting information Figures S1–S9. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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