Supporting Information

2D Fluorophlogopite Mica as Van der Waals Dielectrics for High-Breakdown-Strength Field-Effect Transistors

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S1. Distributions of the electric field and potential in the 2D FET simulated by TCAD

Considering that MoS_2 in the 2D FET is a natural n-type semiconductor, it exhibits an ON state (conductive state) without gate voltage. Therefore, as a complement to the DFT simulations, in TCAD simulations, we produce the n-type characteristics of the MoS_2 channel by adding charges to it.

The device model includes a top gate electrode, a FL mica gate dielectric, a MoS_2 channel, and a SiO_2 substrate from top to bottom, wherein the thicknesses of the dielectric, MoS_2 and substrate are 26 nm, 7 nm, and 300 nm, respectively. The distributions of electric field and potential are shown in **Figure S9**.

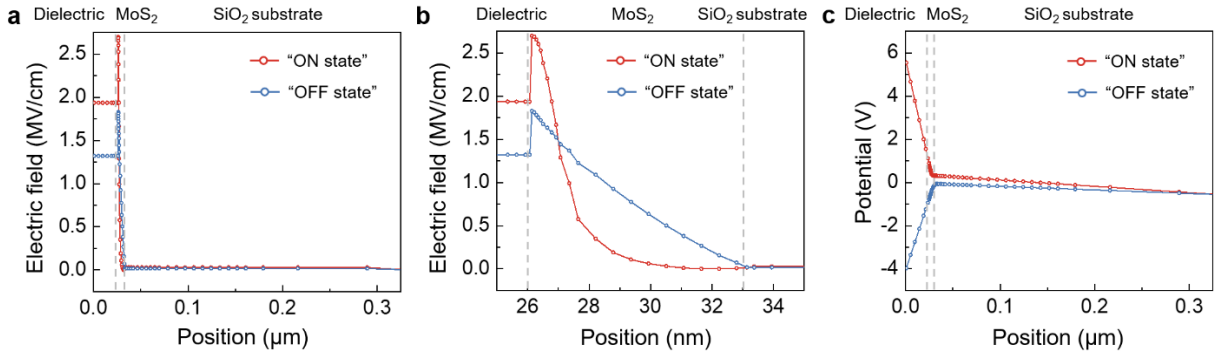

Figure S1. Electric field distribution and potential distribution along the vertical direction in the 2D FET device. **a,** The electric field distribution among the gate dielectric, MoS_2 channel, and SiO_2 substrate. **b,** The magnified region of electric field distribution around MoS_2 channel. **c**, The potential distribution of the MoS_2-based 2D FET with FL mica as the gate dielectric.

Since the dielectric constant of FL mica is larger than that of MoS_2 and SiO_2 substrate, the electric field distribution in **Figure S1 a** well illustrates the rule that the electric field strength is inversely proportional to the dielectric constant. In **Figure S1 b**, it can be seen that even when the 2D FET is in the off state, charge carriers in the MoS_2 channel can effectively deplete the gate electric field, making the electric field approach zero at the bottom surface of the channel and in the SiO_2 substrate. The potential distribution also well demonstrates that almost all the gate voltage is dropped in the gate dielectric and the channel, with almost no voltage drop on the substrate. Therefore, the substrate has no significant effect on the performance simulation

of the MoS_2-based 2D FET device, whether in the ON state, subthreshold region or OFF state. The conclusions drawn by TCAD and DFT simulation methods are reliably consistent.

S2. Elemental composition of FL mica

Since FL mica is consisted of six elements, including K, Mg, Al, Si, O, and F, it is of necessity to confirm the existence and distribution of the elements. Therefore, EDS mapping in TEM characterization is carried out for analyzing a FL mica nanoflake (**Figure S2 a-h**).

Experimentally, it is suggested that the six elements distribute evenly on the FL mica nanoflake. Because of the rich variety of contained elements, vacancy defects would occur within FL mica, which is to some extent illustrated by the discrepancy between the semi-quantitative analysis results of surface elements by EDS and the ideal stoichiometric ratios of chemical formula, $KMg_3AlSi_3O_{10}F_2$ (**Figure S2 i**).

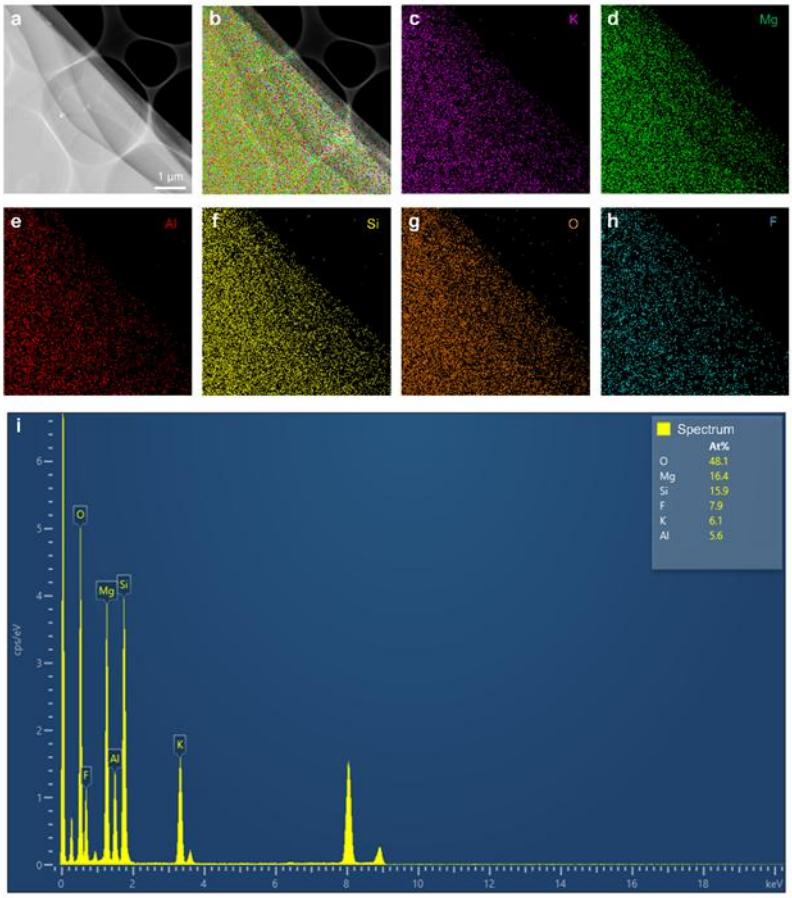

Figure S2. Elemental composition of FL mica. **a**, Morphology of a FL mica nanoflake characterized by TEM. **b**, Elemental distribution of total six elements. **c-h**, Elemental distribution of K, Mg, Al, Si, O, and F, respectively. **i**, Semi-quantitative analysis results of surface elements by EDS, which show a slight deviation from the ideal stoichiometric ratio.

S3. Single-crystal FL mica substrates with different sizes

FL mica is widely recognized as an excellent substrate material for semiconductor epitaxial or deposition growth. Unlike muscovite mica which exist widely in nature, FL mica is a completely synthetic crystal with a vdW layered structure. It is purely prepared with a variety of sizes, including 2-inch, 2×2 cm^2, and 1×1 cm^2, which are shown in **Figure S3**.

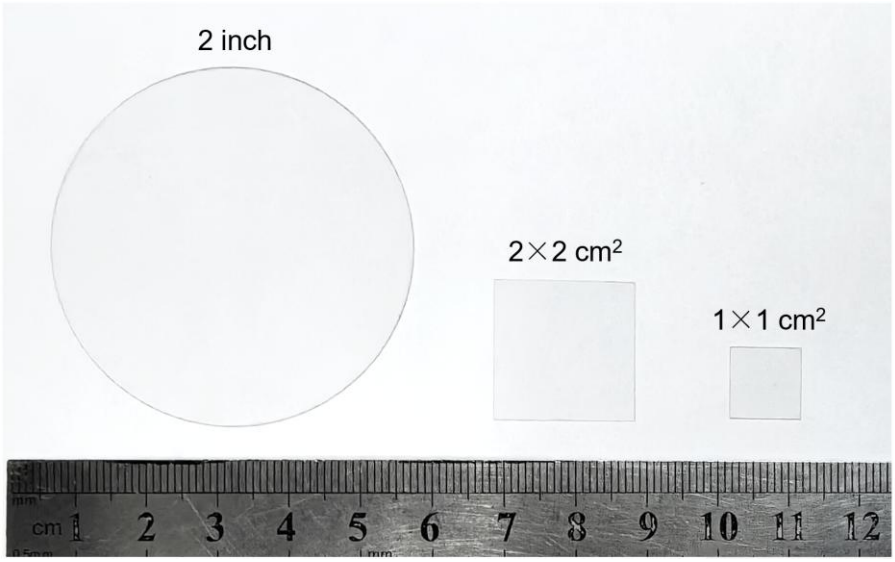

Figure S3. Single-crystal FL mica with different sizes of 2-inch, 2×2 cm^2, and 1×1 cm^2.

S4. Cleavage energy of FL mica

The cleavage energy of FL mica is calculated as:

$$E = \frac{\Delta E}{A} = \frac{0.65\ eV}{1273\ \text{Å}^3 \div 51\ \text{Å}} = 26.04\ meV/\text{Å}^2$$

Where ΔE is the calculated total energy change of the crystal cell when the surface layer is artificially moved along the out-of-plane direction, A is the area of the in-plane FL mica cell, which is calculated by dividing the volume the height. (**Figure S4**).

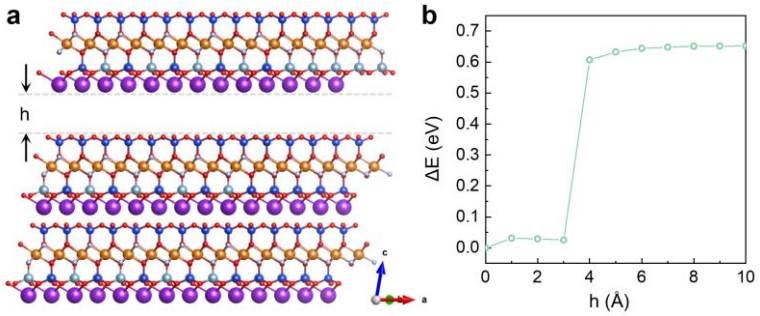

Figure S4. Cleavage energy of FL mica. **a**, Schematic of the modeling on calculation of the cleavage energy by artificially move up the top layer. **b**, The total energy change of the calculated FL mica crystal cell.

S5. The electron diffraction of FL mica single crystal

Selected area electron diffraction (SAED) analysis of mechanically exfoliated FL mica nanoflake is performed, and the electron diffraction spectra obtained from the [010] directions are shown in **Figure S5**, which confirms the triclinic lattice configuration of FL mica.

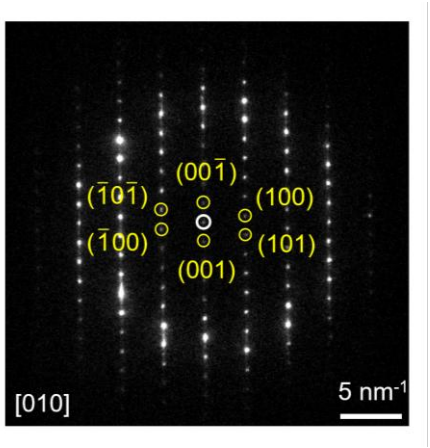

Figure S5. The selected area electron diffraction pattern of single-crystal FL mica nanoflake along [010] crystal direction.

S6. Cross-sectional characterization of FL mica/MoS_2 FET device

To further illustrate the vdW contact and elemental distribution of the FL mica and MoS_2 in FET device, focused ion beam (FIB) and high-resolution transmission electron microscopy (HRTEM) are used to transect and visualize contact and composition distribution.

The vdW contact between MoS_2 and FL mica can be clearly seen, as well as the distribution of the six elements, K, Mg, Al, Si, O, and F in the FL mica, and the distribution of Mo and S in the MoS_2, shown in **Figure S6**.

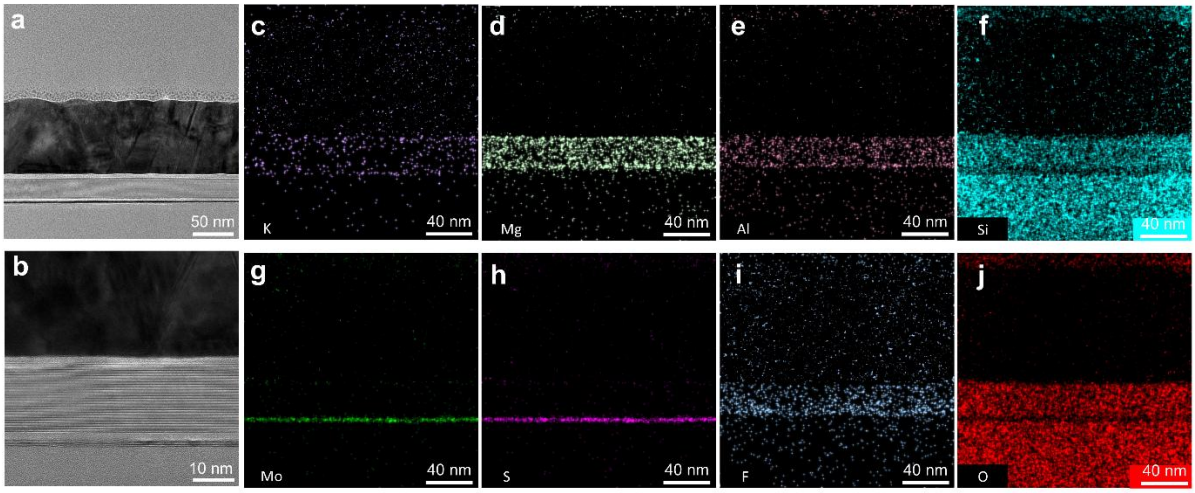

Figure S6. Cross-sectional TEM and EDS mapping of FL mica/MoS_2 FET device. **a**, The cross-sectional morphology of FL mica/MoS_2 FET device. **b**, The zoomed-in view of a. **c-j**, The EDS mapping of the elemental distribution analysis of K, Mg, Al, Si, Mo, S, F, and O, respectively.

S7. Breakdown strength of FL mica dielectrics in MoS_2-based transistors

Different from the C-AFM test in which the conductive probe tip with a sub-nanometer size tests the local dielectric properties of FL mica, when FL mica is used as a gate dielectric to work in a MoS_2 transistor, it may exhibit distinguished breakdown electric field strengths in the top-gate FET architecture. Therefore, it is of necessity to exert high voltage to the top gate and verify the dielectric performance of FL mica from the perspective of device.

In this case, a 2D MoS_2 transistor was constructed by using a FL mica as gate dielectric with a thickness of ~12 nm. The top-gate voltage was swept from -4 V to 35 V, indicating a maximum electric field strength exerted to FL mica would reach ~29.2 MV/cm. As shown in **Figure S7**, it is suggested that the 2D MoS_2 transistor with FL mica gate dielectrics can be stabilized in the saturation region under high gate voltage and the leakage current can be maintained at a low level of ~10 fA, demonstrating the advantages of large bandgap and high-voltage resistance of FL mica.

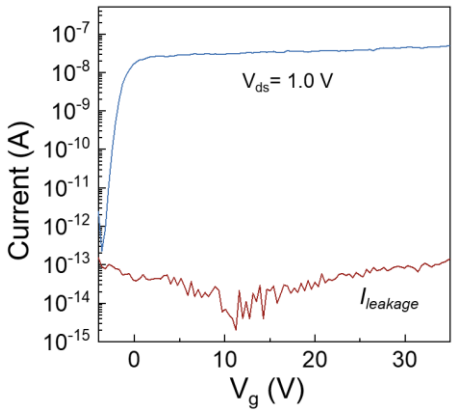

Figure S7. High-voltage test for the top-gate MoS_2 transistor. Transfer curve of the 2D MoS_2 transistor under a Vds of 1.0 V with a high gate voltage range from -4 V to 35 V.

S8. Simulation on the contact configuration between FL mica and MoS_2

Due to the structure of the interlayer intercalation of Potassium (K) ions in the FL mica single crystal, there is no overall symmetry along the vdW stacking direction (out-of-plane direction) in a single unit cell. Considering either the K-atom side or the O-atom side in contact with MoS_2 during device simulations will affect the reliability of the final conclusions. Therefore, it is necessary to perform energy calculations on heterostructures with different contact configurations before device simulation to find out the contact configuration with the lowest energy of the system.

Four contact configurations are simulated with calculated energy of -207.667 eV, -207.595 eV, -207.550 eV, and -207.554 eV, respectively. The schematic of the models is shown in **Figure S8**. It is suggested that the lowest system energy occurs when FL mica is contacted with MoS_2 using the K-atom side.

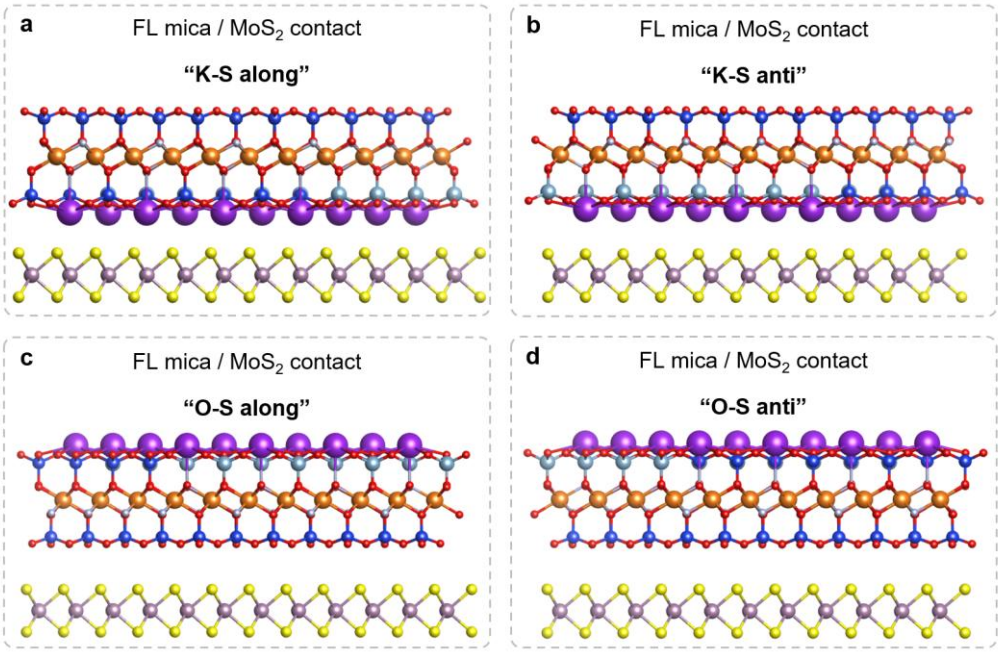

Figure S8. Four contact configurations of FL mica/MoS_2 heterostructure. **a-b**, FL mica is contacted with MoS_2 using the K-atom side but opposite in-plane orientation. **c-d**, FL mica is contacted with MoS_2 using the O-atom side but opposite in-plane orientation.

S9. Transmission spectra of 2D FET devices with different gate dielectrics

The transmission spectra of electrons from the left electrode to the right electrode at different gate voltages are employed to provide information about the performance of FETs with different gate dielectrics.

More transmission spectra of FETs when four gate dielectrics (FL mica with ε of 6, SiO_2 with ε of 3.9, non-defect SiO_2, and defect SiO_2) are employed at different gate voltages are displayed in **Figure S9**. From the modulation effect of the gate voltage on the device barriers, it is suggested that the switching performance of the FETs is optimal when FL mica with a large dielectric constant under vdW contact is used as the gate dielectrics. In addition, the simulation results also illustrate that SiO_2 gate dielectrics with non-ideal contacts and rich in defects are unfavorable for transistors with 2D semiconductors as channels.

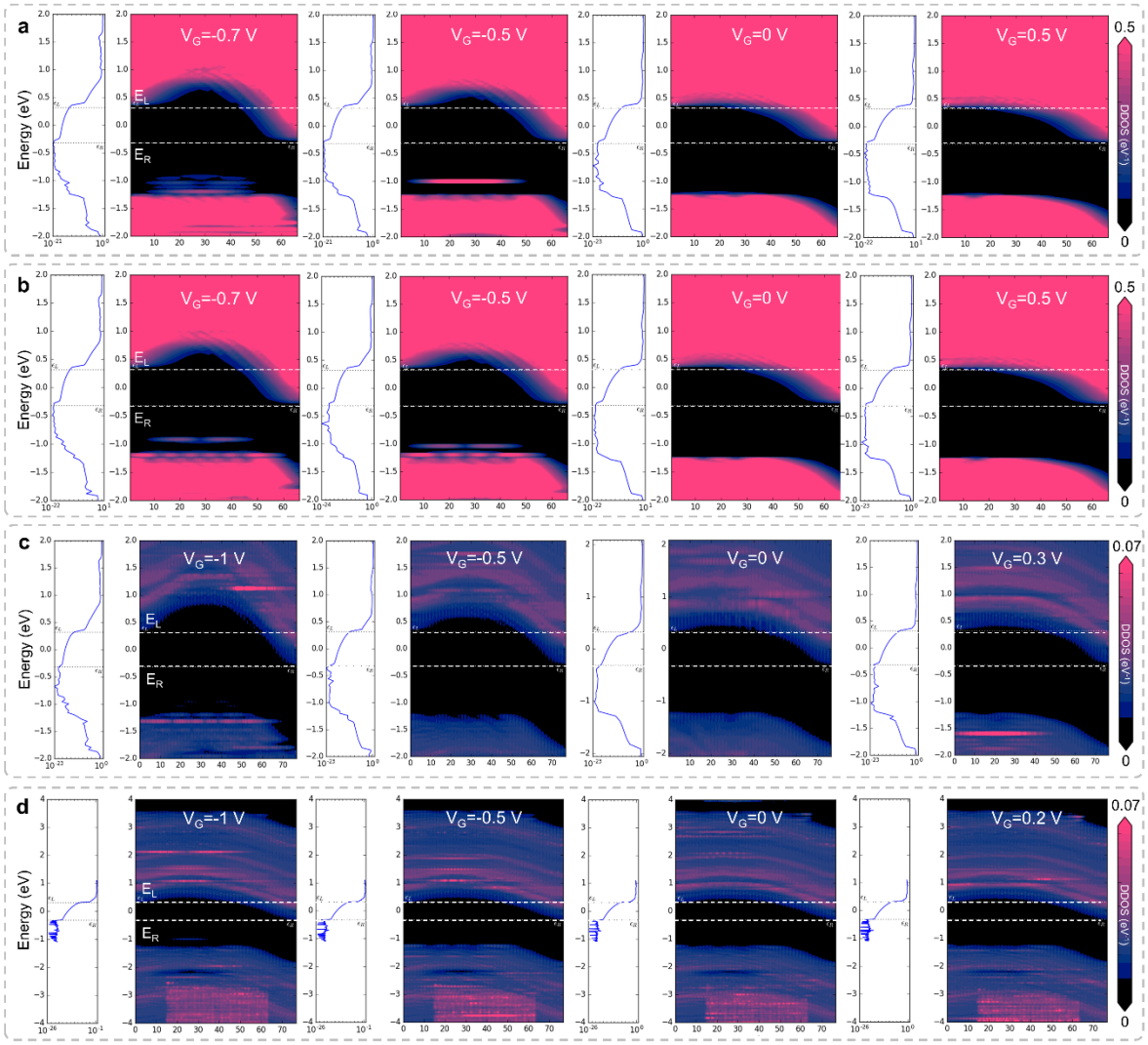

Figure S9. Transmission spectra of 2D FET devices with different gate dielectrics. **a,** PLDOS spectra of ideal FL mica/MoS_2 FET with gate dielectric constant of 6, indicating energy barriers controlled by gate voltages of -0.7 V, -0.5 V, 0 V, and 0.5 V, respectively. Left panel is the corresponding transmission spectrum. **b,** PLDOS spectra of ideal SiO_2/MoS_2 FET with gate dielectric constant of 3.9 without considering real contact, indicating energy barriers controlled by gate voltages of -0.7 V, -0.5 V, 0 V, and 0.5 V, respectively. **c,** PLDOS spectra of real SiO_2/MoS_2 FET without defects, indicating energy barriers controlled by gate voltages of -1 V, -0.5 V, 0 V, and 0.3 V, respectively. **d,** PLDOS spectra of SiO_2/MoS_2 FET with considering real contact and defects, indicating energy barriers controlled by gate voltages of -1 V, -0.5 V, 0 V, and 0.2 V, respectively.