

# E-mode reverse p-i-n junction gate GaN HEMT with high $V_{TH}$ and enhanced gate drive voltage

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Received 2 May 2025/Revised 21 July 2025/Accepted 14 November 2025/Published online 29 April 2026

**Citation** Jia M, Hou B, Yang L, et al. E-mode reverse p-i-n junction gate GaN HEMT with high  $V_{TH}$  and enhanced gate drive voltage. *Sci China Inf Sci*, 2026, 69(8): 189404, <https://doi.org/10.1007/s11432-025-4679-4>

P-GaN HEMTs are selected as a power switching device by miniaturized high-frequency switching power supplies due to their process maturity and fast switching speed, and their production value is increasing year by year [1]. However, they still face several critical challenges. First, the gate drive voltage of p-GaN HEMTs is low, which leads to issues such as increased power loss due to insufficient overdrive voltage and challenges related to gate reliability [2]. In addition, the parasitic capacitance present in the topology induces voltage spikes when it is subjected to the high  $dV/dt$  during switching. This would cause erroneous turn-on of p-GaN HEMTs with low threshold voltage ( $V_{TH}$ ), compromising circuit functionality and stability [3]. Enhancing both the  $V_{TH}$  and the gate operating range would not only improve operational safety but would also enable higher current handling, faster switching speeds, and better compatibility with Silicon-Based drive solutions.

To achieve the aforementioned performance enhancements simultaneously, a reverse p-i-n junction gate enhancement-mode GaN high electron mobility transistor (PIN-HEMT) is proposed, which is fabricated by sequentially growing an i-GaN layer and an n-GaN layer above the conventional p-GaN gate. Technology Computer-Aided Design (TCAD) simulation of this novel structure has been published [4]. This study further demonstrates the feasibility and superiority of the structure from an experimental perspective.

**Experiment.** The structure and energy dispersive spectroscopy of PIN-HEMTs are shown in Figures 1(a)–(c). Details of the growth epitaxy and device fabrication process can be found in Appendix A.

**Results and discussion.** Figure 1(d) illustrates the transfer characteristics of the P-HEMT and PIN-HEMT. All devices have an on/off ratio of  $10^9$ , with a  $V_{TH}$  of 0.5 V for the P-HEMT, which is increased to 2.6 V for the PIN-HEMT. Besides, the PIN-HEMT maintains an ultra-low  $V_{TH}$  hysteresis of 50 mV. The subthreshold swing (SS) of the PIN-HEMT is hardly affected, with an extracted SS of 88 mV/dec. Figure 1(e) demonstrates the transfer characteristics in linear coordinates. The transconductance of the PIN-HEMT peaks at 27.0 mS/mm, which is compared with the

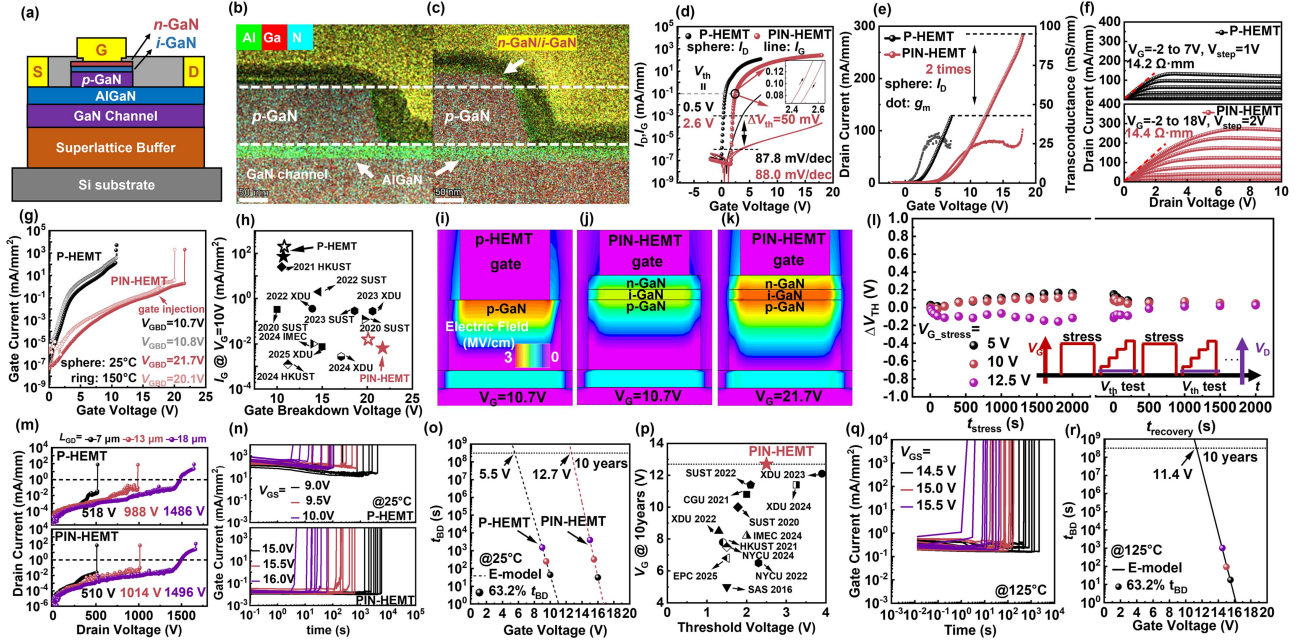
31.8 mS/mm of the P-HEMT with a slight decrease.

Figure 1(f) shows the output characteristics of the P-HEMT and PIN-HEMT. Owing to the limitations of gate leakage current, the conventional Schottky-gate p-GaN HEMT operates at a gate voltage of 7 V, achieving a saturation current density of 133 mA/mm and an on-resistance of  $14.2 \Omega \cdot \text{mm}$ . In contrast, the PIN-HEMT delivers a significantly higher output current density of 273 mA/mm at a gate voltage of 18 V. This substantial improvement in high-current drive capability is achieved while maintaining a nearly consistent on-resistance of  $14.4 \Omega \cdot \text{mm}$ .

Figure 1(g) demonstrates the forward gate breakdown characteristics of P-HEMTs and PIN-HEMTs. The gate breakdown voltage of the P-HEMT is 10.7 V at 25°C. This value is 10.8 V at 150°C. The forward gate breakdown voltages of the PIN-HEMTs are 21.7 V at 25°C and 20.1 V at 150°C, respectively. Figure 1(h) compares the gate leakage and breakdown characteristics of published p-GaN HEMTs. PIN-HEMTs consistently have excellent gate breakdown characteristics at 25°C and 150°C while maintaining very low gate leakage, which are the state-of-the-art values in recent years. Figures 1(i)–(k) demonstrate the gate electric field distribution for P-HEMT and PIN-HEMT. At a gate voltage of 10.7 V, the peak electric field in the P-HEMT reaches 3 MV/cm. When the gate is biased at 21.7 V, the peak electric field in the PIN-HEMT reaches 3 MV/cm, which is in exact agreement with the experimentally measured results. For the P-HEMT, the electric field is mainly focused at the Schottky metal/p-GaN interface. For the PIN-HEMT, the peak electric field is significantly decreased and uniformly distributed on the reverse p-i-n junction, which significantly improves the gate breakdown voltage.

Figure 1(l) illustrates the  $V_{TH}$  shift characteristics of the PIN-HEMT. The  $\Delta V_{TH}$  of the PIN-HEMT is maintained within 0.2 V after 2000 s at  $V_{G\text{stress}}$  of 5, 10, and 12.5 V, and the  $\Delta V_{TH}$  recovers to the normal level after the stress is withdrawn for 500 s, which proves that the PIN-HEMTs have a good  $V_{TH}$  stability. Figure 1(m) shows the off-state drain breakdown characteristics of the P-HEMT. The breakdown voltages of the P-HEMT are 518/988/1486 V for  $L_{GD}$  of 7, 13, and 18  $\mu\text{m}$  ( $I_D = 1 \text{ mA/mm}$ ), respectively, and the corresponding breakdown voltages of the

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**Figure 1** (Color online) (a) Device structure of the PIN-HEMTs; cross-sectional energy dispersive spectroscopy (EDS) of the (b) P-HEMTs and (c) PIN-HEMTs; transfer characteristic in (d) logarithmic coordinate and (e) linear coordinate; (f) output characteristic; (g) gate breakdown characteristics at 25°C and 150°C and (h) comparison for gate breakdown voltage and forward gate leakage at  $V_G$  of 10 V; (i) the electric field distribution of the (i) P-HEMTs and (j) PIN-HEMTs at  $V_G$  of 10.7 V; (k) the electric field distribution of the PIN-HEMTs at  $V_G$  of 21.7 V; (l)  $\Delta V_{TH}$  characteristics of PIN-HEMT under with various gate stress biases; (m) off-state breakdown characteristic; (n) time-dependent gate leakage current characteristics at room temperature; (o) gate lifetime prediction at room temperature; (p) comparison of  $V_{TH}$  and the maximum applicable gate voltage between this work and the other previous studies; (q) time-dependent gate leakage current characteristics of PIN-HEMTs at 125°C; (r) gate lifetime prediction of the PIN-HEMTs at 125°C.

PIN-HEMT are 510/1014/1496 V, respectively. This indicates that the reverse p-i-n junction gate structure has no influence on off-state drain breakdown characteristics.

Figure 1(n) monitors the gate leakage currents of P-HEMT and PIN-HEMT during time-dependent gate breakdown (TDGB) testing. It can be observed that the P-HEMT exhibits a significantly higher gate leakage of  $10^2$  mA/mm<sup>2</sup> under a gate stress of 9 V, whereas the PIN-HEMT demonstrates an extremely low gate current density of  $10^{-2}$  mA/mm<sup>2</sup> even at a gate voltage stress of 15 V. Figure 1(o) analyzes the maximum applicable gate voltages of P-HEMT and PIN-HEMT using the E-model fitting method, revealing values of 5.5 V for P-HEMT and an exceptionally high 12.7 V for PIN-HEMT. Figure 1(p) indicates that the PIN-HEMT achieves both high  $V_{TH}$  and gate drive voltage operation, enabling seamless integration of GaN power transistors with silicon-based MOSFETs and their control circuits. Figure 1(q) presents the gate leakage current characteristics of the PIN-HEMT under TDGB testing at 125°C. Notably, it maintains an ultra-low gate current density of  $10^{-1}$  mA/mm<sup>2</sup> even when subjected to 15 V gate bias stress. The maximum applicable gate voltages extracted via E-model fitting are shown in Figure 1(r), yielding 11.4 V at 125°C for a 10-year operating lifetime. These results demonstrate good high-temperature gate reliability of the PIN-HEMT.

**Conclusion.** This work presents a reverse p-i-n junction gate technique that mitigates the peak electric field of a normally-off p-GaN HEMT to achieve a higher gate breakdown voltage of 21.7 V and a gate operating range of 18 V. The PIN-HEMTs also have

a high  $V_{TH}$  of 2.6 V while maintaining an ultra-low subthreshold swing of 88 mV/Dec. While exhibiting almost the same on-resistance (14.4  $\Omega$ ·mm) and drain breakdown voltage as conventional p-GaN HEMTs, as well as excellent  $V_{TH}$  stability, the reverse p-i-n junction gate HEMT demonstrates great potential for GaN power transistors, as evidenced by its higher maximum applicable gate voltage of 12.7 V.

**Acknowledgements** This work was supported in part by National Natural Science Foundation of China (Grant Nos. 62474135, 62234009, 62090014, 62404165), China Postdoctoral Science Foundation (Grant Nos. 2025M770531, 2024M752517), and Fundamental Research Funds for the Central Universities (Grant Nos. ZYTS25218, QTZX25069).

**Supporting information** Appendix A. The supporting information is available online at [info.scichina.com](http://info.scichina.com) and [link.springer.com](http://link.springer.com). The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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