

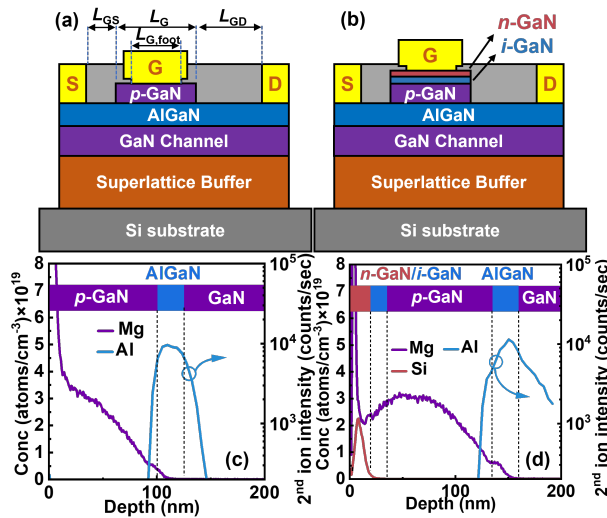
• Supplementary File •

# E-mode reverse p-i-n junction gate GaN HEMT with high $V_{TH}$ and enhanced gate drive voltage

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## Appendix A Growth epitaxy and device fabrication



**Figure A1** Schematic diagram for the (a) P-HEMTs and (b) PIN-HEMTs. Secondary ion mass spectrometry results of (c) P-HEMTs and (d) PIN-HEMTs.

The epitaxial layer grown by metal organic chemical vapor deposition (MOCVD) consists of a 6-inch Si-based substrate, a AlN/GaN superlattice buffer layer and a 1.6  $\mu\text{m}$  GaN channel layer,  $\text{Al}_{0.15}\text{Ga}_{0.85}\text{N}$  barrier layer and 100 nm p-GaN layer with a Mg doping concentration of  $3 \times 10^{19}\text{cm}^{-3}$ . Figure A1(a) shows the structure of conventional p-GaN HEMT under test, which features a p-GaN gate length ( $L_G$ ) of 1.5  $\mu\text{m}$ , a gate-drain distance ( $L_{GD}$ ) of 13  $\mu\text{m}$ , a gate-source distance ( $L_{GS}$ ) of 1  $\mu\text{m}$ , and a gate width ( $W_G$ ) of 100  $\mu\text{m}$ . The length of gate metal foot is 0.7  $\mu\text{m}$ . For PIN-HEMTs, the p-GaN layer is capped with a 15 nm i-GaN and 20 nm n-GaN doped with Si at  $2 \times 10^{19}\text{cm}^{-3}$  are above the p-GaN layer, as shown in Figure A1(b). The corresponding secondary ion mass spectrometry (SIMS) results for the two epitaxial structures are presented in Figure A1(c-d). The preparation process is as follows. First, the PIN-GaN layer in the active region is removed by atomic layer etching (ALE). Subsequent Hall effect measurement results show an electron mobility of  $1380\text{cm}^2/(\text{V}\cdot\text{s})$  and a carrier concentration of  $4.41 \times 10^{19}\text{cm}^{-3}$  at room temperature. The Ti/Al/Ni/Au (20/160/55/45 nm) was deposited by electron beam evaporation, followed by rapid annealing for 60 s in a nitrogen atmosphere at 860  $^\circ\text{C}$  to obtain good ohmic contacts. After device isolation by ion implantation, TiN/Au was deposited as gate metal. According to a transmission line model measurement (TLM), the contact resistance ( $R_C$ ) and sheet resistance ( $R_{SH}$ ) of these devices are approximately 1.1  $\Omega\cdot\text{mm}$  and 572  $\Omega/\text{sq}$ . Then, 120 nm SiN was deposited on the wafer as passivation layer using PECVD. Finally, F-based inductively coupled plasma (ICP) etching was used to complete the via-hole opening step of the metal pad.

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