SCIENCE CHINA
Information Sciences

• LETTER •

August 2026, Vol. 69, Iss. 8, 189402:1–189402:2
https://doi.org/10.1007/s11432-025-4717-9

1.4 kV β-Ga_2O_3 VDMOSFET with high-temperature nitrogen-implanted current blocking layer

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Received 14 August 2025/Revised 24 October 2025/Accepted 15 December 2025/Published online 15 July 2026

Citation Lu X, Hu Y J, Li J J, et al. 1.4 kV β-Ga_2O_3 VDMOSFET with high-temperature nitrogen-implanted current blocking layer. Sci China Inf Sci, 2026, 69(8): 189402, https://doi.org/10.1007/s11432-025-4717-9

The ultrawide bandgap semiconductor beta-phase gallium oxide (β-Ga_2O_3) has emerged as a promising material for next-generation high-power electronics due to its wide bandgap of ∼4.8 eV, high critical breakdown field of ∼8 MV/cm, and an exceptional Baliga's figure of merit (BFOM) of 3444. Furthermore, the availability of low-cost, large-area, and high-quality melt-grown single-crystal substrates makes β-Ga_2O_3 highly attractive for scalable device fabrication.

Vertical metal-oxide-semiconductor field-effect transistor (MOSFET) architectures are well-suited for high-voltage applications, as they allow the breakdown voltage (BV) to scale with drift layer thickness without increasing chip area, enabling higher power density and better volumetric efficiency. Enhancement-mode (E-mode) operation is particularly desirable for power switching applications due to its inherent fail-safe characteristics and simplified gate drive requirements. However, the absence of p-type doping in β-Ga_2O_3 has been a major obstacle to the development of vertical E-mode MOSFETs. Fin-channel β-Ga_2O_3 MOSFETs have emerged as promising vertical power device structures that enhance gate control through multi-facet channel modulation. However, forming such fin geometries requires deep dry etching, which may degrade the β-Ga_2O_3 surface and deteriorate the MOS interface quality, thus limiting device performance and reliability. Recent advances have shown that deep-level acceptor nitrogen (N) ion implantation can induce a quasi-p-type current blocking layer (CBL), offering a practical alternative to conventional p-type doping and enabling vertical MOSFET architectures [1]. Various CBL-based vertical β-Ga_2O_3 MOSFETs have been demonstrated, including current aperture vertical electron transistors (CAVET), vertical diffused barrier FETs (VDBFET), and U-shaped trench-gate MOSFETs (UMOSFET).

Despite these advances, challenges such as excessive leakage current and early breakdown still persist, indicating room for improvement in CBL design and processing. In comparison, vertical double-implanted MOSFETs (VDMOSFETs) have been widely adopted in SiC technologies due to their planar gate structures, which mitigate electric field crowding and avoid the reliability issues associated with trench-gate geometries [2]. Additionally, their inversion-mode channels circumvent the trade-off between threshold voltage (V_{th}) and output current density encountered in CAVET-type devices.

For wide-bandgap semiconductors such as SiC and GaN, ion implantation performed at elevated temperatures has shown remarkable advantages over conventional room-temperature implantation. The high-temperature process provides an in-situ dynamic annealing effect that effectively suppresses implantation-induced lattice damage and enhances impurity activation efficiency, thereby improving dopant electrical activity and preserving crystal quality. Inspired by these findings, our previous work [3] demonstrated that applying high-temperature N ion implantation to β-Ga_2O_3 can similarly mitigate implantation damage and achieve higher acceptor activation, leading to a significantly improved CBL performance. Building upon this foundation, the present work develops β-Ga_2O_3 VDMOSFETs incorporating a high-temperature N-implanted CBL, demonstrating record-high breakdown voltage and power figure of merit among CBL-based β-Ga_2O_3 devices.

Device fabrication. The VDMOSFET was fabricated using a 10-μm-thick β-Ga_2O_3 epitaxial layer with a carrier concentration of 1×10 cm^{-3}, grown on a Sn-doped β-Ga_2O_3 (001) substrate by halide vapor phase epitaxy (HVPE). Figures 1(a) and (b) show the cross-sectional schematic and optical microscope image of the fabricated device, respectively. The device has a gate-to-source spacing (L_{gs}) of 5 μm, gate-to-n$^+$ source overlap (L_{gn}) of 5 μm, channel length (L_{ch}) of 5 μm, JFET region width (L_{jfet}) of 20 μm, half-active region width (L_{act}) of 25 μm, and a source

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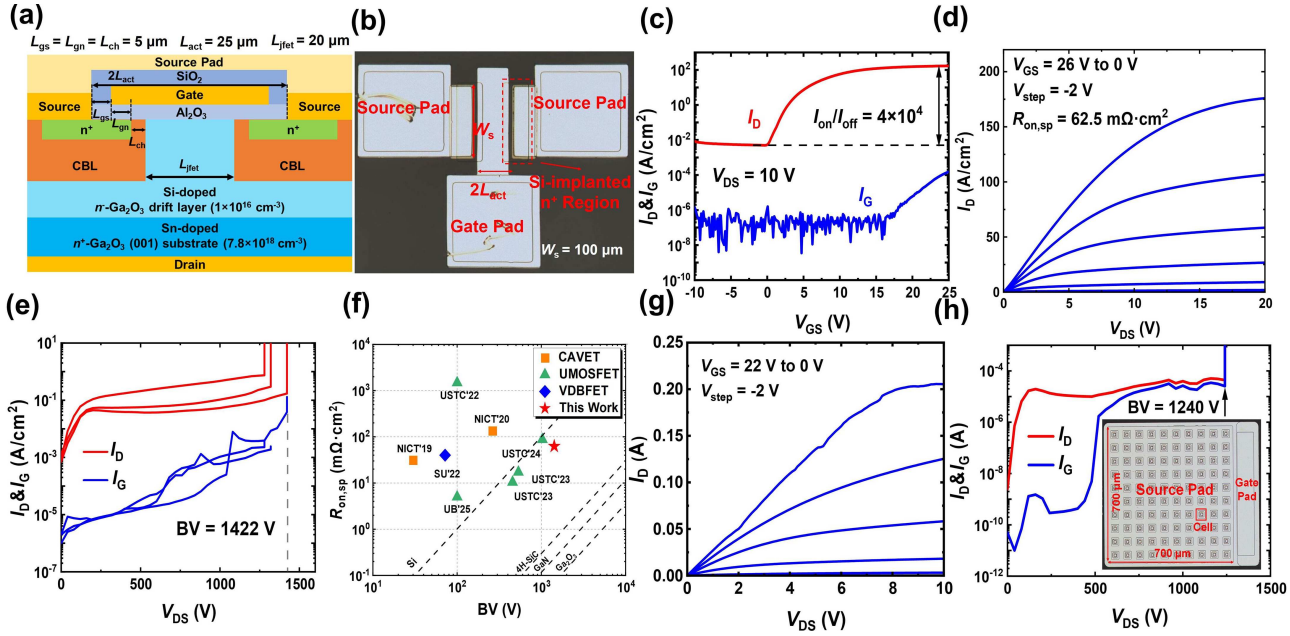

Figure 1 (Color online) (a) Cross-sectional schematic; (b) optical microscope image of the fabricated β-Ga_2O_3 VDMOSFET; (c) transfer, (d) output, and (e) off-state breakdown characteristics of the fabricated β-Ga_2O_3 VDMOSFET; (f) benchmark of $R_{on,sp}$ and BV for state-of-the-art CBL-based vertical β-Ga_2O_3 MOSFETs; (g) output and (h) off-state breakdown characteristics of the fabricated large-area β-Ga_2O_3 VDMOSFET (inset).

width (W_s) of 100 μm. The fabrication process is detailed in Appendix A.

Results and discussion. Figure 1(c) shows the transfer characteristics of the fabricated β-Ga_2O_3 VDMOSFET at V_{DS} = 10 V. The current density and on-resistance are normalized to the half-cell layout, where the effective area is defined as $W_s \times (L_{act} + L_T)$, where L_T refers to transfer length. The device demonstrates E-mode operation with a V_{th} of 5.6 V, attributed to the strong current-blocking capability of the high-temperature N-implanted CBL, which effectively supports quasi-inversion channel formation at high gate bias. The relatively high V_{th} improves noise immunity and reduces the risk of unintended turn-on. The measured on/off current ratio (I_{on}/I_{off}) is 4×10^4. The relatively limited I_{on}/I_{off} is mainly due to vertical leakage through the CBL across the unisolated sample, rather than the device itself. This is confirmed by the similar off-state leakage observed across devices of different sizes, indicating that the leakage current originates from the entire sample area in the absence of device isolation. The output characteristics of the fabricated β-Ga_2O_3 VDMOSFET are shown in Figure 1(d). The device exhibits a maximum drain current (I_D) of 176 A/cm^2 at V_{GS} = 26 V and V_{DS} = 20 V, with an extracted specific on-resistance ($R_{on,sp}$) of 62.5 mΩ · cm^2.

Figure 1(e) shows the off-state breakdown characteristics of the fabricated β-Ga_2O_3 VDMOSFET, which achieves a BV of 1422 V at V_{GS} = 0 V. To the best of our knowledge, this is the highest reported BV for CBL-based vertical β-Ga_2O_3 MOSFETs. Notably, this performance is achieved without any edge termination structures, corresponding to a high average breakdown field of 1.42 MV/cm across the 10 μm drift layer. Figure 1(f) benchmarks the performance of the fabricated device against other state-of-the-art CBL-based vertical β-Ga_2O_3 MOSFETs (Appendix B). The demonstrated power figure of merit (PFOM) of 32.4 MW/cm^2 surpasses the unipolar theoretical limit for Si devices and represents the best reported performance for CBL-based vertical β-Ga_2O_3 MOSFETs to date.

Figures 1(g) and (h) present the output and off-state breakdown characteristics of a fabricated large-area β-Ga_2O_3 VDMOSFET consisting of 100 unit cells within a 700 μm × 700 μm footprint. At V_{GS} = 22 V and V_{DS} = 10 V, the device delivers a maximum I_D of 0.21 A, corresponding to a current density of 42.8 A/cm^2. Furthermore, a high BV of 1240 V is achieved, representing the highest reported value for large-area β-Ga_2O_3 MOSFETs to date.

Conclusion. A β-Ga_2O_3 VDMOSFET employing a high-temperature N-implanted CBL has been successfully demonstrated. Compared to conventional room-temperature implantation followed by high-temperature annealing, the high-temperature implantation process yields significantly improved current blocking capability. The fabricated device demonstrates the highest BV and PFOM values among reported CBL-based vertical β-Ga_2O_3 MOSFETs, highlighting the effectiveness of high-temperature N-implantation in enabling high-performance β-Ga_2O_3 vertical power devices.

Acknowledgements This work was supported in part by National Key Research and Development Program of China (Grant No. 2024YFE0205300), National Natural Science Foundation of China (Grant No. 62471504), and Guangdong Basic and Applied Basic Research Foundation (Grant No. 2025A1515011208).

Supporting information Appendixes A and B. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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