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1.4 kV $\beta - Ga_2O_3$ VDMOSFET with High-temperature Nitrogen-implanted Current Blocking Layer

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Appendix A Device fabrication process

The VDMOSFET was fabricated using a 10-μm-thick $\beta - Ga_2O_3$ epitaxial layer with a carrier concentration of 1×10 cm^{-3}, grown on a Sn-doped $\beta - Ga_2O_3$ (001) substrate by halide vapor phase epitaxy (HVPE). The $\beta - Ga_2O_3$ substrates used in this work were purchased from Novel Crystal Technology, Japan. To form the CBL, N ion implantation was performed at 200 keV, 300 keV, 440 keV, and 600 keV, with a total dose of 2.9×10^{14} cm^{-2} at an implantation temperature of 500 °C, without post-annealing. This process formed a box-like N distribution with a depth of approximately 700 nm and a plateau concentration of 5×10^{18} cm^{-3}, serving as both CBL and quasi-inversion channel. Subsequently, multi-energy silicon (Si) ion implantation with a maximum energy of 180 keV was performed, followed by dopant activation through annealing at 900 °C for 15 minutes in N_2 ambient, resulting in a box-like n^+ source region with a depth of approximately 100 nm and a concentration of 5×10^{19} cm^{-3}. To mitigate implantation-induced surface damage and suppress channel effects, a 100-nm-thick sacrificial SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) prior to the N and Si implantations. The depth profiles of implanted N and Si were simulated using the stopping and range of ions in matter (SRIM), as shown in Figure A1(a). Then, a 50-nm-thick Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD). Ti/Au (50/100 nm) metal stacks were deposited on the $\beta - Ga_2O_3$ drift layer surface and the substrate backside to form the source and drain electrodes, followed by rapid thermal annealing (RTA) at 470 °C for 1 minute in N_2 ambient to achieve ohmic contacts. Following this, Ni/Au (50/100 nm) gate metals were deposited on theAl_2O_3 surface. Subsequently, a 200 nm SiO_2 passivation layer was deposited using PECVD, and source/gate interconnect windows were opened by buffered oxide etchant (BOE) etching. Finally, Ni/Au (50/300 nm) was deposited as the gate and source pad metal.

As shown in Figure A1(b), transfer length method (TLM) measurements show that the sheet resistance (R_{sh}) of the n^+ source region above the CBL is 2033 Ω/sq, with a contact resistance (ρ_c) of 2.02×10^{-5} $\Omega \cdot cm^2$ and a transfer length (L_T) of 1.0 μm. The relatively high sheet resistance is attributed to the unintended etching of approximately 80 nm of the Si-implanted $\beta - Ga_2O_3$ layer during HF removal of theSiO_2 implantation mask. Although HF does not etch pristine $\beta - Ga_2O_3$, room-temperature Si implantation damages the surface, making it susceptible to HF attack. Figure A1(c) presents the 1 MHz capacitance-voltage (C-V) measurements of MOS capacitors co-fabricated with the VDMOSFET. The extracted near-surface carrier concentration within 10 nm is approximately 2.5×10^{19} cm^{-3}, corresponding to an effective dopant activation rate of 50%, consistent with other reported values in the literature [1]. This result confirms that high-temperature N implantation does not significantly degrade the electrical properties of the n^+ source region.

To assess the current blocking capability of the CBL, test structures with varied N implantation conditions were fabricated. As shown in Figure A1(d), the CBL formed via 500 °C N implantation without post-annealing significantly outperforms the conventional CBL formed by room-temperature implantation followed by 1100 °C annealing. At an anode voltage of 20 V, the leakage current is suppressed by approximately three orders of magnitude.

To further evaluate the electrical behavior of the quasi-inversion channel formed by the high-temperature N implantation, a lateral long-channel MOSFET (L_{ch} = 100 μm) was fabricated alongside the VDMOSFET, as depicted in Figure A2(a). The channel carrier concentration (n_s), effective mobility (μ_{eff}), and sheet resistance (R_{sh}) as a function of gate voltage were extracted from differential C-V and output characteristics, as shown in Figure A2(b). At V_{GS} = 24 V, n_s reaches 8.8×10^{12} cm^{-2}, with μ_{eff} = 72.8 cm^2/Vs and R_{sh} = 9.8 kΩ/sq. The peak μ_{eff} of 74.6 cm^2/Vs occurs at V_{GS} = 20 V. These extracted values demonstrate that our channel mobility is superior to that of devices fabricated based on diffusion or implantation techniques [2,3], and approaching the performance of epitaxial channels [4,5].

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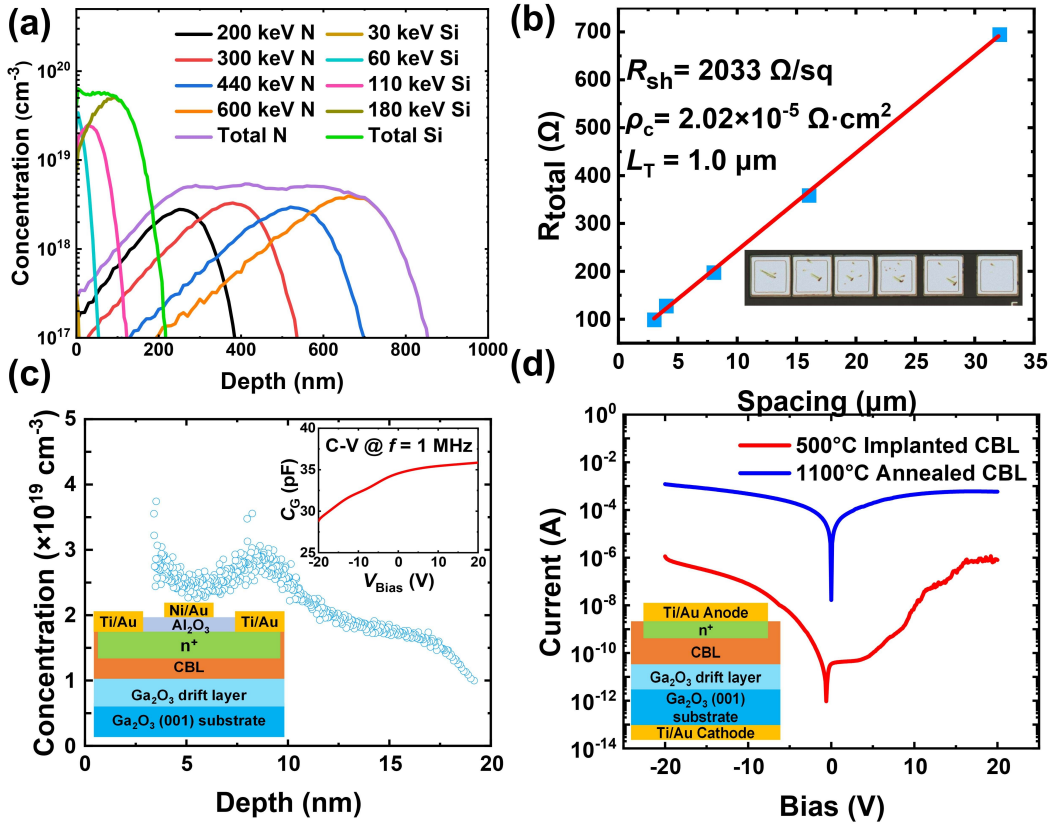

Figure A1 (a) Simulated depth profiles of implanted N and Si in $\beta - Ga_2O_3$, (b) TLM measurements of the n^+ source region above the CBL, (c) C-V characteristics of the MOS capacitor (inset) and the extracted carrier distribution, (d) comparison of the current-blocking capability for CBLs with different N implantation conditions.

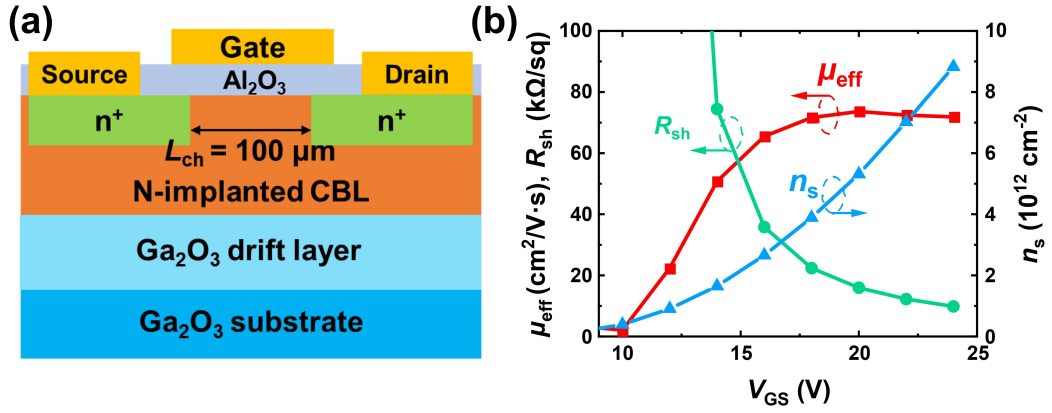

Figure A2 (a) Cross-sectional schematic of the lateral long-channel MOSFET fabricated alongside the VDMOSFET, (b) extracted channel carrier concentration (n_s), effective mobility (μ_{eff}), and sheet resistance (R_{sh}) as a function of gate voltage.

Appendix B Benchmark

The references for benchmark of $R_{on,sp}$ and BV for state-of-the-art CBL-based vertical $\beta-Ga_2O_3$ MOSFETs are detailed in Figure B1 [2, 6–11].

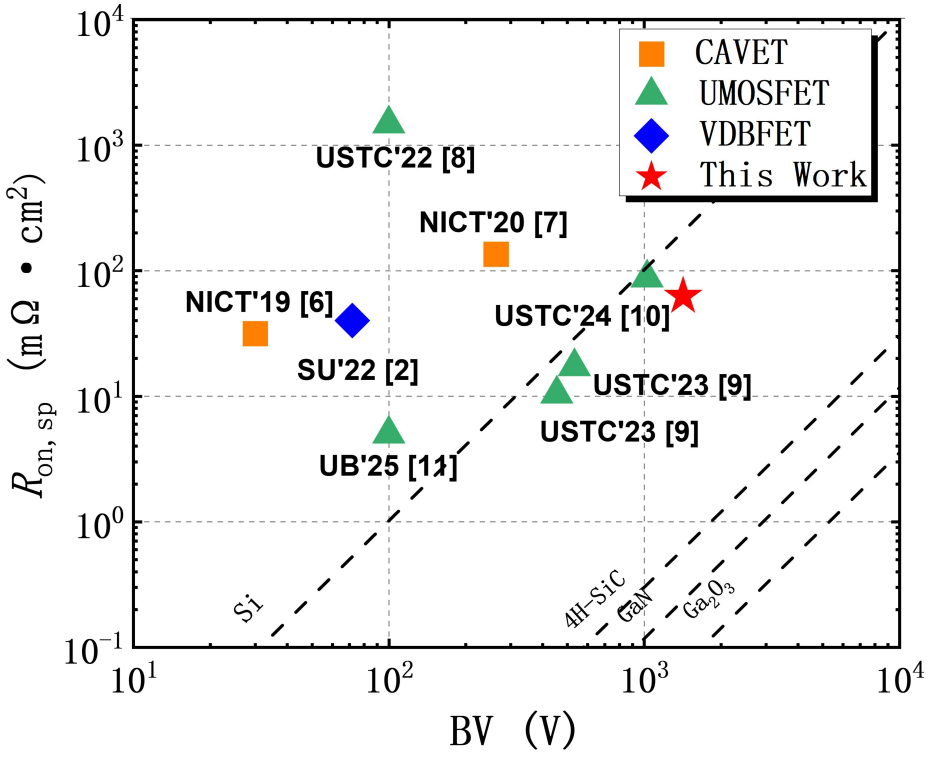

Figure B1 benchmarks the performance of the fabricated device against other state-of-the-art CBL-based vertical $\beta-Ga_2O_3$ MOSFETs.

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