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Special Topic: Advanced Optoelectronics Based on Two-Dimensional Materials

From wafer-scale growth to 3D integration: 2D WSe_2 pMOS for next-generation

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Abstract Two-dimensional (2D) p-type semiconductors are essential for realizing complementary logic and energy-efficient electronics beyond silicon technology. Among them, tungsten diselenide (WSe_2) has emerged as one of the most promising p-type metal-oxide-semiconductor (pMOS) channel materials due to its intrinsic p-type behavior, high carrier mobility, excellent electrostatic control, and compatibility with low-temperature processing. In recent years, significant progress has been made in the wafer-scale growth of high-quality 2D WSe_2, enabling systematic investigations of its electrical properties and large-area device integration. This review provides a comprehensive overview of the state-of-the-art advances in wafer-scale growth strategies of 2D WSe_2 pMOS, including chemical vapor deposition (CVD), van der Waals (vdW) epitaxy, and interface-engineered growth approaches. We further summarize key developments in contact engineering, band structure modulation, and transport optimization that underpin high-performance pMOS devices. Building on these foundations, recent efforts toward three-dimensional (3D) integration of WSe_2-based electronics are discussed, highlighting heterogeneous stacking, monolithic integration, and transfer-free integration schemes. Finally, we analyze the remaining challenges and outline future opportunities for integrating 2D WSe_2 pMOS into next-generation 3D integrated electronic systems.

Keywords WSe_2, p-type semiconductor, wafer-scale growth, pMOS devices, monolithic 3D integration

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1 Introduction

As the continuous miniaturization of silicon-based devices approaches fundamental physical limits, the information technology industry faces an epoch-defining challenge: the progressive slowdown of Moore's Law [1–3]. Since the advent of integrated circuits, advances in semiconductor technology have been driven primarily by aggressive dimensional scaling. However, as device dimensions enter the deep nanoscale regime, intrinsic physical constraints become increasingly dominant, including enhanced carrier scattering from thickness fluctuations, quantum tunneling, and exacerbated short-channel effects [4]. These factors collectively restrict further performance gains and energy efficiency improvements in conventional silicon technologies. In this context, two-dimensional (2D) semiconductor materials, characterized by their atomically thin nature and absence of surface dangling bonds, have emerged as a promising material platform to sustain device scaling and extend Moore's Law [5–7]. Their ultimate thickness limit enables superior electrostatic gate control, while their van der Waals (vdW) nature facilitates heterogeneous integration beyond the constraints of lattice matching [8–11]. Consequently, wafer-scale growth and integration of 2D semiconductors have become central research directions for next-generation electronics and advanced integrated circuit architectures [11].

Over the past decade, significant advances have been made in n-type 2D semiconductors, such as MoS_2 and InSe, particularly in wafer-scale synthesis [12–15], contact engineering [16, 17], and device performance optimization [18]. In several cases, key device metrics—including subthreshold swing, on/off ratio, and power consumption, have approached or even surpassed those of state-of-the-art silicon transistors [13, 19]. In contrast, the development of high-performance p-type 2D semiconductors has lagged considerably behind, resulting in a pronounced performance asymmetry between N-channel metal-oxide-semiconductor (NMOS) and P-channel metal-oxide-semiconductor (pMOS) devices. This imbalance represents a critical bottleneck for realizing fully functional and energy-efficient 2D complementary metal-oxide-semiconductor (CMOS) logic circuits [2, 9].

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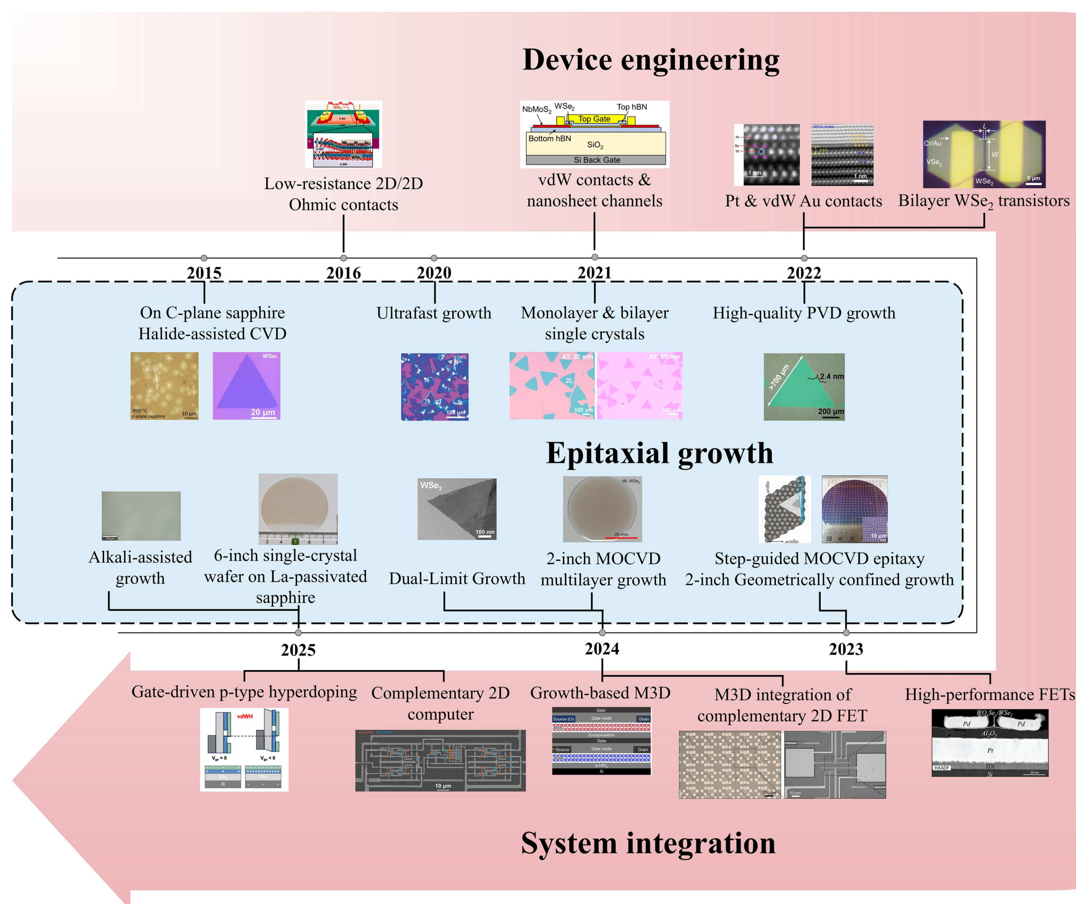

Figure 1 (Color online) Representative advances in the epitaxial growth, device engineering, and system integration of WSe_2. Epitaxial growth: on *c*-plane sapphire [25] Copyright 2015 American Chemical Society; halide-assisted CVD [26] Copyright 2015 Elsevier; ultrafast growth [27] Copyright 2020 Oxford University Press; monolayer/bilayer single crystals [28] Copyright 2021 American Chemical Society; high-quality PVD growth [29] Copyright 2022 John Wiley and Sons; step-guided MOCVD epitaxy [30] Copyright 2023 Springer Nature; 2-inch geometric confinement growth [31] Copyright 2023 Springer Nature; 2-inch MOCVD multilayer growth [32] Copyright 2024 Springer Nature; dual-limit large-area monolayer growth [33] Copyright 2024 American Chemical Society; 6-inch single-crystal wafer on La-passivated sapphire [15] Copyright 2025 The American Association for the Advancement of Science; large-scale alkali-assisted growth [34] Copyright 2025 Springer Nature. Device engineering: low-resistance 2D/2D ohmic contacts [35] Copyright 2016 American Chemical Society; vdW contacts [36] Copyright 2021 American Chemical Society; Pt on multilayer [37] Copyright 2022 Springer Nature; vdW Au contacts [38] Copyright 2022 Springer Nature; bilayer transistors [24] Copyright 2022 Springer Nature. System integration: three-pronged high-performance FETs [39] Copyright 2023 American Chemical Society; M3D integration of complementary 2D FET [32] Copyright 2024 Springer Nature; growth-based M3D integration [40] Copyright 2024 Springer Nature; complementary 2D material-based computer [41] Copyright 2025 Springer Nature; gate-driven hyperdoping [23] Copyright 2025 The American Association for the Advancement of Science.

Among the p-type 2D materials explored to date, black phosphorus exhibits intrinsically high hole mobility but suffers from severe environmental instability, limiting its practical utility [20]. $MoTe_2$ offers wafer-scale growth potential and phase-engineering opportunities; however, challenges related to phase purity, stability, and relatively modest carrier mobility remain unresolved [21, 22]. In contrast, WSe_2 has emerged as a particularly compelling pMOS channel material. Its energetically accessible valence band enables efficient hole transport, while its excellent air stability, compatibility with low-temperature processing, and scalability toward large-area fabrication render it well suited for integrated electronics [2]. Moreover, WSe_2 exhibits favorable band alignment and mobility matching with widely studied n-type MoS_2, facilitating balanced device characteristics at the circuit level. To date, the most advanced 2D pMOS devices have been demonstrated with WSe_2, achieving competitive electrical performance and operational stability. Recent advances in wafer-scale growth, contact and interface engineering, and band structure modulation have further accelerated the development of WSe_2-based pMOS transistors. These achievements establish a robust foundation for exploring 3D integration strategies, wherein vertically stacked and heterogeneous 2D devices offer new pathways toward high-density, energy-efficient, and multifunctional electronic systems [2, 23, 24].

Figure 1 illustrates the decade-long evolutionary trajectory (2015–2025) of WSe_2, highlighting representative advances in epitaxial growth, device-level engineering and system integration. In material synthesis, the paradigm has shifted from the preparation of microscopic flakes to the scalable growth of wafer-scale single crystals [23–41]. Key

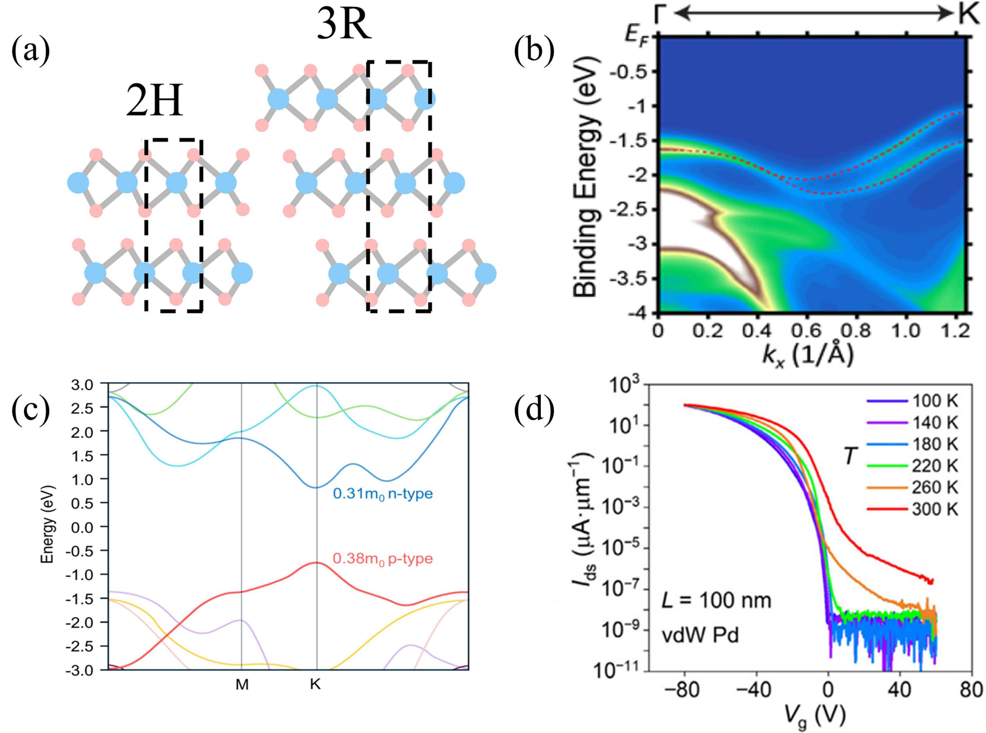

Figure 2 (Color online) Structure, energy-valley physics and optoelectronic properties of WSe_2. (a) Side view of the atomic structure of typical layered WSe_2 with 2H and 3R stacking configurations. (b) ARPES data of epitaxial single-layer WSe_2 thin films along the Γ-K direction. The red dotted curves depict the top VBs [44] Copyright 2016 American Chemical Society. (c) Energy band diagram of monolayer WSe_2 [2] Copyright 2025 Springer Nature. (d) Transfer characteristics of a WSe_2 FET with vdW Pd contacts measured under varying temperatures and gate voltages [47] Copyright 2024 Springer Nature.

methodologies, including halide-assisted chemical vapor deposition (CVD), metal-organic chemical vapor deposition (MOCVD), and geometrically confined epitaxy, have enabled the realization of high-quality single-crystal wafers ranging from 2-inch to 6-inch in scale. Concurrently, device engineering has progressed from fundamental contact optimization (e.g., low-resistance ohmic and vdW contacts) to the demonstration of high-performance p-type field-effect transistors (P-FETs). Recent milestones have further extended into system-level integration, encompassing complementary logic circuits, gate-driven hyperdoping, and monolithic three-dimensional (3D) integration. This roadmap underscores the transition of WSe_2 from fundamental exploration to a pivotal enabler for next-generation computing and post-Moore electronics.

2 Physical properties of WSe_2

The intrinsic physical properties of WSe_2 serve as the core foundation for its application as a high-performance pMOS channel material. Monolayer WSe_2 is a representative 2D transition metal dichalcogenide (TMD) with a bandgap of approximately 1.6 eV, rendering it highly attractive for electronic applications [42]. Owing to its layered vdW crystal structure, WSe_2 can adopt multiple stacking configurations, most notably the centrosymmetric 2H phase and the non-centrosymmetric 3R phase, as illustrated in Figure 2(a). The distinct interlayer translational symmetry associated with these stacking orders gives rise to markedly different interlayer coupling strengths, symmetry properties, and electronic responses, which in turn critically influence charge transport, interlayer exciton formation, and symmetry-dependent phenomena in vertical heterostructures [43]. Experimental mapping of the valence band structure (Figure 2(b)) unambiguously locates the valence band maximum (VBM) at the K point of the Brillouin zone [44]. In conjunction with theoretical calculations that place the conduction band minimum (CBM) also at the K point (Figure 2(c)), the direct-gap nature of monolayer WSe_2 is well established [2].

In terms of band alignment, WSe_2 possesses electronic energy levels that lie closer to the vacuum level than those of widely studied n-type 2D semiconductors such as MoS_2, with its valence band maximum intrinsically located at a relatively high energy. According to the Schottky-Mott rule, this high-lying valence band should theoretically reduce the Schottky barrier height for hole injection when interfaced with high-work-function metals [9,45,46]. In practical devices fabricated via conventional metal deposition, however, this intrinsic advantage is often obscured by Fermi-

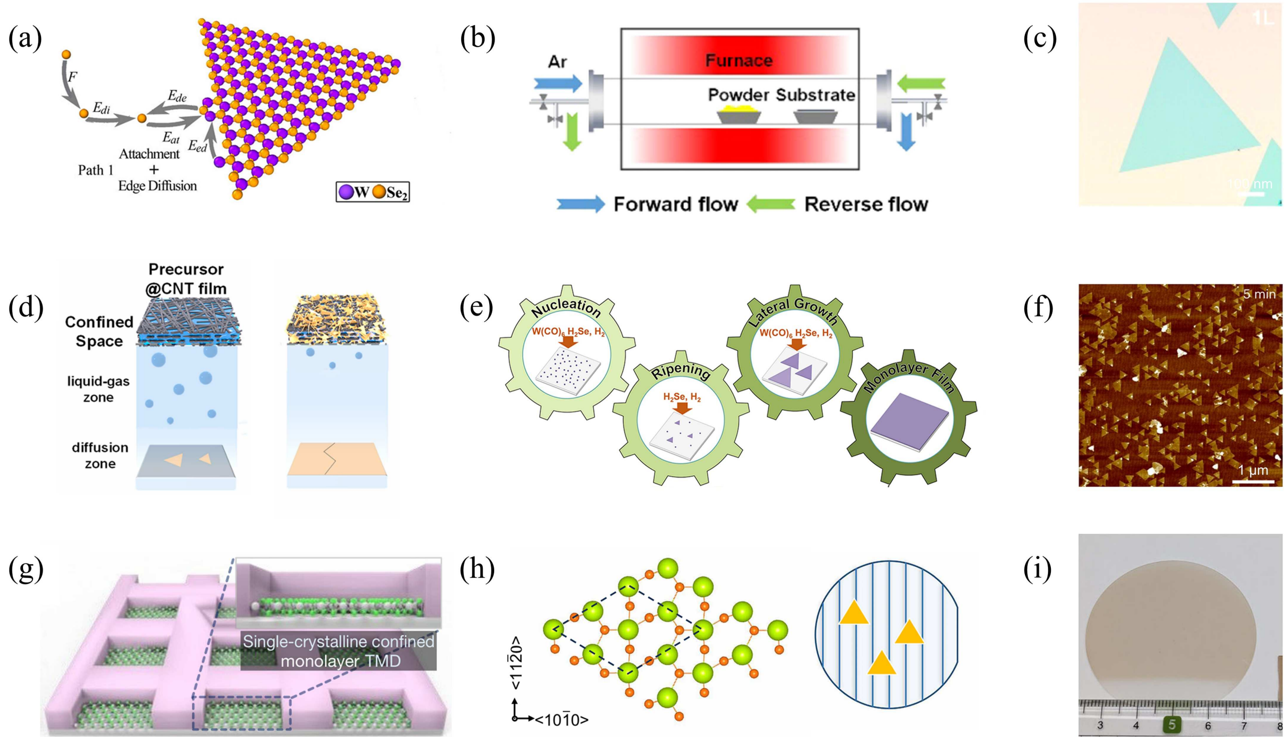

Figure 3 (Color online) Controlled growth and mechanism study of WSe_2 via CVD. (a) Proposed growth mechanism of triangular WSe_2 domains, involving fast attachment and ultrafast edge diffusion [50] Copyright 2019 Springer Nature; (b) bidirectional gas-flow CVD system employed for WSe_2 growth [28] Copyright 2021 American Chemical Society; (c) optical microscopy (OM) image of monolayer WSe_2 synthesized using the method in Figure 3(b); (d) synthesis of TMDs via the dual-limit growth (DLG) strategy [33] Copyright 2024 American Chemical Society; (e) schematic of the multistep diffusion process for epitaxial WSe_2 growth [55] Copyright 2018 American Chemical Society; (f) coalescence of unidirectional WSe_2 domains [30] Copyright 2023 Springer Nature; (g) schematic mechanism for the formation of selective single-domain TMD arrays [31] Copyright 2023 Springer Nature; (h) schematic of a lanthanum passivated $Al_2O_3(0001)$ substrate [15] Copyright 2025 The American Association for the Advancement of Science; (i) optical image of 150 mm WSe_2 wafers synthesized using the method in (h).

level pinning (FLP). FLP is fundamentally an interface phenomenon driven by metal-induced gap states (MIGS) and defect-induced disorder, and cannot be overcome solely by the favorable band alignment of the semiconductor [47]. To realize low-barrier contacts, interfacial disorder must be independently suppressed through advanced interface engineering strategies, such as the adoption of vdW contacts or tunneling buffer layers. Only when these pinning effects are effectively decoupled from the semiconductor surface can the favorable band alignment of WSe_2 be fully harnessed. Together with its reduced hole effective mass and suppressed intervalley scattering, this enables efficient hole accumulation and transport at the device level (Figure 2(d)) [47].

These intrinsic advantages position WSe_2 as a highly promising pMOS channel. Moreover, its p-type characteristics align well with the band structure and carrier mobility of established NMOS materials such as MoS_2, enabling balanced complementary performance in circuits. Consequently, precise control over crystal phase, stacking order, and wafer-scale growth quality is essential for achieving uniform and reproducible device performance.

3 Controlled growth of WSe_2 from microscale to wafer-scale

In the field of 2D semiconductors, the synthesis and integration of n-type materials such as MoS_2 have reached a relatively mature stage. In contrast, the fabrication of p-type materials like WSe_2, which are essential for high-performance complementary electronics, remains significantly more challenging due to precursor limitations and stringent requirements for crystallinity, thickness uniformity, and domain orientation. Primary synthesis routes include chemical vapor deposition (CVD), physical vapor deposition (PVD), and molecular beam epitaxy (MBE), each offering distinct trade-offs between scalability and crystal quality. Among these, CVD has emerged as the most promising method for large-area epitaxial growth of WSe_2, owing to its process flexibility, scalability, and compatibility with standard semiconductor manufacturing [48, 49]. Early studies proposed rapid CVD growth pathways (Figure 3(a)), and continued optimization has established CVD as a reliable route for synthesizing high-quality monolayers [7, 50].

At the microscale, conventional CVD growth faces two fundamental limitations: the low saturated vapor pressure of selenium restricts vapor-phase transport and surface reactivity, while the high melting point of common tungsten precursors such as WO_3 ($\sim$1473°C) hinders the generation of a stable flux of reactive species. These factors lead to uncontrolled nucleation, low domain density, and poor spatial uniformity, rendering single-crystal growth challenging. To address these issues, counter-current CVD systems have been developed to stabilize the gas-phase composition, enabling controlled growth of monolayer and bilayer single crystals (Figures 3(b) and (c)). This approach mitigates volatility-induced instabilities inherent to traditional CVD and provides a robust foundation for microscale single-crystal synthesis [28, 51–53].

Scaling from microscale flakes to larger domains demands both chemical and kinetic control. The introduction of alkali metal halides such as NaCl or KCl as growth promoters lowers the effective growth temperature to approximately 700°C through the formation of volatile tungsten oxohalide species (e.g., WO_2Cl_2 and $WOCl_4$) [26, 34, 54]. This facilitates efficient precursor delivery and enables the synthesis of high-crystallinity, chemically pure monolayers suitable for high-performance field-effect transistors (FETs), achieving hole mobilities of $\sim$100 $cm^2 \cdot V^{-1} \cdot s^{-1}$. For uniform large-area monolayer growth, DLG strategies employ face-to-face stacking of precursor-loaded porous carbon nanotube films on sapphire substrates (Figure 3(d)). In this configuration, spatial confinement stabilizes and uniformly distributes the vapor, suppressing random nucleation and promoting lateral monolayer growth. Concurrently, temporal confinement arises from the accumulation of reaction byproducts, which automatically terminates precursor supply and prevents undesirable secondary vertical growth on existing layers [33].

Achieving wafer-scale single-crystal films further requires precise orientation control [55]. High-density grain boundaries in polycrystalline films can severely degrade electrical properties, rendering domain alignment critical (Figure 3(e)). MOCVD techniques have enabled reversible switching between 0° and 60° domain orientations through adjustment of growth pressure [30], yielding merged monolayers with inversion domain boundary densities below 15% on 50 mm sapphire substrates (Figure 3(f)). Geometric confinement using patterned micrometer-scale trenches restricts the nucleation region and promotes layer-by-layer growth within the trenches (Figure 3(g)). By carefully controlling the growth duration, individual nucleation clusters expand and merge into single-domain structures, suppressing secondary nucleation and enabling uniform monolayer or bilayer films. The resulting films exhibit mobilities of 72.8 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for monolayer WSe_2 and 103.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ for bilayer WSe_2, approaching the performance of mechanically exfoliated flakes [31].

Meanwhile, the periodic surface potential of the substrate has proven highly effective in guiding unidirectional epitaxial growth of these center-symmetric 2D materials. Atomically sawtoothed gold surfaces, for instance, serve as universal growth templates, wherein the periodic stepped edges provide ideal sites for anisotropic adsorption of TMD clusters and thereby induce unidirectional epitaxy [56, 57]. In contrast, conventional *c*-plane sapphire [$Al_2O_3(0001)$] substrates exhibit surface center symmetry (P3 symmetry), which leads to antiparallel domain alignment and grain boundary formation, limiting large-area uniformity. Spin-coating with lanthanum sulfate solution followed by air annealing forms a single-layer lanthanum passivation layer (La-Al_2O_3) on the sapphire surface. Lanthanum atoms substitute for aluminum sites, reducing the surface symmetry from P3 to P1 (Figure 3(h)). This symmetry breaking lifts the degeneracy of antiparallel domains and increases the TMD binding energy difference to 149 $meV \cdot nm^{-2}$. This represents a 26-fold enhancement over the pristine substrate and ensures unidirectional epitaxy. Using this approach, 150-micrometer TMD domains have been successfully grown (Figure 3(i)), with WSe_2 exhibiting an average room-temperature mobility of 131 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [15].

Table 1 summarizes the intrinsic performance of WSe_2 synthesized via various techniques, including geometric confinement growth, salt-assisted CVD, counter-flow PVD, MOCVD, and MBE [15, 28, 30, 31, 34, 52–54, 57, 58]. Key parameters such as growth temperature, substrate, number of layers, orientation, size, polarity, contact metal, carrier mobility, on/off ratio, on-state current, threshold voltage, and subthreshold swing are compiled. It is important to emphasize that the mobility and current values presented herein reflect the as-grown material quality without contact resistance optimization or advanced doping strategies, thereby establishing a critical baseline for decoupling advances in material synthesis from subsequent device engineering improvements. As evident from the table, wafer-scale single-crystal WSe_2 films up to 6 inches have been achieved, with monolayer mobility reaching 131 $cm^2 \cdot V^{-1} \cdot s^{-1}$, a value that already satisfies the mobility targets ($\sim$100 $cm^2 \cdot V^{-1} \cdot s^{-1}$) for semiconductor devices outlined in the International Roadmap for Devices and Systems (IRDS) 2028 edition [59, 60].

Although CVD has enabled the preparation of 6-inch wafer-scale single-crystalline WSe_2 films, its industrial application still faces three major challenges. First, mainstream CVD growth temperatures are concentrated in the range of 800°C–1100°C, far exceeding the 400°C thermal budget limit of the back-end-of-line (BEOL) process in silicon CMOS technology. This necessitates transfer-based integration, which introduces issues such as interfacial contamination and alignment errors. Although a few reports have demonstrated growth at lower temperatures (385°C–600°C), this comes with a pronounced degradation in carrier mobility (e.g., 45 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 450°C) and

Table 1 Summary of intrinsic material performance for WSe_2 grown by various methods.

Growth method	Growth temperature (°C)	Substrate	Numbers of layers	Orientation	Size	Contact metal	Polarity	Carrier mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	On/of ratio	I_{on} (L_{ch}, V_{ds})	V_{th}	SS
Geometric confinement [31]	890°C	c-Al_2O_3 or a-HfO_2/Si	1L&2L	Non	Flakes: 2 μm-wide stripe array	Pt/Au	P-type	1L: 72.8 2L: 103.5	$>10^8$	2L: 155.8 $\mu A \cdot \mu m^{-1}$ (0.7 μm, 1 V)	1L: ∼10 V	240.5 $mV \cdot dec^{-1}$
NaCl assisted CVD growth [54]	920°C	SiO_2/Si	2L–4L and more	Non	Flakes: 120 μm	Ni/Au	2L: P-type 3L: ambipolar 4L: N-type	4L: 2.239	$\sim 10^4$	N/A	2L: ∼−50 V	N/A
MOCVD with substrate surface engineering [30]	1000°C	c-Al_2O_3	1L	>87%	Film: 2 inch	Pt/Au	P-type	0.4	$\sim 10^5$	900 $nA \cdot \mu m^{-1}$ (200 nm, 1 V)	∼ 1 V	980 $mV \cdot dec^{-1}$
MOCVD on La-passivated substrate [15]	950°C	La-passivated c-Al_2O_3	1L	>95.6%	Film: 6 inch	N/A	P-type	131	$>10^7$	N/A	∼−50 V	N/A
Alkali-assisted CVD growth [34]	975°C	c-Al_2O_3	1L&2L	Non	1L: 2 inch 2L: cm-scale	Pt or Ag (Se buffer)	Pt: P-type Ag: N-type	2L: P-type 119 N-type 34	N/A	N/A	∼−22 V	N/A
Au-substrate CVD growth [57]	950°C	Au	1L	Non	Flakes: >800 μm	Au	P-type	139	$\sim 10^6$	N/A	∼−60 V	2.9 $V \cdot dec^{-1}$
Single-source CVD growth [28, 52, 53]	830°C–1150°C	SiO_2/Si	2L–4L	Non	Flakes: 600–800 μm	Pt or Cr	P-type	1L: 92 2L: 145	$>10^7$	N/A	N/A	N/A
MBE-2H/1T′-phase [58]	450°C–600°C	$SrTiO_3$	1L	Non	Nano-to-submicron scale	N/A	N/A	N/A	N/A	N/A	N/A	N/A

Table 2 Summary of polarity control strategies in WSe_2 FETs.

Reference/strategy	Material sources	Contact metal (work function)	Contact integration method	Gate dielectric structure	Observed polarity type
Dual-gated transistor [65]	Mechanical exfoliation	Pt (high)	Transferred back-contacts (pre-patterned)	Top-gate: hBN Back-gate: SiO_2/Si	p-type
Work function induced polarity conversion [66]	Self-Flux method (bulk crystal)	In (low) Cr (medium) Au (high) Pd (high)	Conventional thermal evaporation	SiO_2/Si	In, Cr: n-type Au, Pd: p-type
Contact engineering + Plasma doping [64]	Mechanical exfoliation	In, Cr	Conventional thermal evaporation	SiO_2/Si	In: n-type; Cr: Ambipolar Cr + O_2 plasma: p-type
vdW contacts [47]	CVD-1L	Pd (high)	vdW transfer (pre-fabricated pads)	SiO_2/Si	p-type (high-performance unipolar)
Pt/Sb thickness tuning [67]	CVD-1L	Pt/Sb (tunable Sb thickness)	Conventional thermal evaporation	SiN_x/Si	10 nm Sb: p-type dominant 30 nm Sb: n-type dominant
Au integration comparison [63]	Mechanical exfoliation (multilayer)	Au (high)	vdW transfer vs. conventional thermal evaporation	SiO_2/Si	vdW transfer: p-type Thermal evaporation: n-type
Edge contacts for robust p-type [70]	CVD	Ti, Ni, Pd	Edge contact (Ar^+ ion etching then metal evaporation)	SiO_2/Si	p-type dominant (metal-independent)
Spontaneous oxidation intercalation [69]	Mechanical exfoliation	Au	Ar plasma etching, oxidation, annealing	SiO_2/Si	Pristine: ambipolar Treated: p-type
Theoretical calculation of contacts [68]	Theoretical experimental summary	Au	N/A	N/A	Defect-free: p-type; with Se vacancies: n-type (theoretical prediction)

the formation of undesired secondary phases [58, 61]. Second, CVD-grown WSe_2 films do not exhibit intrinsically p-type polarity; their conduction type is dictated by the interplay of contact metal work function, interface damage, and selenium (Se) vacancy defects [62–64]. Third, mainstream approaches such as halide-assisted CVD suffer from alkali metal residues, which introduce additional doping and scattering centers, thereby degrading the long-term stability of the devices [26].

In summary, although critical challenges persist, the progress achieved to date delineates a clear trajectory from microscale single-crystal flakes to centimeter-scale aligned domains and ultimately toward wafer-scale monolayers with controlled orientation. By synergistically integrating strategies in chemistry, kinetics, and substrate design, high-quality WSe_2 films that fully harness the intrinsic pMOS advantages of the material can now be reproducibly synthesized. This foundation paves the way for the subsequent in-depth discussion of contact engineering, device optimization, and 3D integration of WSe_2-based electronics.

4 Device engineering of WSe_2 for pMOS applications

With the controlled growth of WSe_2, from microscale single crystals to wafer-scale monolayers and orientation-controlled epitaxy, high-quality WSe_2 films are now readily available for functional device integration. However, the material foundation built on large-area uniformity and precise layer control does not by itself guarantee robust p-type transport. CVD-grown WSe_2 frequently exhibits ambipolar behavior. In fact, the carrier polarity in WSe_2 transistors is not an intrinsic material property, but emerges from the interplay of three factors: the quality of the metal-semiconductor interface, the work function of the contact metal, and the defect chemistry of the channel material (Table 2).

In the ideal scenario of a defect-free WSe_2 crystal with a pristine, undisturbed interface, the transistor polarity should follow the Schottky-Mott rule, determined solely by the alignment between the metal work function and the band edges of WSe_2 [65]. High-work-function metals such as Pt, Pd, and Au have Fermi levels close to the valence band edge, favoring hole injection and p-type transport; low-work-function metals such as In and Ag have Fermi levels near the conduction band edge, favoring electron injection and n-type transport. This trend has been directly observed by Thi et al., who systematically compared metals with different work functions on WSe_2 grown by the self-flux method. In contacts yielded n-type devices, while Pd and Au contacts produced p-type behavior [66].

In practice, however, devices frequently deviate from this ideal picture. The key factor is how the metal contacts are integrated onto WSe_2 and the resulting interface quality. When prefabricated metal electrodes are physically laminated onto the WSe_2 surface via vdW transfer, the interface is nearly free of chemical bonding and lattice damage. Fermi-level pinning is effectively suppressed, and the advantage of the metal work function can be fully exploited. Li et al. demonstrated this by transferring Pd electrodes onto CVD-grown monolayer WSe_2, achieving

an on-state current exceeding 100 μA·μm^{-1}, a contact resistance as low as 12 kΩ · μm, and stable pure p-type operation [47]. In stark contrast, conventional thermal evaporation bombards the WSe_2 surface with high-energy metal atoms, disrupting the lattice and introducing abundant interfacial defects and dipoles, leading to strong Fermi-level pinning. Under such conditions, even a high-work-function metal such as Au may have its Fermi level pinned near the conduction band, resulting in n-type or ambipolar behavior. Kong et al. clearly demonstrated this contrast: on the same WSe_2 flake, vdW-integrated Au contacts gave p-type devices, whereas thermally evaporated Au contacts produced n-type devices [63]. Recently, Lin et al. demonstrated that even with thermal evaporation, Fermi-level pinning can be mitigated by using an antimony-platinum (Sb-Pt) bilayer contact, owing to the low melting point of Sb (630°C), which reduces damage to the lattice of the material surface. By increasing the Sb interlayer thickness from 10 to 30 nm, the effective work function at the evaporated contact interface is tuned from 4.42 eV (p-type) to 4.19 eV (n-type), enabling selective n- or p-type polarity in monolayer WSe_2 FETs. This work shows that polarity control is not exclusive to van der Waals transfer; a well-designed bilayer stack can also overcome pinning and achieve both polarities on the same channel material [67].

Defect chemistry plays an equally indispensable role. GW calculations by Noori et al. identified selenium vacancies as the most common intrinsic defect in WSe_2, introducing gap states near the conduction band minimum that effectively pin the Fermi level and drive n-type transport [68]. Selenium vacancies, however, have a crucial characteristic—they are highly susceptible to passivation by oxygen atoms in air or oxygen environments. This passivation can occur naturally or be accelerated through oxygen plasma treatment. Once the vacancies are passivated, the n-type pinning states are removed and the interface recovers its intrinsic properties; the oxidation process itself may also introduce additional p-type doping, further enhancing hole conduction. Tang et al. applied oxygen plasma treatment to Cr-contacted WSe_2 devices and successfully converted them from ambipolar to purely p-type, with an on/off ratio reaching 10^6 [64]. Similarly, Huang et al. proposed a p-type WSe_2 transistor contact modulation technique based on spontaneous oxidation intercalation (SOI), which forms a WO_x buffer layer between the metal/Au and WSe_2 through Ar plasma etching, spontaneous oxidation, and annealing (300°C–400°C), achieving a transition from n-type or ambipolar to purely p-type transport [69]. Abuzaid et al. further reported that edge-contact geometries themselves favor p-type-dominated transport in WSe_2, an effect largely independent of the choice of contact metal [70].

Taken together, the polarity of WSe_2 transistors is not a fixed attribute but a dynamic outcome of the combined influence of metal work function, interfacial defect states, and the ambient environment.

To achieve robust p-type transport in CVD-grown WSe_2, the key is to translate these mechanistic insights into a coordinated device engineering strategy. First, defect chemistry should be controlled at the growth stage: by tuning the Se/W precursor ratio and the temperature window to produce Se-rich or stoichiometric WSe_2, the density of selenium vacancies can be minimized from the outset [68]. Second, a pinning-free vdW contact should be formed by physically transferring, rather than thermally evaporating, a high-work-function metal such as Pd or Pt onto the WSe_2 surface, which is currently the most effective route to high-performance p-type devices, as experimentally validated by Li et al. [47] and Kong et al. [63]. On this basis, residual selenium vacancies can be passivated and moderate p-type doping introduced through brief, low-power oxygen plasma treatment [64], while the channel can be encapsulated with a flat, dangling-bond-free gate dielectric such as hBN to screen environmental perturbations and unlock the intrinsic electrical performance of the material [47, 65]. These three elements—defect-controlled growth, a damage-free vdW contact, and adjunct doping plus dielectric passivation, constitute a complete framework for realizing robust p-type operation in CVD WSe_2.

Consequently, despite the intrinsic advantages of WSe_2, including its favorable band structure and atomic-scale thickness, unipolar p-type 2D transistors still face significant limitations such as low saturation current density and high contact resistance. These issues originate primarily from the Schottky barrier at the metal-semiconductor interface, which arises from work function mismatch and Fermi-level pinning. Overcoming these challenges is essential for realizing high-performance p-channel 2D devices and building balanced complementary logic circuits.

Optimizing the metal-semiconductor interface is a prerequisite for suppressing the Schottky barrier height and maximizing carrier injection efficiency in 2D electronic devices. In conventional metallization processes, the high kinetic energy of deposited atoms readily introduces interfacial defects and causes Fermi-level pinning. By contrast, vdW contacts employing high-work-function metals offer an effective pathway to forming damage-free, atomically pristine interfaces [71]. Using this approach, metals such as platinum (Pt) and palladium (Pd) have been shown to establish well-defined, non-invasive contacts on the WSe_2 lattice (Figure 4(a)), with Pt-contacted devices exhibiting excellent p-type transport and a contact resistance (R_c) as low as ∼3.3 kΩ · μm [37]. Similarly, an intrinsic metal-semiconductor interface can be obtained by laminating Pd electrodes onto WSe_2 via a transfer electrode method (Figure 4(b)) [47]. These studies, driven by the strategy of "avoiding or minimizing bombardment", represent a fundamental advance in interface integrity over conventional deposition. However, while Pt contacts fabricated by

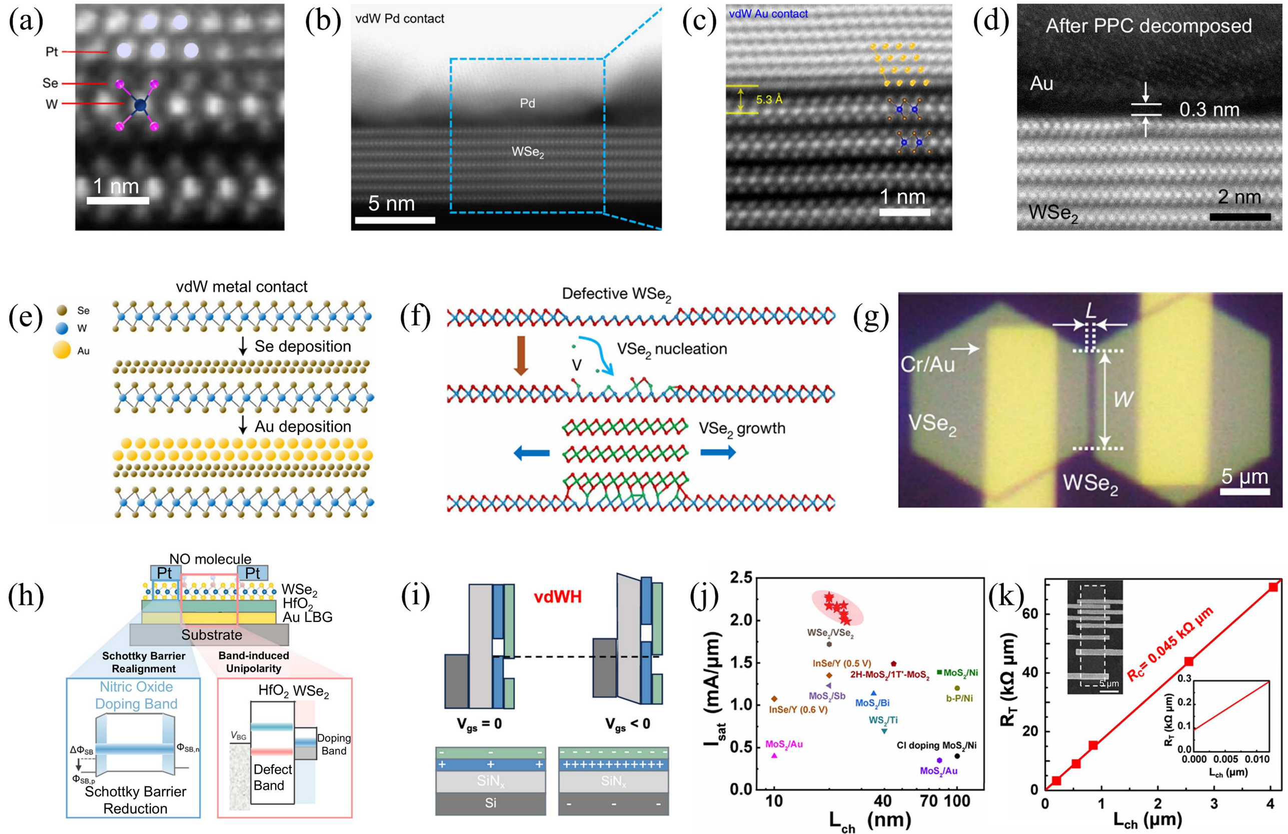

Figure 4 (Color online) Performance enhancement of WSe_2 field-effect transistors. (a) Atomic resolution images of Pt on multilayer WSe_2 [37] Copyright 2022 Springer Nature; (b) HAADF-STEM image of a transferred Pd/WSe_2 vdW interface [47] Copyright 2024 Springer Nature; (c) HAADF-STEM cross-sectional image of WSe_2 with a vdW Au contact [38] Copyright 2022 Springer Nature; (d) atomically sharp vdW interface between Au and WSe_2, achieved via a decomposed polymer buffer layer [72] Copyright 2023 Springer Nature; (e) schematic of the sample cross-sections during fabrication of vdW and direct Au contacts on WSe_2 [38] Copyright 2022 Springer Nature; (f) illustration of VSe_2 nucleation and growth on W-terminated surfaces at patterned sites [73] Copyright 2020 Springer Nature; (g) optical microscopy images of ultrashort-channel WSe_2 transistors with VSe_2 contacts [24] Copyright 2022 Springer Nature; (h) schematic of a 2D FET featuring a monolayer WSe_2 channel, Pt metal contacts, and a local bottom gate after nitric oxide doping [75] Copyright 2025 Springer Nature; (i) band diagram of the 1L-SnS_2/2L-WSe_2 Hall device, showing increased band offset and enhanced charge transfer doping at $V_{gs} < 0$ [23] Copyright 2025 The American Association for the Advancement of Science; (j) comparison of saturation current (I_{sat}) of 1L-SnS_2/2L-WSe_2 FETs with other 2D transistors as a function of channel length [23]; (k) transmission line method (TLM) determination of contact resistance (R_c) in 1L-SnS_2/2L-WSe_2 vdW heterostructure FETs [23].

intermittent evaporation perform reasonably well on multilayer WSe_2, their R_c degrades dramatically on monolayer WSe_2 to as high as 229 $\mathrm{k\Omega \cdot \mu m}$ [37]; moreover, the wafer-scale uniformity and repeatability of transfer-based methods, along with the associated risks of stress and particulate contamination, still limit their transition from the laboratory to a manufacturing environment.

To realize such ideal interfaces in a more operationally viable manner, buffer-layer-assisted integration strategies have been successively proposed. A decomposed polymer buffer layer can effectively shield against direct metal bombardment, yielding a clean Au/WSe_2 interface with a well-defined vdW gap of ∼0.3 nm (Figure 4(d)) [72]. In a related scheme, a ∼10 nm thick selenium (Se) protective layer is pre-deposited before Au evaporation and subsequently removed by thermal annealing at 150°C, leaving the metal electrode in pristine vdW contact with the channel (Figures 4(c) and (e)) [38]. Compared with direct vdW transfer, buffer-layer methods improve process controllability while preserving interface quality, yet they inevitably add extra removal steps; residues from polymer decomposition or residual Se atoms may act as doping/scattering centers, posing potential threats to long-term reliability and thermal stability, and a gap remains with respect to the stringent cleanliness and process integration requirements of silicon CMOS production lines.

Moving beyond physical deposition, epitaxial engineering provides an alternative seamless contact scheme. By selectively nucleating metallic VSe_2 on W-terminated defect sites, contact electrodes can be epitaxially grown directly from the WSe_2 channel crystal (Figure 4(f)) [73]. This method eliminates interfacial contamination via chemical bonding and enables the fabrication of ultra-short-channel, high-performance transistors in which the channel length is defined by the growth gap (Figure 4(g)) [24]. Compared with transfer or buffer-layer ap-

proaches, this "seamless epitaxy" offers significant advantages in scaling contact length and lowering R_c (down to $\sim$0.25 k$\Omega \cdot \mu$m). However, the trade-offs are also pronounced: the epitaxial process generally requires a thermal budget of $\sim$600°C, far exceeding the sub-400°C limit typical for silicon CMOS back-end-of-line (BEOL) integration; the nucleation density, crack control, and phase purity of VSe_2 are highly sensitive to the growth window, resulting in a narrow process window, and the uniformity and wafer-level yield over large-area arrays have yet to be verified, thus posing substantial challenges for manufacturing scalability.

Complementary to contact engineering, doping strategies are indispensable for precise threshold voltage tuning and performance enhancement [74]. Surface charge-transfer doping using nitric oxide (NO) or nitrogen dioxide (NO_2) has proven effective in passivating Se vacancies and inducing pronounced p-type characteristics [75, 76]. As illustrated in Figure 4(h), NO molecules introduce donor states within the bandgap, shifting the Fermi level substantially toward the valence band, thereby tripling the channel mobility, improving the subthreshold swing to 70 mV$\cdot$dec^{-1}, and maintaining an on/off current ratio exceeding 10^9 together with an on-current as high as 448 μA$\cdot\mu$m^{-1} [76]. Gas-phase molecular doping achieves a dramatic performance boost through an exceedingly simple process, especially suitable for proof-of-concept demonstrations. Nevertheless, its intrinsic drawbacks are equally clear: first, dopant molecules gradually desorb even at room temperature, resulting in insufficient long-term operational stability [75]; second, NO_2 is strongly corrosive, raising fundamental compatibility concerns with silicon CMOS cleanroom protocols; in terms of thermal stability, the molecular doping layer may degrade upon moderate-temperature annealing, making it incapable of withstanding thermal budgets in back-end integration. These factors collectively limit the translational potential of molecular doping in industrial-grade manufacturing.

In contrast to unstable chemical doping, band-structure engineering realized through vdW heterostructures offers a more robust pathway for performance modulation [23]. Constructing a 1L-SnS_2/2L-WSe_2 heterojunction yields a type-III band alignment, triggering spontaneous electron transfer from the WSe_2 valence band to the SnS_2 conduction band (Figure 4(i)) and positively shifting the threshold voltage to approximately +10 V. Under negative gate bias, this interlayer charge transfer induces a "super-doping" effect that raises the 2D hole density to 1.49×10^{14} cm^{-2}, far exceeding the limits of conventional electrostatic gating [23]; consequently, the saturation current scales linearly with channel length (Figure 4(j)). Transmission line method analysis confirms that this heterojunction can achieve an ultralow R_c of $\sim$0.041 k$\Omega \cdot \mu$m and a maximum on-state current density of 2.30 mA μm^{-1} (Figure 4(k)), far surpassing the IRDS 2028 targets for advanced-node silicon FETs. However, this leap in performance comes at the expense of process simplicity: the fabrication of SnS_2/WSe_2 heterostructures relies on precise epitaxial stacking or demanding layer-transfer processes, requiring extremely tight control over layer thickness, interfacial cleanliness, and crystallographic alignment, with a structural complexity well beyond that of pure metal contacts; the epitaxial construction temperature of $\sim$600°C is not only incompatible with the BEOL thermal budget but also raises unresolved concerns regarding interlayer diffusion and high-temperature stability. Hence, although this approach represents the performance pinnacle for p-type WSe_2 devices, its evaluation in terms of manufacturing scalability and process compatibility is still at an early stage.

Table 3 systematically summarizes the electrical performance and limitations of representative contact strategies and benchmarks them against the IRDS 2028 targets. It can be seen that heterojunction super-doping leads in performance with an ultralow R_c and extremely high on-state current, yet is constrained by high-temperature processing, high structural complexity, and low silicon compatibility; buffer-layer-assisted vdW contacts (PPC-based $\sim$5.3 k$\Omega \cdot \mu$m, Se-buffer-based $\sim$1.25 k$\Omega \cdot \mu$m) strike a compromise between interface quality and process feasibility, but face risks of residual contamination and additional stress [38, 72]; the band-hybridized Se contact (0.54 k$\Omega \cdot \mu$m) demands precise Se thickness control ($\sim$1 nm) and likewise raises concerns regarding process complexity and thermal stability [77]; whereas conventional Pt contacts perform adequately on multilayer WSe_2 (3.3 k$\Omega \cdot \mu$m) but degrade catastrophically on monolayer WSe_2 to 229 k$\Omega \cdot \mu$m [37].

In summary, simultaneously achieving a low contact resistance on the order of $\sim$0.1 k$\Omega \cdot \mu$m, high stability, and strong compatibility with silicon CMOS technology remains a formidable core challenge on the path toward practical application of WSe_2 contact engineering, requiring concerted progress across materials, interfaces, and process integration.

5 Integration of WSe_2 and 2D CMOS circuits

As the semiconductor industry navigates the "More Moore" era, silicon-based devices are rapidly approaching their fundamental physical limits. Within this landscape, 2D semiconductors (such as MoS_2 and WSe_2) have emerged as leading candidates for next-generation integrated circuits (ICs) owing to their atomic-scale thickness and exceptional carrier transport properties. Translating these intrinsic advantages into practical technologies, however, requires

Table 3 Summary of contact strategies and performance metrics for WSe_2 p-type transistors.

Method	Layers	Contact metal	R_c (kΩ · μm)	I_{on} (L_{ch}, V_{ds})	On/off ratio	V_{th}	Limitations	Si compatibility
Band-hybridized selenium contact [77]	3L	Au/Se	∼0.54	∼0.43 mA·μm^{-1} (80 nm, 1 V)	10^8	∼−2.5 V	Precise deposition and removal of Se buffer required	Moderate
vdW metal contact (Se buffer) [38]	ML (∼12 nm)	Au	∼1.25	∼0.06 mA·μm^{-1} (1.6 μm, 1 V)	10^6	∼−30 V	Se layer thickness (∼1 nm) requires high uniformity; thermal stability of Se/metal interface needs verification	Moderate
vdW metal contact (PPC buffer) [72]	Multi (∼12 nm)	Pd	∼5.3	∼0.5 μA·μm^{-1} (50 μm, 1 V)	10^6–10^7	∼−27 V	PPC decomposition may leave residues or stress longer process flow	Moderate
Metal (Pt) intermittent evaporation [37]	Multi/1L	Pt	Multi: ∼3.3 1L: ∼229	Multi: ∼25 μA·μm^{-1} (4 μm, 1 V) 1L: ∼7.6 μA·μm^{-1} (1.5 μm, 1 V)	10^7	∼−15 V	High contact resistance for Pt on monolayer WSe_2	High
vdW contacts (2D metal VSe_2) [24]	2L	VSe_2	∼0.25	∼1.72 mA·μm^{-1} (20 nm, 1.2 V)	10^2–10^6	∼−35 V	Rely on complex epitaxial growth and crack control of specific vdW materials	Low
SnS_2/WSe_2 heterojunction hyperdoping [23]	2L	Au/SnS_2	∼0.041	∼2.30 mA·μm^{-1} (20 nm, 0.88 V)	10^8–10^9	∼10 V	Depend on specific SnS_2/WSe_2 heterostructure	Low
IRDS 2028 targets for advanced-node silicon FETs [59]	N/A	N/A	∼0.1	I_{on} ∼ 1.2 mA·μm^{-1} $L_{ch} < 12$ nm	10^5	N/A	N/A	N/A

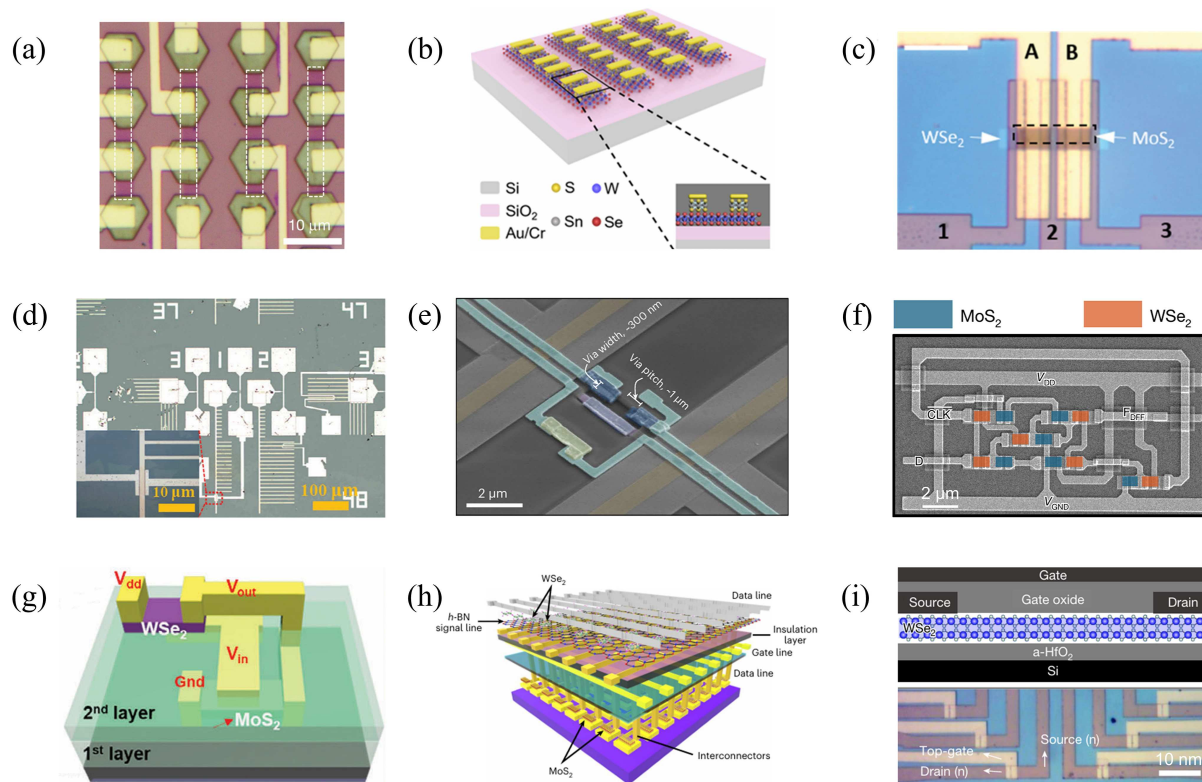

Figure 5 (Color online) WSe_2 arrays, planar integration, and M3D integration. (a) Typical optical microscopy image of back-gated WSe_2 transistors with neighboring VSe_2 nanoplates as synthetic vdW contacts [73] Copyright 2020 Springer Nature; (b) WSe_2 BAC-FET array [79] Copyright 2025 American Chemical Society; (c) device cross-sectional view of a shared-gate CMOS monolithic 3D architecture [80] Copyright 2016 John Wiley and Sons; (d) optical image of top-layer WSe_2 PFET arrays [81] Copyright 2024 John Wiley and Sons; (e) angled, false-colored SEM image of a two-tier cell corresponding to a two-stage inverter circuit [32] Copyright 2024 Springer Nature; (f) 2D CMOS combinational and sequential circuits [41] Copyright 2025 Springer Nature; (g) schematic illustration of the preparation of an M3D integrated inverter [81] Copyright 2024 John Wiley and Sons; (h) schematic diagram of an M3D-integrated AI processor [82] Copyright 2023 Springer Nature; (i) schematic of seamless M3D integration [40] Copyright 2024 Springer Nature.

overcoming critical challenges in scalable fabrication and industrial integration, which form the focus of the following discussion.

Transitioning from lab-scale micromechanical exfoliation to industrial-grade scalable design represents the first prerequisite for 2D electronics [48]. To minimize contact resistance and interface damage, synthetic vdW contacts employing VSe_2 nanoplates have been integrated with WSe_2 transistors (Figure 5(a)), providing a pristine interface for hole injection [73]. However, traditional nanofabrication processes often introduce significant degradation. Electron beam lithography (EBL) exposure can induce doping effects that reduce current density by an order of magnitude, while alkaline developers such as 4% NaOH employed in UV lithography cause a 40%–84% decline in material quality [78].

To circumvent these issues, a damage-free laser patterning technique based on photothermal oxidation was developed, enabling the high-fidelity fabrication of WSe_2 FET arrays [78]. By implementing a WSe_2/SnS_2 heterojunction system, researchers leveraged a type-III band alignment to create a bilateral accumulation contact (BAC). This mechanism facilitates carrier injection via interband tunneling and successfully reduces the R_c to $10.8\ \mathrm{k\Omega \cdot \mu m}$ (Figure 5(b)). Utilizing a self-aligned etching strategy, these BAC-FET arrays achieved a field-effect mobility ($\mu_{\rm FE}$) of 74.6 $\mathrm{cm^2{\cdot}V^{-1}{\cdot}s^{-1}}$ and a drive current of 705 µA, supporting the integration of complete logic gates such as inverters and NAND gates [79].

Beyond planar scaling, monolithic three-dimensional (M3D) integration offers a path to massively enhance integration density and reduce interconnect latency. In 2016, Sachid et al. pioneered a shared-gate M3D CMOS architecture by vertically stacking MoS_2 (n-type) and WSe_2 (p-type) functional layers (Figure 5(c)). This design circumvents the high-thermal-budget requirements of traditional silicon M3D, as 2D materials can be integrated at low temperatures (<250°C), protecting the underlying circuitry [80]. In this context, Liu et al. demonstrated high-performance complementary FETs within a stacked configuration (Figure 5(d)), confirming the electrical integrity of sequentially integrated CVD-grown monolayer n-type MoS_2 and p-type WSe_2 [81].

Recent advancements in M3D integration have been propelled by three distinct studies, which collectively advance the field toward complex functional systems. At the structural level, Pendurthi et al. (Figure 5(e)) demonstrated high-density two-tier cells featuring scaled 300 nm inter-tier vias, thereby establishing a compact physical foundation for continued logic scaling [32]. At the system level, a significant breakthrough was achieved by Ghosh et al. (Figure 5(f)) through the demonstration of a functional 1-bit one instruction set computer [41]. This work represents the first large-scale 2D system comprising over 1000 transistors and incorporates a comprehensive logic library that includes arithmetic logic units (ALUs) capable of executing "reverse subtract and skip if borrow" (RSSB) instructions, static random-access memory (SRAM) arrays, and sequential circuits (such as D-type flip-flops (DFFs)). Notably, the system exhibits exceptional energy efficiency, with picowatt-scale static power consumption and switching energies of approximately 100 pJ, thereby validating the viability of 2D materials for VLSI-compatible computing. Complementing these achievements, Liu et al. (Figure 5(g)) established a robust fabrication framework based on sequential layer transfer, employing a strict low-temperature budget below 250°C to ensure high-yield, wafer-scale production [81].

The ultimate goal of M3D integration is the realization of multifunctional "More than Moore" systems. Kang et al. in 2023 demonstrated a non-von Neumann AI processing unit by vertically integrating six layers of 2D materials, including MoS_2 transistors and WSe_2/h-BN memristors (Figure 5(h)). This architecture achieves seamless sensing, signal processing, and memory-in-logic functionality without the area overhead associated with through-silicon vias [82].

Addressing the challenge of directly growing high-quality single-crystal channels on amorphous dielectrics within the thermal budget (below 400°C) of back-end-of-line (BEOL) processes, Kim et al. introduced a geometrically confined, low-temperature selective growth strategy that enables seamless monolithic integration of heterogeneous layers [40]. This work establishes a fully growth-based vertical complementary field-effect transistor (CFET) array architecture (Figure 5(i)). In this design, high-quality single-crystal p-type WSe_2 serves as the bottom tier, while single-crystal n-type MoS_2 channels are subsequently grown in situ on the interlayer dielectric (ILD) at an ultralow temperature of 385°C, facilitated by a trench-edge-induced heterogeneous nucleation mechanism. By leveraging kinetic control within confined geometries, this strategy not only circumvents the interfacial contamination and misalignment issues inherent to conventional transfer processes but also maintains a strict low-thermal-budget window. Consequently, the growth of the top-tier MoS_2 does not induce thermal degradation in the underlying WSe_2 lattice or metal interconnects, thereby validating the wafer-scale feasibility of high-performance vertical logic circuits based on WSe_2/MoS_2 heterostructures [40].

6 Challenges and outlook

Translating WSe_2 from laboratory demonstrations to industrial CMOS applications requires overcoming critical challenges across three levels: material synthesis, device engineering, and integration technology.

At the material level, the controllable growth of high-quality, wafer-scale WSe_2 films with precise layer control remains a fundamental bottleneck. Achieving uniform growth at low temperatures while minimizing intrinsic defects is particularly challenging, as the low formation energy of selenium vacancies and other defects readily induces undesirable n-type conduction, thereby compromising p-type device performance. Advanced strategies such as the introduction of atomic-layer buffer layers can effectively modulate the interfacial edge energy between the film and the substrate, enabling precise multilayer stacking, reducing defect densities, and paving the way for reproducible large-area growth.

At the device level, high-performance WSe_2 p-type transistors are primarily constrained by contact resistance and doping instability. Two principal contact strategies, namely vdW contacts and covalent metal-semiconductor contacts (currently employed mainly for MoS_2) [83], face distinct challenges. vdW contacts preserve the pristine WSe_2 lattice and circumvent Fermi-level pinning, yet the weak interfacial coupling often results in elevated contact resistance and non-uniform carrier injection. These limitations can be mitigated by introducing ultrathin buffer layers, such as Se or h-BN, between the metal electrode and WSe_2, followed by controlled annealing to enhance interlayer coupling without introducing additional defects. Covalent contacts, in contrast, afford strong orbital overlap and efficient carrier injection, but the risk of lattice damage during deposition can introduce trap states and deep levels that degrade device performance. Employing protective buffer layers in conjunction with selective thermal annealing enables controlled covalent bonding, thereby balancing robust coupling with lattice preservation. Furthermore, optimized doping techniques including chemical passivation and interlayer charge transfer can further enhance p-type conductivity, facilitating low-resistance, high-transconductance devices suitable for complementary CMOS circuits.

From the integration perspective, realizing high-density, wafer-scale, vertically stacked circuits introduces additional process challenges. Precise layer alignment, uniform thickness control, and well-defined crystallographic orientation are essential prerequisites for maintaining consistent electrical performance across large areas. Low-temperature processing and damage-free transfer techniques are equally indispensable to prevent degradation of previously fabricated layers. Interlayer contacts and vias must be formed with minimal resistance and without contamination, while lithography and patterning processes must preserve interface integrity. The synergistic application of multiple strategies, including atomic-layer controlled growth, vdW stacking, laser-assisted patterning, polymer-mediated transfer, and self-aligned via formation, provides a viable pathway toward reproducible, low-resistance interconnects and high-density 3D integration. Consequently, M3D integration of WSe_2 pMOS devices with n-type 2D semiconductors offers promising opportunities for enhancing device density, reducing interlayer power consumption, and enabling multifunctional system capabilities.

Ultimately, coordinated optimization across material synthesis, contact engineering, and integration processes is essential to establish industrially viable WSe_2-based 2D CMOS platforms and to bridge the gap between experimental prototypes and large-scale manufacturing.

7 Summary

WSe_2 has emerged as a leading p-type 2D semiconductor, owing to its atomic-scale thickness, direct bandgap, excellent stability, and superior hole transport properties. Significant advances in controllable growth, from microscale single crystals to wafer-scale, layer-controlled films, have enabled the production of high-quality, uniform monolayers and bilayers suitable for large-area device fabrication. At the device level, vdW contact engineering, buffer-layer-assisted interfaces, and interlayer charge transfer doping have effectively reduced contact resistance and stabilized p-type operation, thereby enabling high-performance pMOS transistors. The integration of WSe_2 into complementary CMOS and 3D stacked architectures further demonstrates its potential for ultrahigh-density, low-power, and multifunctional circuits. Coordinated progress in synthesis, interface engineering, and processing thus establishes WSe_2 as a clear pathway toward scalable, energy-efficient, and industrially viable 2D electronics, paving the way for the next generation of post-silicon semiconductor technologies.

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