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Special Topic: Advanced Optoelectronics Based on Two-Dimensional Materials

Asymmetric WSe_2 reconfigurable devices for logic-in-memory computing: contact barrier engineering and floating gate-controlled operation

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Abstract The explosive growth of artificial intelligence, autonomous driving, and the Internet of Things demands edge devices capable of making localized decisions within milliseconds. This imposes considerable requirements on the energy efficiency of hardware. Traditional von Neumann architectures suffer from serious energy consumption issues owing to the separation of memory and computing modules. This study developed an asymmetric WSe_2/h-BN/graphene (Gr) reconfigurable floating-gate field-effect transistor (AFGFET). The reconfigurability of device functionality is achieved by dynamically adjusting the Schottky barrier through asymmetric Au/Gr electrodes and floating-gate charge storage, which integrates logical reconfigurability and nonvolatile storage within a single device. By simply changing the source-drain bias and the back-gate voltage, six Boolean logic functions, namely, NAND, IMP, NOT, TRUE, AND, and NIMP, can be dynamically executed. Compared with traditional static complementary metal-oxide-semiconductor (CMOS) logic-in-memory (LIM) circuits implementing the same logic functions, the usage of transistors is reduced by 87.5%. Owing to the modulation effect of the employed engineering technology, the transistors can be flexibly adjusted to exhibit bipolar or p-type characteristics. When used as a memory, endurance of $> 10^3$ cycles and retention time of > 2000 s can be achieved, demonstrating nonvolatile storage capabilities. The developed AFGFET, which combines logical reconfigurability and nonvolatile storage characteristics, will open up a new paradigm for high-density, low-power storage.

Keywords reconfigurable transistor, logic-in-memory, floating gate, asymmetric, contact barrier engineering

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1 Introduction

Emerging technologies, such as artificial intelligence, robots, the Internet of Everything, and autonomous driving, have catalyzed an unparalleled surge of progress but have large-scale data processing requirements. Traditional "Von Neumann" architectures inadequately address these requirements, posing a considerable obstacle to the advancement of emerging technologies [1–4]. To address speed and power consumption limitations from the separation of memory and computation, integrating these two functions into a single device that unifies logic operations and data storage has become a key focus of modern scientific research [5,6]. Traditional three-dimensional semiconductors face severe scaling bottlenecks owing to their interface defects and fixed-function architectures [7, 8]. Two-dimensional (2D) materials provide pathways via which these physical limitations may be surpassed through their atomic thickness, dangling-bond-free surfaces, and tunable bandgaps [9,10]; as such, 2D materials can catalyze breakthroughs in high-performance logic and neuromorphic computing [10–14]. Transition metal dichalcogenides, particularly WSe_2, serve as highly effective platforms for such advancements. Leveraging its intrinsic ambipolar transport capabilities, WSe_2 enables dynamic gate-controlled transitions between n-type and p-type modes. This unique reconfigurability is pivotal for developing next-generation multifunctional logic circuits with substantially enhanced functional density and architectural versatility [15–26]. Additionally, the interface between electrodes and channel materials plays a decisive role in device performance. Owing to the low density of states and weak Fermi pinning effect of WSe_2, the electrode-WSe_2 contact readily forms a large Schottky barrier, considerably affecting carrier injection [27, 28].

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In recent years, contact barrier engineering has successfully adjusted the contact barrier through the selection of diverse electrodes (e.g., Ti, Au, and graphene (Gr)) and thereby modified device characteristics such as threshold voltage and carrier transport [29–34].

The transition toward next-generation intelligent computing necessitates the integration of reconfigurable logic and nonvolatile memory into unified LIM architectures [21, 22, 35]. Existing 2D reconfigurable devices offer exceptional flexibility in executing multiple Boolean functions within a minimal footprint, considerably reducing the hardware redundancy associated with conventional complementary metal-oxide-semiconductor technology [21,22,36–38]. However, traditional multigate devices suffer from excessive structural complexity and high interconnect density, hindering their large-scale scalability. Additionally, the functional density of existing 2D reconfigurable devices remains limited, such that individual devices can typically implement only a few types of logic gates with limited complexity, and most lack integrated nonvolatile memory capability—hindering the realization of true LIM architectures [21, 22, 35–41]. The performance of these devices is often degraded by metal-semiconductor interface issues, such as strong Fermi-level pinning and high contact resistance, which reduce the switching ratio and energy efficiency. Consequently, designing simplified device geometries by harnessing intrinsic physics (e.g., contact barrier engineering) and floating-gate structures is crucial for realizing high-performance, low-power, and integrated reconfigurable LIM devices.

This study presents a synergistic regulatory approach utilizing contact barrier engineering and floating gate storage. Transistors are fabricated from the van der Waals heterostructures of 2D materials, namely, Au electrodes, Gr electrodes, WSe_2, hexagonal boron nitride (h-BN), and Gr. Unlike conventional reconfigurable WSe_2 devices that can only alternate between n-type and p-type FETs through gate control, this device facilitates dynamic switching of Boolean logic, such as NAND and IMP, by utilizing different source electrodes. Moreover, the device can attain different initialization states by modifying the charge of the floating gate using gate voltage to execute the NIMP logic function. The conventional WSe_2 floating gate field-effect transistor is limited by its intrinsic bipolar conductivity, hindering nonvolatile on/off state operation via exclusive floating-gate charge modulation. This device can write or erase the floating gate charge (electrons or holes) in a nonvolatile manner using gate voltage pulses, harnessing the highly sensitive characteristics of the electrode-WSe_2 Schottky barriers to enable dynamic conduction switching within the channel.

2 Results and discussion

Figure 1(a) shows the configuration of the asymmetric WSe_2/h-BN/Gr reconfigurable floating-gate field-effect transistor (AFGFET), fabricated via mechanical exfoliation of bulk crystals and PDMS-assisted dry transfer. The AFGFET utilized Au and Gr contact designs to achieve asymmetric carrier injection characteristics. Both electrodes were fabricated via the van der Waals transfer process to reduce interfacial defects and the Fermi pinning effect induced by high-energy particle bombardment characteristics in traditional deposition techniques [42,43]. Energy band alignment analysis reveals that asymmetric carrier injection in the WSe_2 channel stems from the differing work functions of Au and Gr. The work function of Gr is 4.6 eV, which is considerably close to the conduction band of WSe_2 ($E_C \approx 4.1$ eV) and the valence band ($E_V \approx 5.1$ eV), thereby providing a low potential barrier for electron and hole injection and exhibiting bipolar transport characteristics [17, 34, 44]. The work function of Au (5.1 eV) is also close to the valence band top of WSe_2, considerably reducing the hole injection barrier; however, the large energy difference between Au and the conduction band bottom results in a low electron injection efficiency [45]. The asymmetric contact configuration tailors carrier transport pathways via energy band engineering, laying a physical foundation for the device's polarity reconfigurability.

Figures 1(b) and (c) show optical microscope and atomic force microscopy (AFM) images of the AFGFET. Figure 1(d) shows the measured thicknesses of the heterojunction along the dashed line in Figure 1(c). The thicknesses of h-BN, Gr (floating gate), Gr (electrode), and WSe_2 are 18, 5, 10, and 6 nm, respectively. To verify the stacking sequence and lattice integrity of the fabricated van der Waals heterostructure, micro-Raman spectroscopy (excitation wavelength: 532 nm) was performed on two representative regions of the device. As shown in Figure 1(e), the spectrum acquired from the Gr/h-BN/Gr region (red curve) exhibits the characteristic D ($\sim$1350 cm^{-1}), G ($\sim$1582 cm^{-1}), and 2D ($\sim$2680 cm^{-1}) peaks of Gr, in addition to the E_{2g} mode of h-BN at $\sim$1366 cm^{-1}, thereby confirming the formation of an intact Gr/h-BN/Gr stacked configuration. In the WSe_2/h-BN/Gr region (blue curve in Figure 1(e)), in addition to the Gr and h-BN signatures, three distinct Raman features appear in the low-frequency range, which are assigned to the intrinsic E^1_{2g} ($\sim$250 cm^{-1}) and A_{1g} ($\sim$260 cm^{-1}) vibration modes of WSe_2, and a second-order Raman scattering peak appears at $\sim$308 cm^{-1}. The simultaneous observation and unambiguous assignment of these peaks provide direct evidence that the WSe_2/h-BN/Gr van der Waals heterostructure is reliably constructed,

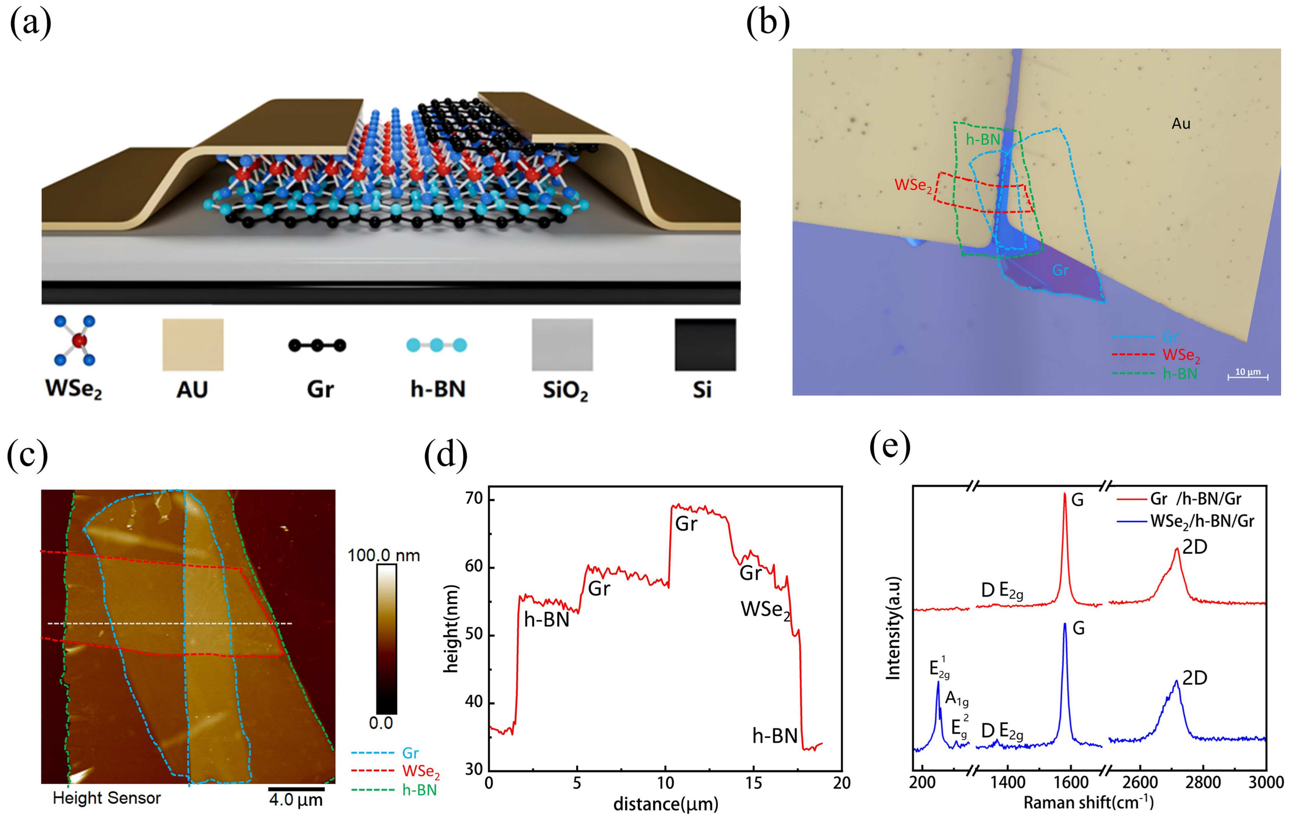
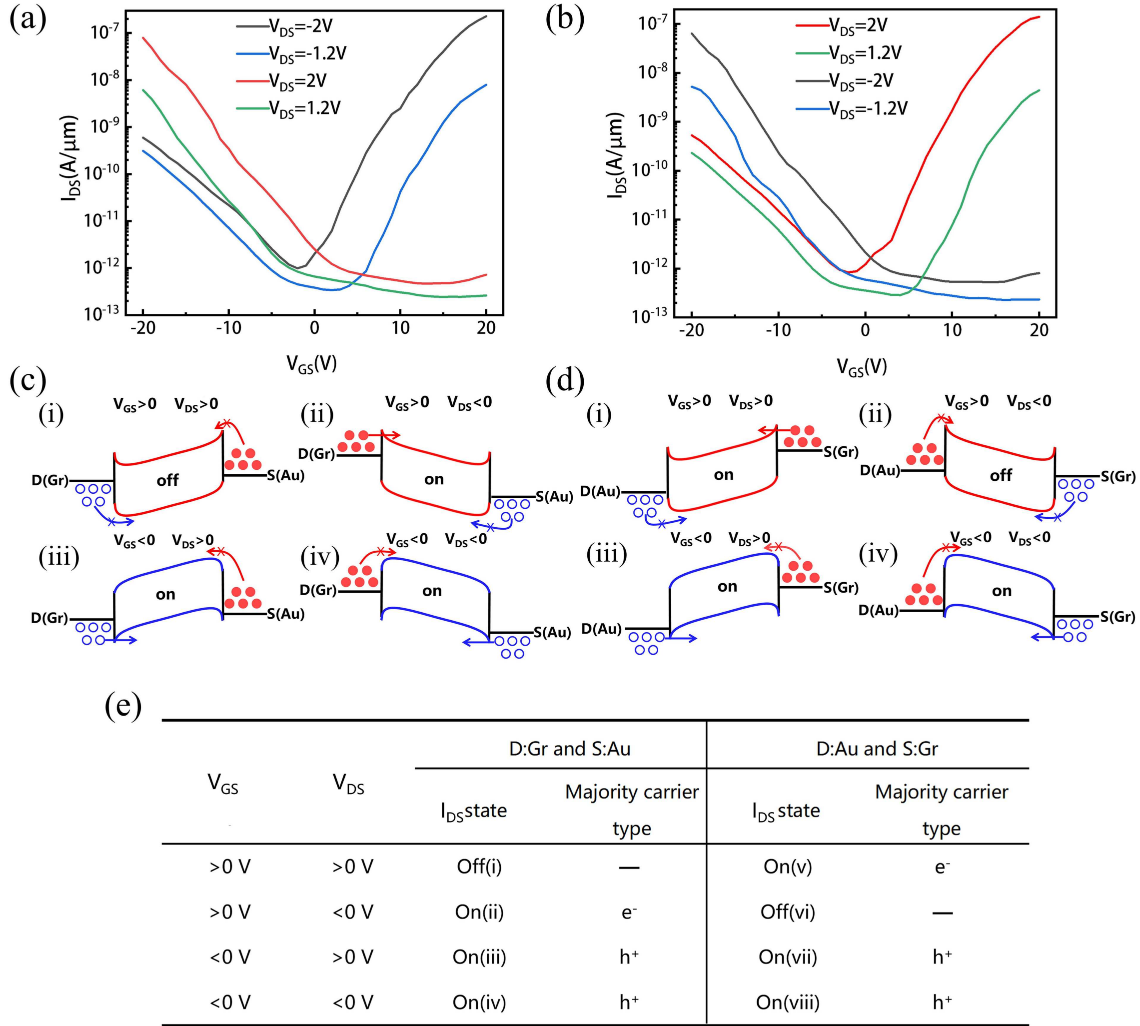


Figure 1 (Color online) Structure and characterization of AFGFET. (a) Structures of asymmetric reconfigurable floating gate transistors stacked sequentially using two different electrode stacks of floating gate Gr/floating-gate dielectric h-BN/2 μm WSe_2 channel/Gr and Au; (b) annotated optical microscope image showing a typical device; (c) AFM image of AFGFET; (d) thicknesses of each layer of device material extracted from the white dashed line in panel (c); (e) Raman spectra obtained from the Gr/h-BN/Gr electrode (red) and WSe_2/h-BN/Gr heterostructure (blue) regions.

and that all constituent layers of the heterostructure retain good integrity after stacking. Prefabricated 100-nm-thick Au electrodes were then transferred onto the heterostructure, using a 300 nm SiO_2 dielectric layer on p^+ Si as the substrate.

The transfer characteristics of the AFGFET and the fundamental logical properties in the floating gate charge neutral state are shown in Figure 2. To reduce the influence of the floating gate charge storage effect on test results, the back-gate voltage (V_{GS}) is swept from −20 to +20 V. This avoids excessively high electric fields that can cause tunneling of channel carriers through the h-BN floating-gate dielectric layer. Figure 2(a) shows the transfer characteristics when using Gr as the drain and Au as the source. Substantial carrier polarity modulation behaviors are observed at drain voltages (V_{DS}) of −2 and −1.2 V. The AFGFET shows bipolar transport characteristics. When V_{DS} is 2 and 1.2 V, the device exhibits unipolar p-type characteristics [46, 47]. By exchanging the source and drain terminals, the opposite results are obtained, as shown in Figure 2(b), where the device exhibits unipolar p-type and bipolar transport characteristics at $V_{DS} < 0$ and $V_{DS} > 0$ V, respectively. The AFGFET controls determine the conductive state by manipulating different source-drain electrodes, V_{DS}, and V_{GS}. The intricate manipulation of electrical properties allows the AFGFET to adaptively configure various logic functions, thereby enabling logic operations through simple condition switching and effectively serving as a reconfigurable logic device.

Figure 2(c) shows the energy band diagram when Au is used as the source electrode and Gr as the drain electrode. Applying a positive V_{GS} leads to electron accumulation in the channel due to the effect of the electric field, causing the energy band of WSe_2 to bend downward and decrease the Schottky barrier height at the source-drain interface. However, the high work function of the Au electrode considerably hinders electron injection efficiency. The increased Schottky barrier height at the drain simultaneously restricts hole injection (Figure 2(c)(i)). When $V_{DS} < 0$ V, the work function of Gr (4.5 eV) is strongly consistent with the intrinsic Fermi level of WSe_2 ($E_F \approx 4.5$ eV). This lowers the Schottky barrier height, which promotes the effective injection of electrons into the channel through the quantum tunneling effect. The increased Schottky barrier for holes at the source terminal prevents them from overcoming the barrier and reaching the channel (Figure 2(c)(ii)). When a negative V_{GS} is applied, the attraction



V_{GS}	V_{DS}	D:Gr and S:Au		D:Au and S:Gr	
		I_{DS} state	Majority carrier type	I_{DS} state	Majority carrier type
>0 V	>0 V	Off(i)	—	On(v)	e^-
>0 V	<0 V	On(ii)	e^-	Off(vi)	—
<0 V	>0 V	On(iii)	h^+	On(vii)	h^+
<0 V	<0 V	On(iv)	h^+	On(viii)	h^+

Figure 2 (Color online) Band diagrams showing the transfer characteristics of the device, and examination of the operating principle of the asymmetric reconfigurable floating gate transistor. (a) Au as source, Gr as drain. Drain current ($I_{\rm DS}$)-$V_{\rm GS}$ transfer characteristic curves of the device for different values of $V_{\rm DS}$ (-2, -1.2, 1.2, and 2 V). (b) Gr as source, Au as drain. $I_{\rm DS}$-$V_{\rm GS}$ transfer characteristic curves of the device for different values of $V_{\rm DS}$ (-2, -1.2, 1.2, and 2 V). (c) Influence of different $V_{\rm GS}$ and $V_{\rm DS}$ on energy bands and carriers when using Au as the source and Gr as the drain. (d) Influence of different $V_{\rm GS}$ and $V_{\rm DS}$ on energy bands and carriers when using Gr as the source and Au as the drain. (e) Eight current states and majority carrier types under different bias and electrode configurations, corresponding to the energy band diagrams in (c) and (d).

of negative voltage leads to hole accumulation in the device channel and an upward bending of the conduction and valence bands of WSe_2. When $V_{\rm DS} > 0$, the source terminal creates a substantial barrier for electrons, which considerably impedes electron injection into the channel. Furthermore, the drain terminal facilitates hole injection into the channel due to the reduction of the Schottky barrier (Figure 2(c)(iii)). Conversely, when $V_{\rm DS} < 0$, the reduction of the p-type Schottky barrier at the source promotes efficient hole injection into the channel, whereas the increased Schottky barrier for holes at the drain hinders this process (Figure 2(c)(iv)). Exchanging the source and drain electrodes causes the opposite situation, as shown in Figure 2(d). This comparison illustrates the cooperative interaction between electrode materials and bias voltages in guiding the transport of charge carriers. Figure 2(e) further summarizes these eight current states and their corresponding majority carrier types under varying bias conditions and electrode configurations, with sub-labels (i)–(viii) directly mapping to the energy band diagrams in Figures 2(c) and (d). This concise summary, rooted in the underlying energy band analysis, provides an intuitive reflection of the rich functional diversity of the AFGFET device. (Figure 2(e) presents an energy band analysis that visually represents eight current states, reinforcing the functional diversity of AFGFET devices.) Compared with most conventional FETs, the AFGFET can achieve considerably more current states while maintaining structural simplicity [19, 26, 48–50].

The reconfigurable logic functions obtained by AFGFETs were considered. $V_{\rm GS}$ and $V_{\rm DS}$ act as input signals

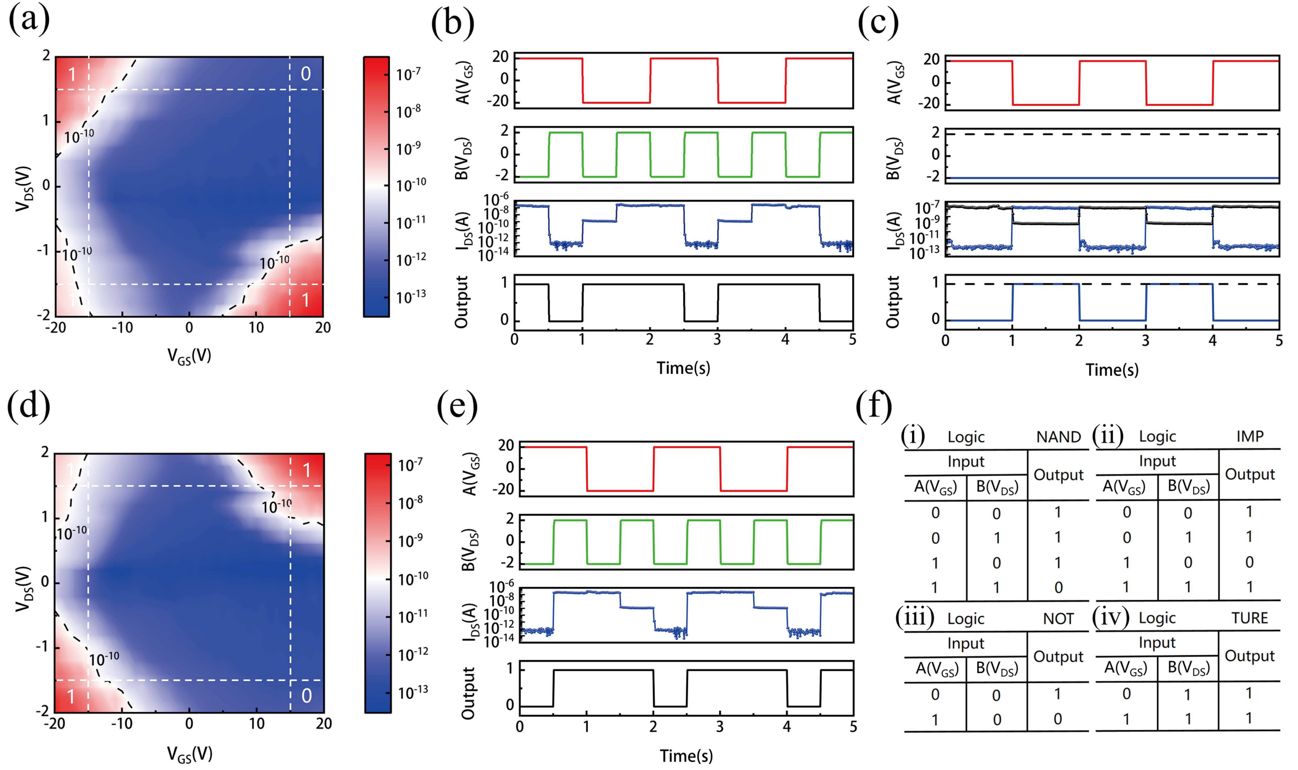


Figure 3 (Color online) Electrical characteristics and reconfigurable logic operation of AFGFET. (a) 2D contour plot showing the channel current I_{DS} for back-gate voltage V_{GS} and drain voltage V_{DS} when using Gr as the drain electrode; (b) timing of NAND logic for inputs (V_{DS}, V_{GS}) and outputs (I_{DS}); (c) timing of NOT and TRUE logic; (d) 2D contour plot showing the channel current I_{DS} for back-gate voltage V_{GS} and drain voltage V_{DS} when using Au as the drain electrode; (e) timing of IMP logic; (f) truth tables corresponding to NAND, IMP, NOT, and TRUE logic.

A and B, and the drain current (I_{DS}) acts as the output signal. Boolean logic functions can be achieved by changing the combinations of input signals A and B. Figures 3(a) and (d) show the values of I_{DS} as a function of the relationship between V_{GS} and V_{DS}, using Gr and Au, respectively, as the drain electrode. The V_{DS} and V_{GS} ranges are -2 to $+2$ V and -20 to $+20$ V, allowing four current states to be obtained in four quadrants. To further illustrate the logic function, V_{DS} values of -2 and $+2$ V and V_{GS} values of -20 and $+20$ V are assigned as the binary values of 0 and 1 for input signals A and B. When I_{DS} is greater/less than 10^{-10} A, the logic output is 1/0. The temporal logic for different inputs and outputs is shown in Figures 3(b), (c), and (e). When using Gr as the drain electrode and maintaining input signal B at logic 0, the output demonstrates an inverse logic relationship with the input signal A, corresponding to NOT logic (blue curve). Conversely, when the input signal B is assigned logic 1, the output remains at a high level, independent of the value of input signal A, corresponding to TRUE logic (black curve). Figure 3(f) presents the truth table. Traditional metal-oxide-semiconductor field-effect transistor devices require four devices for NAND logic; the AFGFET reduces this number by 75% for NAND and 87.5% for IMP (compared to a static CMOS realization of the same logic function) while achieving logical conversion through reconfigurable logic.

The charges stored in the floating gates can modify the logic state of the device, thereby enabling functional reconfiguration. Figure 4(a) demonstrates that the application of a back-gate voltage pulse ($V_{\text{GS-Pulse}} = -50$ V; 10 ms) leads to accumulation in the WSe_2 channel, which causes considerable upward bending of the conduction and valence bands of WSe_2. When the back-gate voltage pulse exceeds a specific threshold, the strong electric field at the WSe_2/h-BN interface drives accumulated holes to tunnel through the h-BN barrier layer, forming nonvolatile storage charges. The localized electric field facilitates the induction of electrons as major carriers, enabling the AFGFET to exhibit stable n-type transistor characteristics (Figure 4(b)).

Figure 4(c) shows the transfer characteristic curves (I_{DS}-V_{GS}) at different V_{DS} after applying a back-gate voltage with a pulse width of 10 ms and amplitude of -50 V when using Gr as the drain material. Applying a scanning voltage ($V_{\mathrm{GS}} = -20$ to $+20$ V) to the back-gate achieves synergistic manipulation of channel characteristics via floating gate charge and back-gate voltage. When using a back-gate voltage of zero ($V_{\mathrm{GS}} = 0$ V), the n-type channel produced by the floating gate storage charge dominates the device function, resulting in the activation of

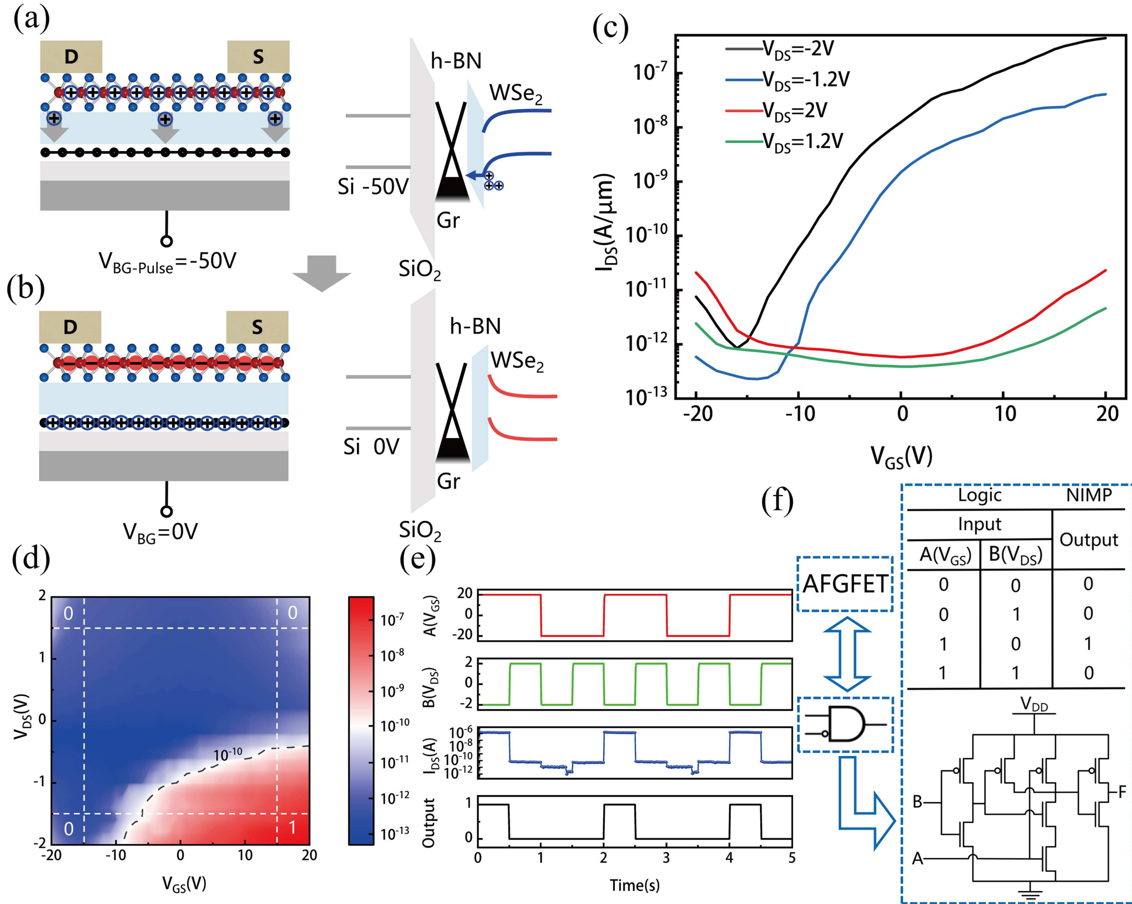


Figure 4 (Color online) Electrical characterization and reconfigurable logic operation of the added floating gate-regulated AFGFET. (a) A large negative gate voltage pulse and (b) the energy diagram of the zero-bias AFGFET after the pulse. Using Gr as drain and after initialization of negative gate voltage pulse; (c) $I_{\rm DS}$-$V_{\rm GS}$ transfer characteristic curves of the device for different values of $V_{\rm DS}$ and (d) 2D contour plots showing channel current $I_{\rm DS}$ with respect to the back-gate voltage $V_{\rm GS}$ and drain voltage $V_{\rm DS}$; (e) timing of NIMP logic; (f) characterization of AFGFET for NIMP logic operation: logic symbol, truth table, and static CMOS circuit.

the transistor ($I_{\rm DS} \approx 10^{-8}$ A/μm). Upon applying a negative back-gate voltage ($V_{\rm GS} = -20$ V), hole accumulation occurs in $\rm WSe_2$ owing to the back-gate electric field, and the positive charge on the floating gate attracts electrons or repels holes. The two processes oppose one another in channel carrier modulation, leading to a considerable reduction in net channel carrier concentration and low current levels ($I_{\rm DS} = 10^{-11}$ A/μm). In contrast, when a positive back-gate voltage ($V_{\rm GS} = +20$ V) is applied, the back-gate electric field and the electric field generated by the floating gate storage charge facilitate the induction or accumulation of electrons in the channel. The synergistic effect of these two phenomena considerably increases the channel electron concentration, producing a high on-state ($I_{\rm DS} = 10^{-7}$ A/μm) device. The on/off ratio transfer characteristic standard unipolar n-type transistor behavior exceeds 10^5, consistent with physical mechanisms based on the modulation of channel carrier type and concentration by floating gate charge. Figure 4(d) illustrates the distribution of $I_{\rm DS}$ as a function of $V_{\rm DS}$ and $V_{\rm GS}$. Figure 4(e) shows the timing logic. The NIMP logic is achieved by the AFGFET, and the number of devices is reduced by 87.5% compared with that required in the conventional configuration. Figure 4(f) characterizes the NIMP logic operation of the AFGFET, including the logic symbol, truth table, and corresponding static CMOS circuit. As NIMP logic is relatively uncommon in conventional circuits, the supplemented CMOS circuit intuitively illustrates the traditional implementation, which highlights the transistor count reduction advantage of the AFGFET. The electrical characterization performed before and after the specified pulse operation indicates that AFGFETs with an asymmetric structure and nonvolatile floating gate modulation provide considerable advantages: the progress and transfer of 2D materials at the wafer level provide a fundamental foundation for devices that enhance the integrated density of integrated circuits and facilitate low-static-power-consumption logic functions [51–55].

Further characterization of the storage characteristics of the device was conducted, as shown in Figure 5. The insulating properties of h-BN and its atomically flat, non-dangling bond surface can reduce carrier scattering, and the high mobility of Gr can improve the effective charge storage capacity [56–60]. Figure 5(a) shows the endurance

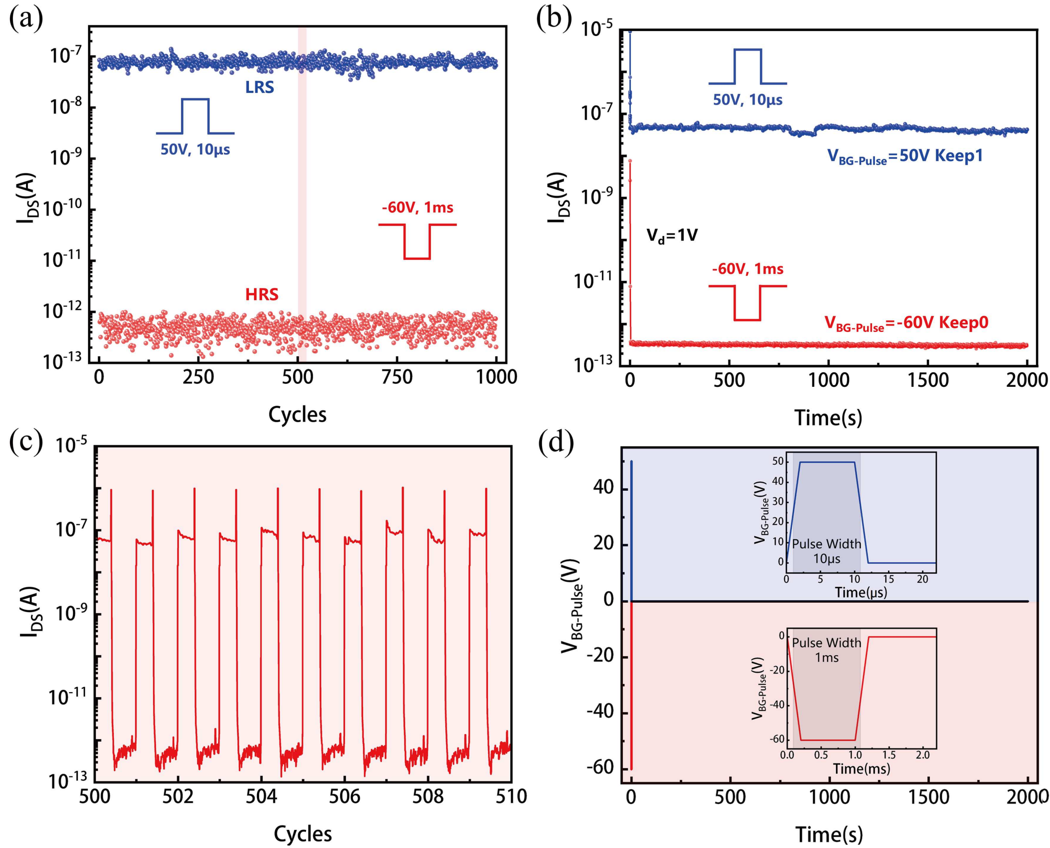


Figure 5 (Color online) Device storage characteristics when using Gr as the drain and Au as the source, $V_{\rm DS}$ = 2 V. (a) Endurance of the memory device at 1000 cycles for erase/programming voltage pulses of 50 and −60 V and pulse widths of 10 μs and 1 ms; (b) and (d) plots showing the retention performance of p-type transmission versus drain current over 2000 s for high- and low-current states; infographics of pulses applied during the test; (c) typical drain current switching waveforms during cycles 500–510.

characteristic at $V_{\rm DS}$ = 2 V when using Gr and Au as the drain and the source electrode. The programmed state (ON; low-resistance state, LRS) and erased state (OFF; high-resistance state, HRS) can be reversibly switched by applying different $V_{\rm GS}$ pulses. After 10^3 cycles of programming and erasure, no substantial degradation was observed in the device. Figure 5(b) shows the retention characteristics of the AFGFET; to further evaluate its reliability and transient switching behavior, Figure 5(c) shows a magnified view of endurance cycles 500–510. The device demonstrates highly reproducible and abrupt switching between the LRS and HRS, with a consistent memory window of approximately five orders of magnitude, underscoring the robust bistable nature of the heterostructure. For the nonvolatile retention tests, specific gate pulse configurations were implemented to trigger the programming and erasure processes, as detailed in Figure 5(d). A programming pulse of 50 V with a duration of 10 μs was employed to achieve the LRS (Keep 1), while an erasing pulse of 60 V with a longer duration of 1 ms was applied to return the device to the HRS (Keep 0). After these excitations, the temporal evolution of the drain current $I_{\rm DS}$ was monitored at a quiescent back-gate voltage of $V_{\rm GS}$ = 0 V. As shown in Figure 5(b), both memory states exhibit negligible decay and remain distinct for > 2000 s, confirming that the h-BN/Gr interface provides an effective charge storage. This combination of high endurance and persistent retention emphasizes the potential of the AFGFET for high-performance, low-power, nonvolatile memory applications [44–47, 61]. The current ratios achieved in high and low resistive states remain at 10^5 after 2000 s of retention time, and the outstanding endurance and retention characteristics indicate that AFGFET has remarkable nonvolatile storage capacity. To more clearly illustrate the comprehensive performance advantages of our AFGFET for LIM computing, key performance metrics against recently reported 2D reconfigurable devices and LIM devices are summarized in Table 1.

3 Conclusion

This study fabricated an asymmetric reconfigurable floating gate transistor. By designing asymmetric Au and Gr electrodes, the carrier injection polarity was changed. The floating gate was utilized to overcome the functional

Table 1 Key performance metrics comparison of recent 2D reconfigurable devices and logic-in-memory devices.

Materials	On/off ratio	Endurance	Retention (s)	Logics per device	Reference
WSe_2/h-BN/Gr/SiO_2/Si	10^4	–	800	4	[22]
WSe_2/h-BN/$CuInP_2S_6$/Au	10^5	–	10000	3	[25]
WSe_2/AuNPs/h-BN/Au/SiO_2/Si	10^3	–	100	4	[38]
WSe_2/h-BN/Au/SiO_2/Si	10^6	–	–	3.5	[39]
WSe_2/SiO_2/Si	10^4	100	600	–	[40]
WSe_2/h-BN/Au/SiO_2/Si	10^5	–	–	4	[41]
MoS_2/$CuInP_2S_6$/SiO_2/Si	10^6	10000	3000	–	[41]
WSe_2/h-BN/HfO_2/Al_2O_3/Au(Ti)/SiO_2/Si	10^4	1000	1000	2	[62]
Gr/WSe_2/h-BN/Gr/SiO_2/Si	10^5	1000	2000	6	This work

limitations of traditional reconfigurable devices. A single device exhibited logical reconfigurability and realized six Boolean logic functions, namely, NAND, IMP, NOT, TRUE, AND, and NIMP. Compared with traditional structures, the number of transistors could be reduced by 75%–87.5%. Nonvolatile switching between the programmed state (ON) and the erased state (OFF) could be achieved by adjusting the floating gate charge with voltage pulses, attaining an on/off ratio of approximately 10^5. The device showed excellent durability over 10^3 cycles and a retention capability of > 2000 s. Despite the superior performance and functional advantages of the AFGFET, this work has inherent limitations, and its practical wafer-scale application faces typical challenges for 2D devices: mechanical exfoliation fabrication causes poor contact uniformity and low performance reproducibility, large-scale heterostack integration is hampered by transfer-induced interface defects, and the device requires a relatively high operating bias voltage. Future research will focus on three aspects: optimizing preparation processes via wafer-scale epitaxial growth and high-precision transfer techniques to improve integration uniformity and reduce interface defects, refining contact barrier engineering to lower operating bias and enhance device stability, and exploring arrayed integration design to advance the practical application of AFGFETs in LIM circuits. This LIM computing configuration has the potential to drive the development of intelligent hardware in the post-Moore's era. Looking forward, the synergistic design paradigm of contact barrier engineering and floating-gate modulation in 2D van der Waals heterostructures is expected to not only break the inherent memory-computing separation bottleneck of the von Neumann architecture, advance high-density, low-power edge and neuromorphic computing, and offer a promising solution for the rapidly growing demand for efficient data processing in AIoT and autonomous driving, but also provide a generalizable, referable design framework for functional device development based on other 2D material systems.

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