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• Supplementary File •

High threshold voltage and enhanced threshold voltage stability of Schottky p-GaN gate HEMT by p-GaN bridge engineering

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Appendix A Device structure and fabrication

The epitaxial wafer was grown by metal organic chemical vapor deposition on Si substrates. The epitaxial structure consisted of a GaN buffer layer, a 200-nm-thick undoped GaN channel layer, a 15-nm-thick undoped $Al_{0.2}Ga_{0.8}N$ barrier layer, a 70-nm-thick Mg-doped p-GaN cap layer. The Mg concentration in p-GaN layer is approximately 3×10^{19} cm^{-3}. Device fabrication began with etching the p-GaN cap layer using a Cl/N/O gas mixture at a slower etch rate to achieve selective etching. The surface was treated with hydrofluoric acid to remove oxides from the surfaces of AlGaN and p-GaN after etching. Then ohmic contact metal (Ti/Al/Ni/Au= 20/160/55/45 nm) was formed by an E-beam evaporator and rapid thermal annealing at 810 °C for 30 s in N_2. Mesa isolation was conducted by dry inductively coupled plasma etching (ICP), and a 90-nm-thick Si_3N_4 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). Finally, the gate contact window of the p-GaN layer was formed by ICP etching, and the Ti/Al/Ti (50/200/100 nm) gate metal was deposited by magnetron sputtering. Figure A1 illustrates the structure and micrograph of a p-GaN gate HEMT with multiple p-GaN bridges (PB-HEMT), where the p-GaN bridges connect the p-GaN in the gate region to the source and make full contact with the ohmic metal. Conventional p-GaN gate HEMTs (C-HEMTs) without p-GaN bridges were also fabricated for comparison. The gate length, gate to source length, gate to drain length, and gate width are 4 μm, 2.5 μm, 15 μm, 50 μm, respectively. The length of the gate metal foot is 2 μm. PB-HEMTs with 1, 2, 3, 4, and 5 bridges were manufactured, each with a single bridge width of 5 μm. Device characteristics measurements were carried out with the Keithley 4200 and Keysight B1505A semiconductor parameter analyzer.

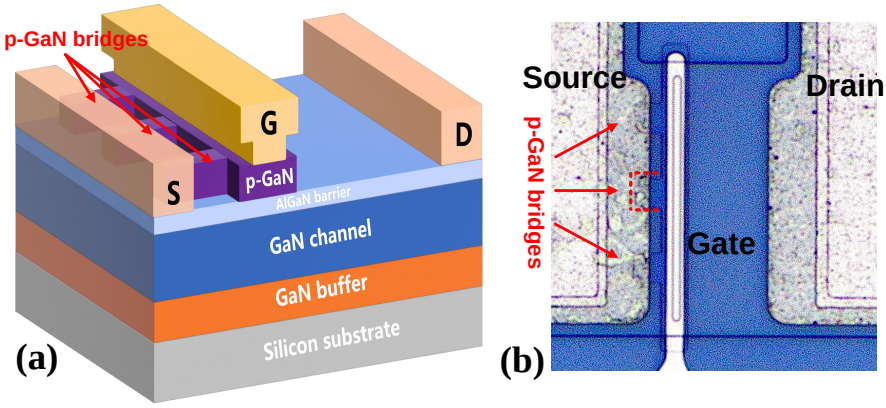

Figure A1 (a) Schematic diagram and (b) Micrograph of a p-GaN gate HEMT with multiple p-GaN bridges (PB-HEMT).

Appendix B Electrical performances

Figures B1(a) shows the transfer characteristics of the C-HEMT and PB-HEMTs with 1, 2, 3, 4, and 5 bridges. Defining V_{TH} as V_{GS} when the drain current reaches 0.1 mA/mm, the V_{TH} of C-HEMT is 1.66 V. For the PB-HEMT, the V_{TH} are

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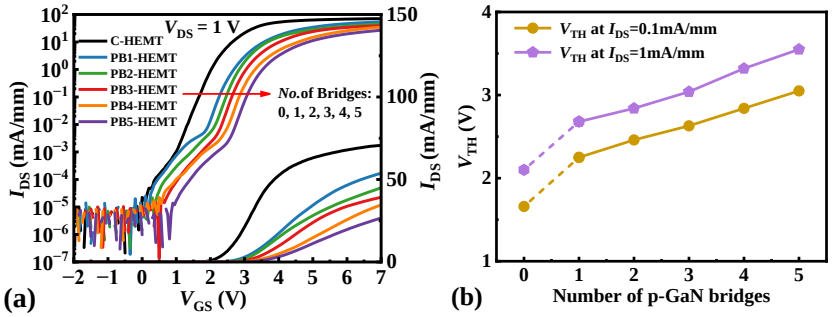

Figure B1 (a) Transfer characteristics of C-HEMT and PB-HEMT with 1, 2, 3, 4, and 5 bridges. (b) V_{TH} as a function of the number of p-GaN bridges.

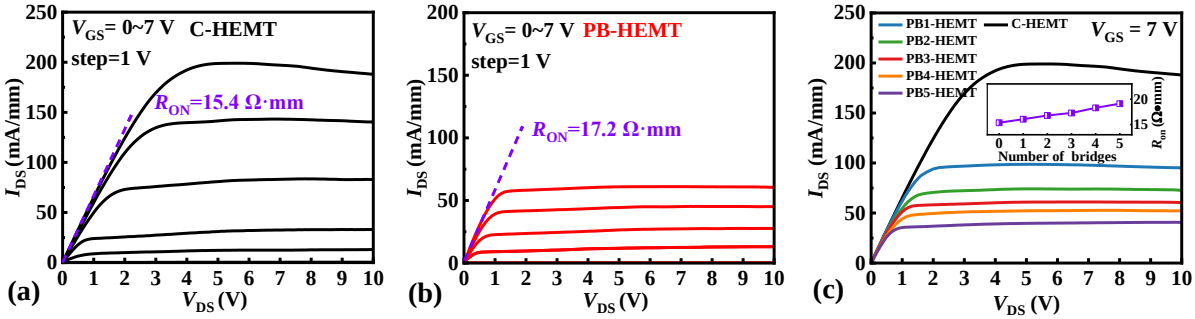

Figure B2 Output characteristics of (a) C-HEMT and (b) PB-HEMT (with 3 bridges). (c) I_{DS}-V_{DS} characteristics of C-HEMT and PB-HEMTs with 1, 2, 3, 4, and 5 bridges at V_{GS}=7 V.

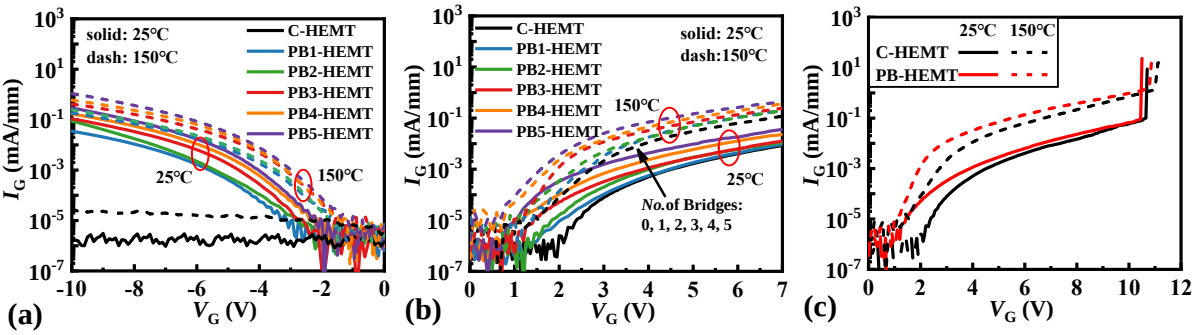

Figure B3 (a) Gate reverse leakage and (b) gate forward leakage characteristics of C-HEMT and PB-HEMTs at 25°C and 150°C. (c) Gate forward breakdown characteristics of C-HEMT and PB-HEMT with 3 bridges.

2.25 V, 2.46 V, 2.63 V, 2.84 V, and 3.05 V for devices with 1 to 5 bridges, respectively. As depicted in Figure B1(b), the V_{TH} of PB-HEMT is significantly increased, and a wide range of V_{TH} can be achieved by varying the number of bridges.

Figurs B2(a) and (b) show the output characteristics of a C-HEMT and a PB-HEMT with three p-GaN bridges, respectively. At V_{GS}= 7 V, the C-HEMT has an on-risitance (R_{on}) of 15.4 Ω·mm, while the PB-HEMT with 3 bridges has an R_{on} of 17.2 Ω·mm. The I_{DS}-V_{DS} characteristics of C-HEMT and PB-HEMTs with multiple p-GaN bridges at V_{GS}= 7 V are illustrated in Figure B2(c). As the number of p-GaN bridges increases, the device's drain saturation current decreases, and the R_{on} increases, which can be attributed to the increase in V_{TH}. Two additional factors contribute to the low drain saturation current: the low drain saturation voltage leads to premature current saturation, and the effective channel width is reduced due to depletion of the p-GaN bridges near the source. In fact, small saturation currents may help improve the short-circuit reliability of power HEMT [1, 2]. Notably, the on-resistance does not increase significantly, likely because the p-GaN bridge is electrically connected to the gate. This allows the forward gate voltage to control the enhancement of the two-dimensional electron gas (*2DEG*) density in the channel beneath the p-GaN bridge near the gate, as reported by Wei et al [3].

Figures B3(a) and (b) show the gate reverse leakage and gate forward leakage characteristics of C-HEMT and PB-HEMTs, respectively. The gate reverse and forward leakage of PB-HEMTs increases compared to that of C-HEMT and increases with the number of p-GaN bridges. The higher gate leakage of the PB-HEMTs is attributed to the p-GaN bridges creating leakage current paths between the gate and the source. Since the gate Schottky junction is positively biased at

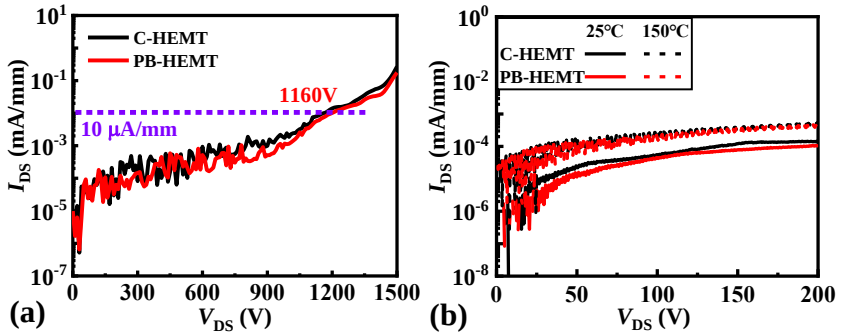

Figure B4 (a) Off-state breakdown characteristics and (b) off-state leakage characteristics 25°C and 150°C of C-HEMT and PB-HEMT with 3 bridges.

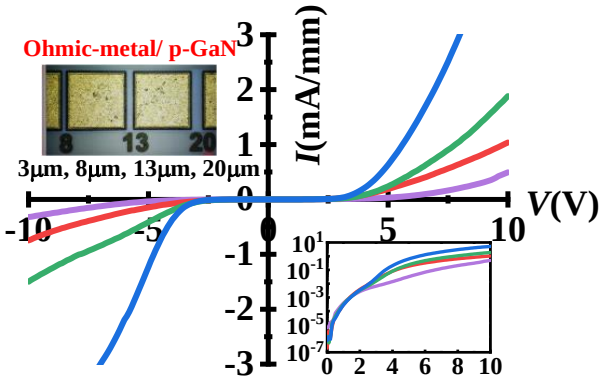

Figure C1 Transfer length method (TLM) measurement results of p-GaN/source ohmic contact characteristics.

negative gate voltages, the gate reverse leakage in PB-HEMTs becomes more pronounced. However, the channel can be fully turned off at V_{GS}= 0 V, meaning that high negative gate voltages are rarely used in practical applications. Additionally, the gate leakage current from V_{GS}= 0 V to -4 V remains below 10^{-3} mA/mm, which is considered an acceptable level. The increase in gate leakage current for C-HEMT and PB-HEMTs at 150°C is attributed to the enhanced thermionic emission and tunneling processes of holes at high temperatures. The gate forward breakdown characteristics of the C-HEMT and the PB-HEMT with three bridges at 25°C and 150°C are shown in Figure B3(c). At room temperature, the gate forward breakdown voltage of the C-HEMT is 10.7 V, whereas the PB-HEMT exhibits a slightly lower gate breakdown voltage of 10.5 V. The gate breakdown voltage of both devices increases at high temperature. This increase is attributed to the partial annihilation of hot electrons due to enhanced hole injection, which mitigates the hot electron bombardment of the Schottky junction [4]. However, since the reverse-biased Schottky junction between the gate metal and p-GaN remains intact, the gate forward leakage of the PB-HEMT is kept at a low level, and the gate breakdown voltage is not significantly reduced.

The off-state breakdown characteristics of C-HEMT and PB-HEMT with 3 bridges at V_{GS} = 0 V are illustrated in Figure B4(a). The off-state leakage current of the PB-HEMT is slightly smaller, which may be attributed to the p-GaN bridges depleting the channel more fully and thus suppressing the leakage current. However, the overall results indicate that there is no significant difference in the breakdown voltage and leakage current between the two devices. The off-state leakage of both devices at 150°C is higher compared to that at 25°C, as shown in Figure B4(b). However, the source-drain leakage current remains below 10^{-3} mA/mm under high temperature and high voltage conditions, demonstrating the excellent high-temperature performance of the PB-HEMT.

Appendix C V_{TH} increase and operation principle

Figure C1 shows the transfer length method (TLM) measurement results of p-GaN/ source ohmic metal contact characteristics. The I-V curve indicates a relatively high current, and the I-V curve in logarithmic scale shows a low reverse barrier, suggesting that the p-GaN/source metal contact forms a weak Schottky junction with high leakage ($J_{HL\text{-}SCH}$). Therefore, the p-GaN bridge is sufficient to establish a conductive path for charge transfer between the gate and source before the channel is fully turned on. Figure C2(a) shows the equivalent gate circuit of C-HEMT. The gate stack of the C-HEMT can be modelled as a p-GaN/metal Schottky junction (J_{SCH}) with a p-GaN/AlGaN/GaN PIN junction (J_{PIN}) connected back-to-back in series [5]. The source is grounded and neglecting the channel resistance between the gate and source, V_{GS} can be expressed as [6]

$$V_{GS} = V_{SCH} + V_{PIN} \tag{C1}$$

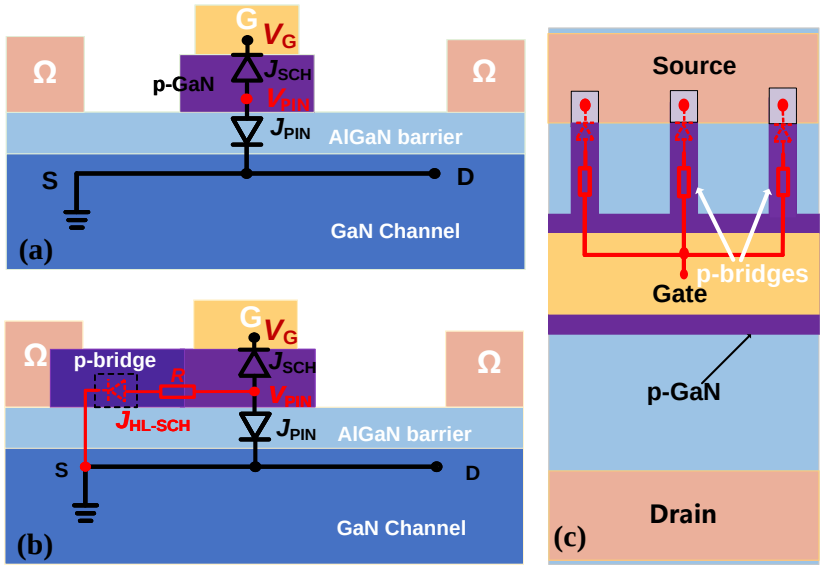

Figure C2 Equivalent gate circuits of (a) C-HEMT and (b) PB-HEMT. (c) Top view of equivalent circuit the PB-HEMT with 3 bridges.

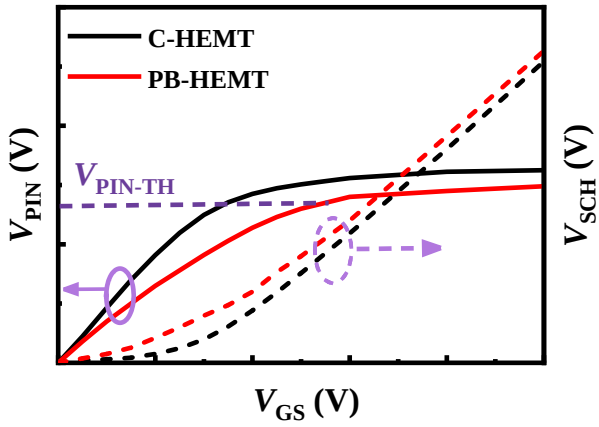

Figure C3 Simulated voltage drop across the J_{SCH} and J_{PIN} with varying V_{GS} in C-HEMT and PB-HEMT.

where V_{SCH} and V_{PIN} are the voltage drop of the J_{SCH} and drop across the J_{PIN}, respectively. The conduction of the p-GaN gate HEMT channel depends on the voltage drop across the PIN junction [7]. For the PB-HEMT, the p-GaN bridge connects the gate to the source, forming a second path (P_2) in parallel with the initial gate-source conduction path (P_1). The (P_2) consists of the resistance of the p-GaN bridge (R) and the J_{HL-SCH} formed between the p-GaN and the source metal, as shown in Figure C2(b). The p-GaN/source metal TLM results demonstrate that the (P_2) current path is available for conduction currents and transfer potentials.

As a result, the source's ground potential is conducted to the anode of the J_{PIN} diode through the P_2 path. Consequently, the V_{PIN} in the PB-HEMT is reduced compared to that in the C-HEMT. However, V_{PIN} is not directly grounded because of the partial voltage division between J_{HL-SCH} and R. The TCAD simulation is conducted to qualitatively demonstrate the forward V_{GS} distribution in the C-HEMT and PB-HEMT gate stacks, as shown in Figure C3. The V_{PIN} in the PB-HEMT is lower than in the C-HEMT, and requires a higher gate voltage to bring the V_{PIN} up to the voltage needed to open the channel (V_{PIN-TH}), which results in a higher V_{TH} for the PB-HEMT. A lower V_{PIN} in the PB-HEMT indicates a decrease in the effective gate voltage applied to the channel. The drain saturation voltage is strongly dependent on the gate voltage applied to the channel due to the pinch-off effect [8]. Therefore, the drain saturation voltage in PB-HEMT is lower, causing the drain current to prematurely saturate at a lower value. Meanwhile, the decrease in V_{PIN} also leads to an increase in V_{SCH}, which results in a larger gate leakage current in PB-HEMTs compared to that of C-HEMT. However, since the J_{SCH} is reverse-biased, the gate forward leakage of the PB-HEMT remains relatively small. When the gate is reversely biased, the J_{SCH} of the C-HEMT is positively biased, but the J_{PIN} reverse bias helps suppress gate leakage. For PB-HEMTs, the p-GaN bridges provide a leakage path between the gate and the source. Only the weak reverse-biased Schottky junction J_{HL-SCH} and the resistance R of the p-GaN bridges limit the current, which results in greater gate reverse leakage for PB-HEMTs. Increasing the number of p-GaN bridges creates more gate-source parallel paths, reducing the overall voltage drop across the p-GaN bridges and thereby decreasing V_{PIN}. Therefore, V_{TH} increases with the number of p-GaN bridges

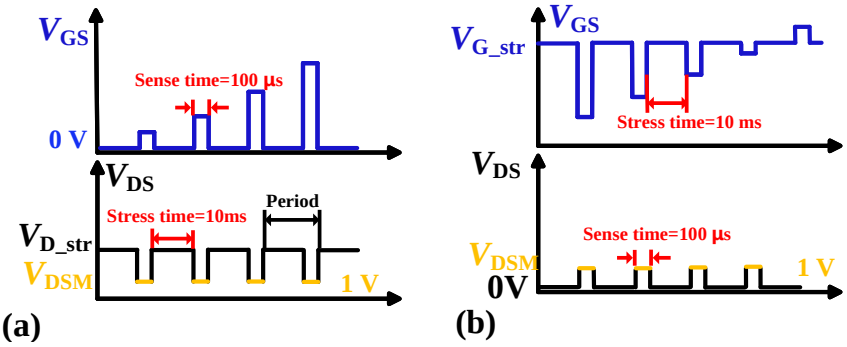

Figure D1 Schematic waveforms of dynamic I/V measurement (a) drain bias stress, (b) gate bias stress.

of the PB-HEMT.

It is important to note that the contact between the source and p-GaN is crucial. If the leakage current between the source and the p-GaN bridge is excessively large, even forming an ohmic contact, the ground potential of the source will be fully conducted to the p-GaN layer under the gate. As a result, the V_{PIN} will remain grounded regardless of the gate voltage applied, preventing the device channel from opening. Furthermore, excessive leakage current between the source and p-GaN bridges can also lead to a significant increase in both forward and reverse leakage of the gate. On the other hand, if the source/p-GaN contact is poorly characterized, the p-GaN bridge's ability to conduct potential and charge will be reduced, diminishing the PB-HEMT's advantages of increased V_{TH} and V_{TH} stability. The contact formed between the source metal (annealed Ti/Al/Ni/Au) and the p-GaN bridge exhibits an appropriately high leakage current level. This prevents the p-GaN from being fully grounded while still allowing for the effective release of stored charges, achieving an effective compromise. To verify the reliability of the process, multiple field areas on the wafer are uniformly selected for yield testing. The results demonstrate that nearly all PB-HEMTs exhibit similar V_{TH} and high V_{TH} stability. This indicates that the contact process between the source metal and p-GaN in this work is both stable and reliable. However, there remains potential for optimizing the contact characteristics between the source and p-GaN, which should be a key focus of future research.

Appendix D V_{TH} Stability under Drain/Gate Bias Stress

To fully assess the V_{TH} stability of the C-HEMT and PB-HEMT, dynamic and static stress tests have been conducted by a 4200 and Keysight B1505A semiconductor parameter analyzer.

The schematic waveform of the dynamic I/V measurement is shown in Figure D1 and consists of a stress phase and a subsequent sense phase. The transfer characteristics under drain/gate stress pulses are obtained by performing I_{DS}-V_{GS} measurements with a V_{DS} of 1 V after drain/gate has been biased for a stress time of 10 ms, with a sensing time of 100 μs. Figures D2(a) and (b) show the transfer characteristics of C-HEMT and PB-HEMT with 3 bridges under 0-40 V dynamic drain bias stress, respectively. The V_{TH} of the C-HEMT shifted severely positively with the increase of drain stress, with the maximum positive shift reaching 0.78 V. The V_{TH} of the PB-HEMT shows only a slight positive shift of 0.21 V over the entire drain bias stress range, indicating a significant improvement in the stability of V_{TH}. Figures D2(c) and (d) demonstrate the transfer characteristics of two devices under dynamic gate bias stress. The V_{TH} of the C-HEMT exhibits a slight positive shift under 1-3 V gate stress, which may be related to electron trapping in the p-GaN or AlGaN layers. However, under 4-8 V gate stress, the V_{TH} shifts negatively, with the magnitude of the negative shift increasing as the gate voltage increases. This is primarily attributed to hole accumulation at the p-GaN/AlGaN interface, which cannot be released quickly due to the charge storage mechanism [9]. The PB-HEMT exhibits only a slight positive shift in V_{TH} within the 1-8 V gate stress range, primarily attributed to the fast release mechanism of hole storage, as will be discussed in more detail later.

Figures D3(a) and (b) illustrate the variation in V_{TH} shift with the number of p-GaN bridges under dynamic drain voltage stress and gate voltage stress. Under high drain voltage stress, the V_{TH} shift decreases with the number of bridges and saturates. The improved V_{TH} stability with an increasing number of bridges can be attributed to the fact that more bridges release non-equilibrium charge (ΔQ) in p-GaN more evenly and efficiently. Under high gate stress, the V_{TH} shift is negative for 0-2 bridges, becomes positive for 3-5 bridges, and reaches a minimum at 3 bridges. This indicates that the PB-HEMT with three bridges has the best V_{TH} stability under gate stress.

The static stress test is conducted by performing a transfer characteristic test at $V_{\mathrm{DS}} = 1$ V immediately after a drain/gate bias stress of 10 s, with a switch transition time from OFF-to-ON within 1 s. Figure D4(a) shows transfer characteristics of C-HEMT measured after 10 s drain voltage stress ($V_{\mathrm{D\_str}}$). The V_{TH} of the C-HEMT is positively shifted with increasing drain voltage stress, and the V_{TH} shifts is 0.58 V at $V_{\mathrm{D\_str}}$= 400 V, which represents 35% of the initial V_{TH}. In contrast, Figure D4(b) shows that the V_{TH} shift of the PB-HEMT with 3 bridges is slightly positive, with a maximum shift of 0.19 V, which represents only 7% of the initial V_{TH}. Figures D4(c) and (d) illustrate the V_{TH} shift in C-HEMT and PB-HEMT PB-HEMT with 3 bridges under static gate voltage stress ($V_{\mathrm{G\_str}}$), respectively. C-HEMT exhibits a positive V_{TH} shift under $V_{\mathrm{G\_str}} \leqslant 5$ V and a negative shift under $V_{\mathrm{G\_str}}$>5 V, with the maximum shift ($\Delta V_{\mathrm{TH\text{-}max}}$) being 0.23 V. It is worth noting that the V_{TH} begins to shift negatively at a higher $V_{\mathrm{G\_str}}$ value compared to the dynamic test, which may result

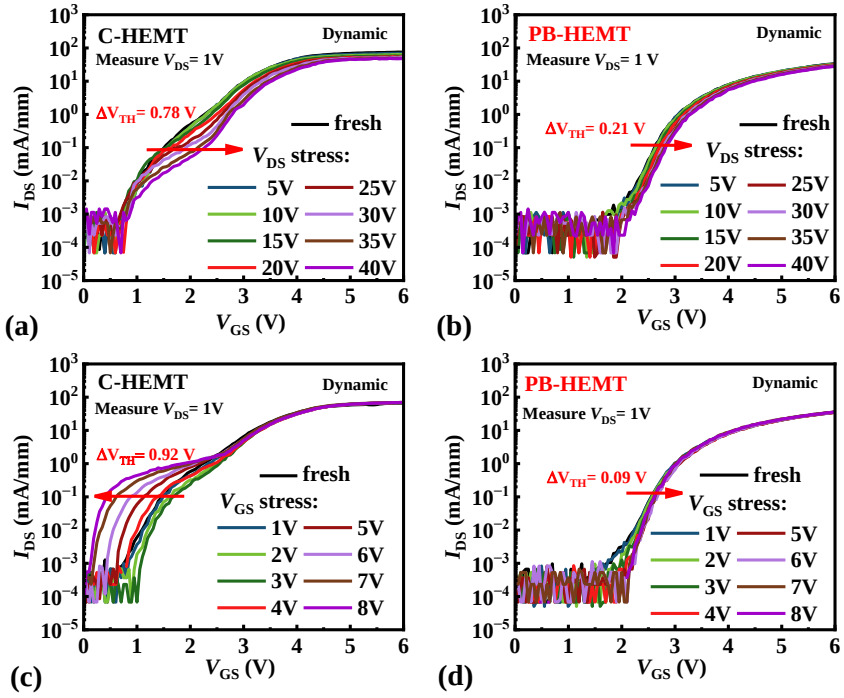

Figure D2 Transfer characteristics of (a) C-HEMT and (b) PB-HEMT with 3 bridges under dynamic drain bias stress. (c) C-HEMT and (d) PB-HEMT with 3 bridges under dynamic gate bias stress.

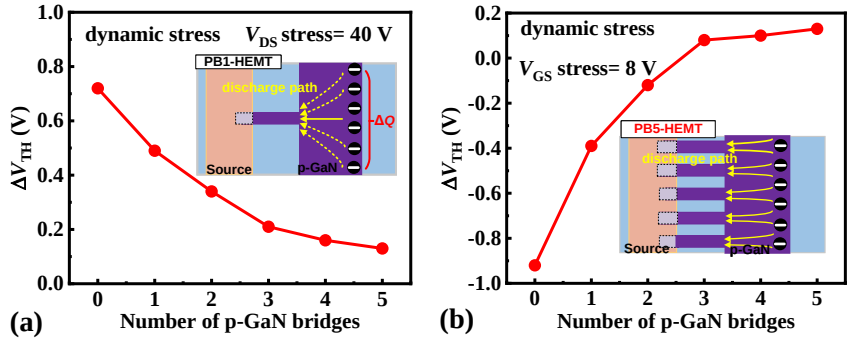

Figure D3 V_{TH} shift as a function of the number of p-GaN bridges under different stress conditions: (a) dynamic drain bias stress, (b) dynamic gate bias stress.

from a combination of mechanisms. In contrast, PB-HEMT shows a slight positive V_{TH} shift under 0-8 V gate stress, with a $\Delta V_{TH\text{-max}}$ of 0.06 V at V_{G_str} = 4 V. Figures D5(a) and (b) illustrate the variation in V_{TH} shift with the number of p-GaN bridges under high static drain voltage stress and gate voltage stress, demonstrating a similar trend to that observed under dynamic stress. The V_{TH} shift under drain bias stress decreases as the number of p-GaN bridges increases. Under gate stress, the V_{TH} shift changes from negative to positive with the increase in the number of p-GaN bridges, reaching the minimum V_{TH} shift with three bridges.

Figures D6(a) and (b) show the time-dependent V_{TH} shift of the two devices under V_{DS} = 400 V and V_{GS} = 7 V bias stress, respectively. Under long-term high drain/gate bias stress, PB-HEMT demonstrates superior V_{TH} stability than C-HEMT. Notably, V_{TH} of the PB-HEMT shifts from positive to negative as the gate stress time increases. This is attributed to the degradation of the Schottky junction under prolonged high gate voltage stress [10], leading to a significant increase in holes injected from the gate into p-GaN, with excess holes either accumulating in p-GaN or being captured by traps. Despite this, PB-HEMT can maintain a small V_{TH} shift even under high gate/drain bias stress for long periods (1000 s). Figure D6(c) shows the V_{TH} shift for both devices at 25°C and 150°C under long-term drain voltage stress of 200 V. Notably, the V_{TH} shifts of both devices at high temperature are reduced compared to room temperature. The decrease in V_{TH} shift is attributed to the increased Schottky junction leakage at high temperatures, which causes a greater release of the stored charge in the floating p-GaN through the gate, similar to an ohmic p-GaN gate. Additionally, high temperature cause electrons and holes to gain higher energy, which accelerates the release of non-equilibrium charges in the p-GaN, driving it toward equilibrium. Overall, PB-HEMT maintains robust V_{TH} stability under various stress conditions, highlighting its significant potential for power applications.

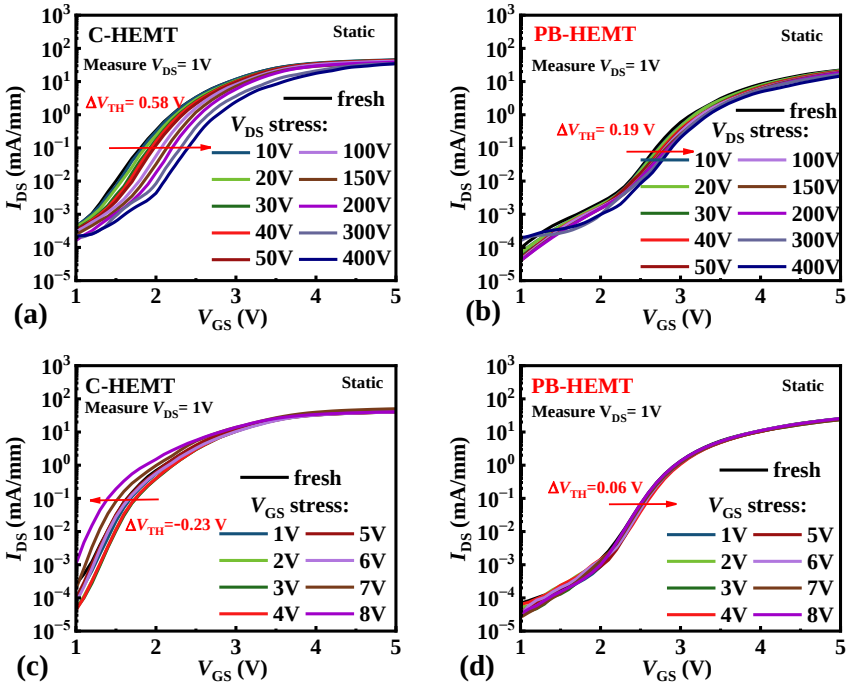

Figure D4 Transfer characteristics of (a) C-HEMT and (b) PB-HEMT with 3 bridges under static drain bias stress, and (c) C-HEMT and (d) PB-HEMT with 3 bridges under static gate bias stress.

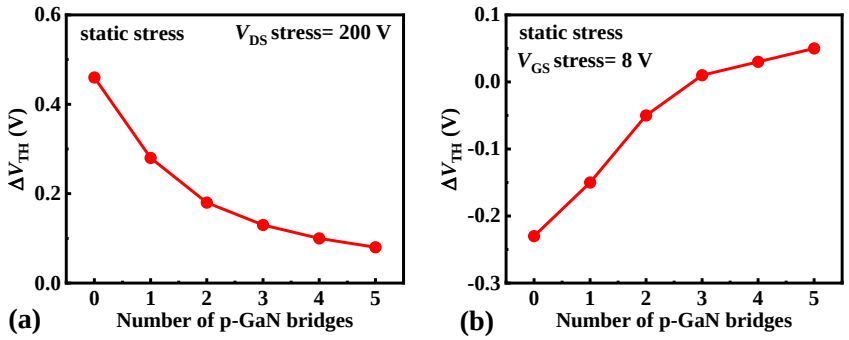

Figure D5 V_{TH} shift as a function of the number of p-GaN bridges under different stress conditions: (a) static drain bias stress, (b) static gate bias stress.

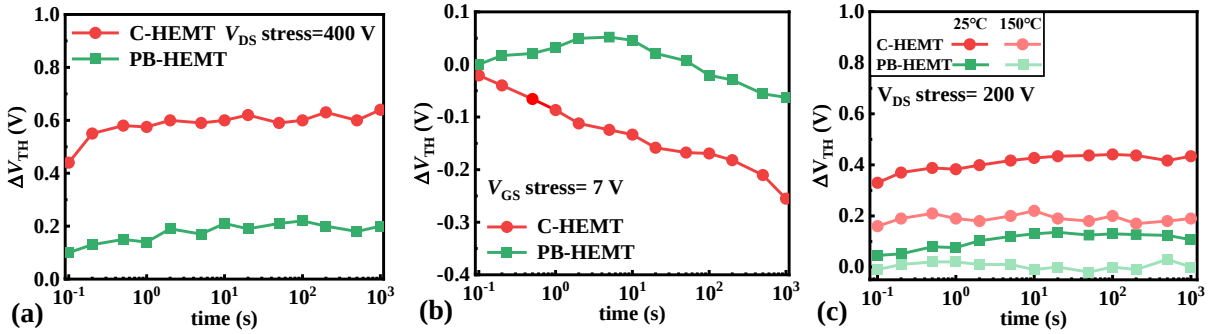

Figure D6 V_{TH} shifts of C-HEMT and PB-HEMT with 3 bridges under long-term static stress: (a) V_{DS}= 400 V, (b) V_{GS}= 7 V, and (c) V_{DS}= 200 V at 25℃ and 150℃.

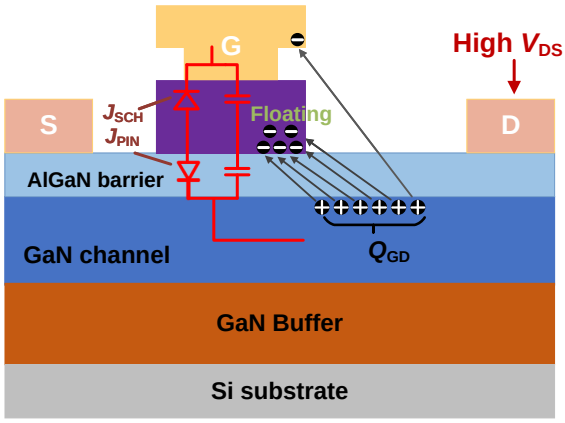

Figure E1 Gate-to-drain charge distribution under high drain voltage stress and simplified gate stack equivalent circuit.

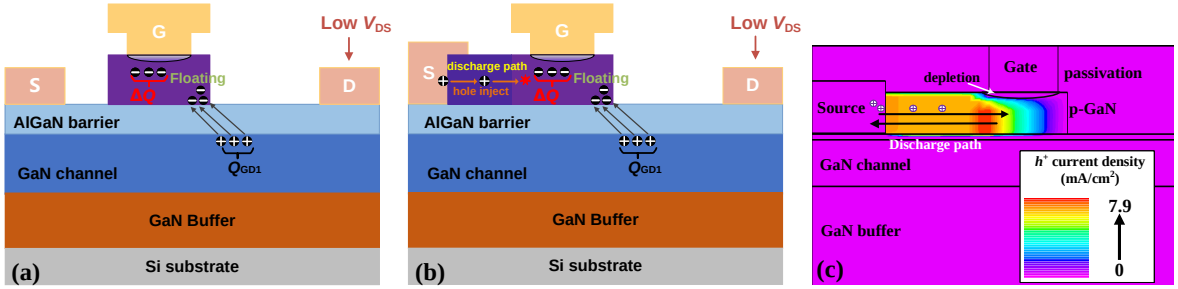

Figure E2 Gate-to-drain charge distribution of (a) C-HEMT and (b) PB-HEMT under low drain voltage. (c) Simulated hole current density in the p-GaN bridge and p-GaN layer at V_{GS}=1 V.

Appendix E Mechanisms of V_{TH} stability

The p-GaN layer is sandwiched between two junctions (J_{SCH} and J_{PIN}), creating a "floating region" [9]. In the off state (V_{GS} = 0), when a high drain voltage stress is applied to p-GaN gate HEMT, the channel electrons between the gate and drain are depleted, resulting in the accumulation of ionized positive fixed charge. As shown in Figure E1, the J_{PIN} is reverse-biased and junction capacitor (C_{PIN}) is charged to Q_{GD}. The positive charge is provided by the fixed charge in the channel depletion region, while the negative charge primarily comes from ionized Mg acceptor in the p-GaN. This charge distribution results from the forward bias of the metal/p-GaN Schottky junction, which causes holes to flow from the p-GaN to the gate metal, leaving behind negatively charged fixed charges. When the C-HEMT swicthes from the off-state to the on-state, the drain voltage drops from high to low and the gate becomes forward-biased. The C_{PIN} discharges, reducing the fixed positive charge (Q_{GD}) in the channel to (Q_{GD1}), as shown in Figure E2(a). Consequently, the negative charge in the p-GaN is also expected to decrease. However, the forward bias of the gate reverse-biases J_{SCH}, blocking the flow of holes into the p-GaN layer. Therefore, the extra negative charges (ΔQ) in p-GaN cannot be released, resulting in V_{TH} positively shifts in C-HEMT shown in Figure D4(a). For PB-HEMT, the p-GaN bridges connect the floating p-GaN layer beneath gate to the source, provide discharge path for negative charge (ΔQ), as shown in Figure E2(b). When the drain voltage transitions from high stress to a lower value, the source rapidly injects holes into the floating p-GaN layer through the multiple p-GaN bridges. These holes recombine with the fixed negative charges in the floating p-GaN layer, reducing the amount of stored negative charge. Therefore, the positive shift of V_{TH} caused by high drain stress is weakened, thereby enhancing the stability of V_{TH}. Figure E2(c) shows the simulated hole current density at V_{GS} = 1 V, demonstrating that the p-GaN bridge efficiently transfers charge between the source and the p-GaN layer.

The V_{TH} shift mechanism under gate bias stress is more complex, including electron/hole trapping as well as charge storage effect. Figure E3 shows schematic band diagram of the p-GaN gate HEMT under the gate region at the gate stress phase. Under low gate voltage stress, the V_{TH} shift is dominated by three main factors: (i) The metal/p-GaN Schottky junction becomes reverse-biased, and the p-GaN depletion region is flooded with negatively charged acceptor ions that cannot be released rapidly during the switching phase. (ii) The J_{PIN} is forward biased, leading to electron spill over the AlGaN layer, where some electrons recombine with holes in the undepleted p-GaN layer [10].(iii) The overflowing electrons are captured by existing electron traps in the AlGaN layer or the depleted p-GaN, which may originate from Mg diffusion or the E2 deep level trap widely reported [11]. And at this condition, the Schottky barrier has a relatively large thickness, so the hole injection from the gate to the p-GaN layer is weak. As a result, the extral negative charge stored or trapped in the p-GaN or AlGaN layer dominates, causing a positive V_{TH} shift. Under high gate voltage stress, the band bending of

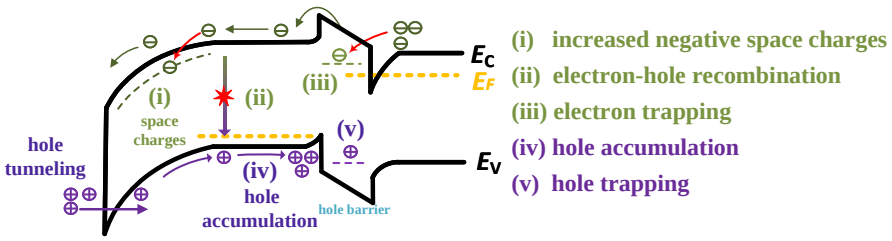

Figure E3 Schematic band diagram of the p-GaN gate HEMT under the gate region under gate bias stress.

p-GaN increases, significantly reducing the Schottky barrier thickness and enhancing hole tunneling from gate to p-GaN. Some holes recombine with electrons that overflow from the channel, while most holes accumulate at the p-GaN/AlGaN interface due to the AlGaN hole barrier (iv) or are captured by hole traps in AlGaN (v). This dominant hole injection leads to positive charge accumulation in p-GaN, resulting in a negative V_{TH} shift. The V_{TH} begins to shift negatively at a higher $V_{\mathrm{G\_str}}$ value in the static test compared to the dynamic test, primarily due to the rapid accumulation and release of holes. The switching time of the static measurement is much longer, and the holes that have been stored are partially released during the measurement, which results in the dominance of the V_{TH} positive shift caused by the trapping or accumulation of electrons in the p-GaN layer under low gate bias stress.

For PB-HEMT, the V_{TH} shows only a slight positive shift under gate stress. Under low gate stress conditions, holes quickly replenish the negative charge in the Schottky depletion region through the p-GaN bridge and recombine with electrons injected from the channel, effectively suppressing the positive V_{TH} shift induced by behaviors (i) and (ii) observed in C-HEMT. Under higher gate stress, the accumulated extra holes are released through the p-GaN bridge under high gate voltage, preventing a negative V_{TH} shift caused by behavior (iv). The observed slight positive shift in V_{TH} is primarily due to the capture of electrons by deep energy level traps in the p-GaN or AlGaN layers, which are not quickly released through the p-GaN bridges. With a small number of bridges, the release of accumulated holes is limited, and the accumulation of positive charge in p-GaN leads to a negative shift in V_{TH}. However, an increase in the number of bridges (4 and 5) leads to the release of an excessive number of holes, which causes the capture and accumulation of electrons in p-GaN to become dominant. The dominance of negative charge in p-GaN results in a positive shift in V_{TH}. Therefore, PB-HEMT with three bridges achieves an optimal balance of positive and negative charges in p-GaN, resulting in the best V_{TH} stability under high gate voltage stress as shown in Figures D3(b) and D5(b).

The number of p-GaN bridges significantly affects the performance and reliability of PB-HEMTs. A trade-off exists between high V_{TH} and V_{TH} reliability, as well as low on-resistance and gate leakage. Based on a comprehensive comparison, the device with three p-GaN bridges demonstrates the most balanced performance. The number of bridges can also be selected based on the requirements for V_{TH} and other performance metrics in the practical application.

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