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An H-band sliding-IF transmitter and receiver chipset in 130-nm SiGe BiCMOS

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The H-band (220–320 GHz) is a crucial potential frequency spectrum for next-generation 6G wireless communications, supporting applications such as ultra-high-speed short-range links and wireless backhaul [1, 2]. While silicon-based processes like SiGe BiCMOS offer high integration density, designing high-performance circuits as the operating frequency approaches the transistor's cutoff frequency (f_T/f_{max}) presents significant challenges. Specifically, achieving high performance in transmitters (Tx) and receivers (Rx) is constrained by lots of issues, such as limited power gain, pronounced parasitic effects, and inaccuracies in process design kits (PDKs) [3].

To address these challenges, we propose an H-band sliding-IF phase-shifting architecture. By effectively reducing the operating frequency of critical components such as mixers, phase shifters, and LO chains while maintaining a high level of integration, this architecture mitigates circuit-level limitations and enhances overall system performance. We present a chipset fabricated in 130-nm SiGe BiCMOS (f_T/f_{max} = 350/450 GHz), featuring a high-power PA-last Tx and a wideband LNA-first Rx with advanced circuit techniques.

System architecture. The transceiver plans to cover the 240–300 GHz band using a sliding-IF architecture in Figure 1(a), which optimally distributes the frequency conversion burden. The RF frequency f_{RF} is related to the input LO frequency f_{LO} by

$$f_{RF} = M(N+1)f_{LO}. \quad (1)$$

By selecting multiplication factors $M = 4$ (quadrupler) and $N = 2$ (doubler), the input LO (20–25 GHz) generates the first IF (80–100 GHz) and the second LO (160–200 GHz). The chips consist of a two-stage LO chain, two-stage up/down-conversion mixers, a phase shifter, a power amplifier, and a low-noise amplifier.

This architecture offers three primary advantages. First, it enables phase shifting in the IF domain (80–100 GHz). Compared to RF phase shifting, the IF approach significantly reduces insertion loss, preserving the link budget; compared to LO phase shifting, it offers superior phase precision by avoiding the multiplication of phase errors. Second, the two-stage conversion naturally separates the RF and LO frequencies, significantly improving LO-RF isolation and achieving a high RF frequency. It inherits the benefits of the heterodyne approach while requiring only a single LO, thereby improving system compactness. Third, it can realize excellent image and LO rejection simultaneously.

Key building blocks. **LNA:** The receiver adopts a single-to-differential five-stage LNA architecture to combine the low-noise advantage of single-ended input stages with the high linearity of differential downstream stages in Figure 1(b).

Conventional passive baluns at THz frequencies suffer from high insertion loss, directly degrading the receiver's noise figure and gain. Traditional active baluns also cannot offer high gain in this high frequency. To address these issues, our proposed active balun incorporates two key techniques. First, this design incorporates an inductive (L_{BB}) gain-boosting technique and a cascode configuration. Resistors (R_{BB}) and capacitors (C_{BB}) are added at the (L_{BB}) port to improve circuit stability. Second, to rigorously correct the inherent transconductance disparity between the common-base (CB) and common-emitter (CE) paths, the base bias voltages are independently fine-tuned to V_{B_CB} = 0.94 V and V_{B_CE} = 0.87 V. This precise biasing ensures amplitude balance is maintained over a wide bandwidth. Consequently, this balun in LNA's third stage performs robust single-to-differential conversion with inherent noise cancellation and high gain, effectively driving the subsequent differential stages.

PA: As the last stage of the transmitter chain, the H-band PA further amplifies the output signal from the preceding up-conversion mixer. To enhance the output capability of the PA, a modified three-conductor balun is employed at the output stage [4]. Unlike conventional three-conductor baluns, this structure utilizes physically isolated coupled lines, eliminating DC-blocking capacitors and their associated losses. The network constitutes a higher-order resonant network, achieving broadband impedance matching and wideband power combining.

The PA adopts a five-stage four-way architecture, as illustrated in Figure 1(c). It also uses the inductive gain-boosting cascode technology in the core of the PA [5]. The input and inter-stage matching network employs transmission lines and transformers.

Mixers, LO chains and phase shifter: As shown in Figure 1(d), a double-balanced quadrature mixer topology is adopted to enhance the isolation among LO, IF, and RF ports, further mitigating image signal generation. The second-stage up-conversion mixer in Tx and the first-stage down-conversion mixer in Rx per-

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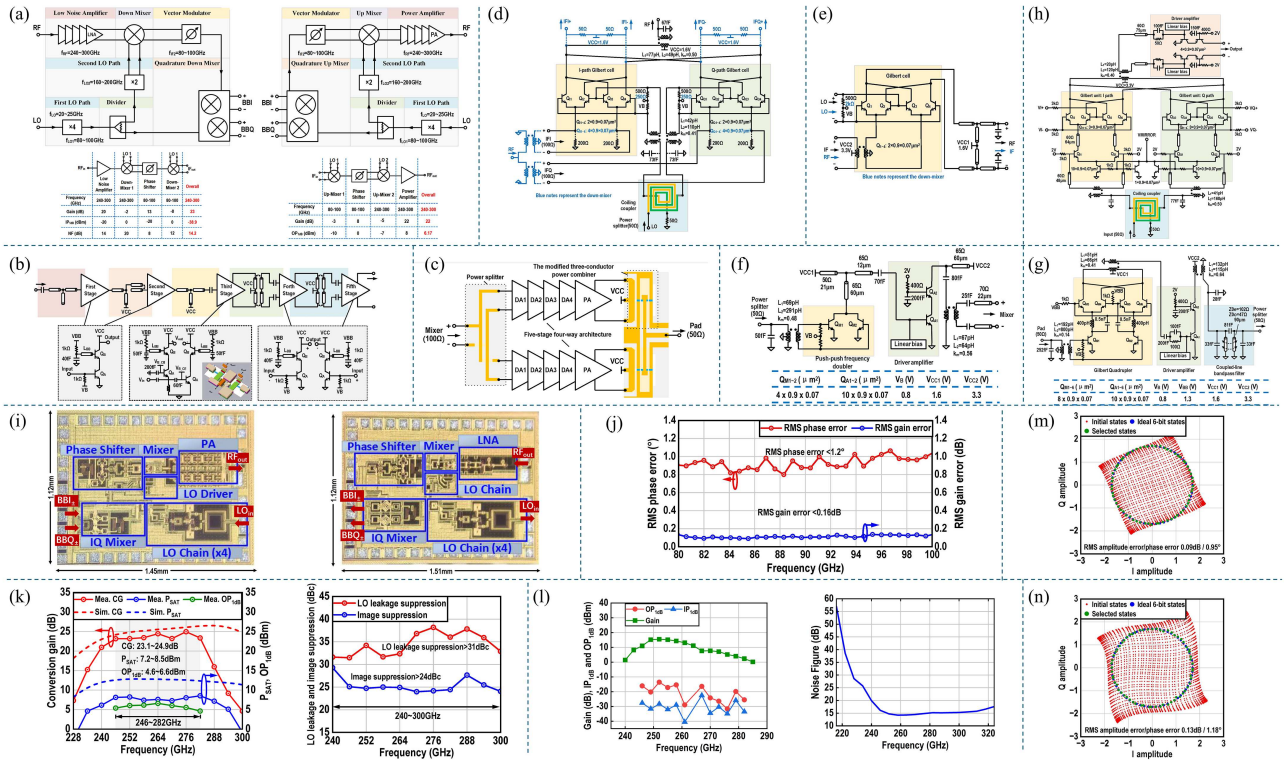

Figure 1 (Color online) (a) Link budgets of Tx and Rx; the architectures of (b) LNA and (c) PA; (d) IQ up/down-conversion mixer; (e) up/down-conversion mixer without IQ; (f) the second stage of LO chain; (g) the first stage of LO chain; (h) vector modulator PS; (i) Tx and Rx chip photos; (j) RMS phase and gain errors in PS; (k) simulated and measured results of Tx; (l) simulated and measured results of Rx; (m) phase-shifting state results in 80 GHz; (n) phase-shifting state results in 100 GHz.

form frequency conversion between the 80–100 GHz IF and the RF bands in Figure 1(e). These mixers adopt a non-quadrature configuration to reduce circuit size and power consumption.

As shown in Figure 1(g), the first-stage LO chain comprises a frequency quadrupler, a driver amplifier, and a bandpass filter. The second-stage LO chain (Figure 1(f)) employs a push-push frequency doubler followed by a driver amplifier. The phase shifter is implemented as a vector modulator in the IF band (80–100 GHz). Each I/Q path is implemented using a Gilbert-cell topology, followed by a driver amplifier to enhance the overall gain and output power of the phase shifter.

Measurement results. The chipset was fabricated in a 130-nm SiGe BiCMOS process. The Tx and Rx occupy 1.45 mm × 1.12 mm and 1.51 mm × 1.12 mm, respectively.

As shown in Figure 1(k), the Tx chip achieves a flat conversion gain of 23.1–24.9 dB, a saturated output power of 7.2–8.5 dBm, and an $OP_{1\mathrm{dB}}$ of 4.6–6.6 dBm across a broad RF range of 246–282 GHz. the measured power-added efficiency (PAE) ranges from 0.61% to 0.83%, with a total DC power consumption below 0.9 W. LO and image rejection exceed 31 dBc and 24 dBc, respectively.

In Figure 1(l), the Rx achieves a peak CG of 15.5 dB with a 3-dB bandwidth of 248–258 GHz. The maximum $OP_{1\mathrm{dB}}$ and $IP_{1\mathrm{dB}}$ are measured as −13.6 dBm and −22.5 dBm, respectively. Due to the limitation of measurement equipment, we only show the simulated noise figure. It achieves the best noise figure of 14.2 dB.

The standalone phase shifter verifies beamforming capability. In Figures 1(j), (m), and (n), across 80–100 GHz (corresponding to 240–300 GHz RF), the RMS gain error is <0.16 dB and the RMS phase error is <1.2°, enabling 6-bit resolution.

Conclusion. A broadband H-band phased-array transceiver chipset is demonstrated. Leveraging a sliding-IF architecture and innovative circuit designs such as broadband PA implementation and a gain-boosting cascode active balun in a five-stage LNA, the TRx exhibits excellent output power, bandwidth, linearity, and phase control performance. The results validate the proposed solution for future silicon-based THz phased-array systems.

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