SCIENCE CHINA
Information Sciences

• LETTER •

March 2026, Vol. 69, Iss. 3, 139404:1–139404:2
https://doi.org/10.1007/s11432-025-4628-9

A 67 dB-SNDR 1.6 GS/s fully passive SAR-assisted noise-shaping pipelined ADC with gain error shaping

Zhangming ZHU, Xianghui ZHANG & Yanbo ZHANG*

Key Laboratory of Analog Integrated Circuits and Systems, Ministry of Education, School of Integrated Circuits, Xidian University, Xi'an 710071, China

Received 23 May 2025/Revised 12 October 2025/Accepted 15 October 2025/Published online 22 January 2026

Citation Zhu Z M, Zhang X H, Zhang Y B. A 67 dB-SNDR 1.6 GS/s fully passive SAR-assisted noise-shaping pipelined ADC with gain error shaping. Sci China Inf Sci, 2026, 69(3): 139404, https://doi.org/10.1007/s11432-025-4628-9

The noise-shaping (NS) successive approximation register (SAR) analog-to-digital converter (ADC) achieves low power consumption and high resolution, but the bandwidth (BW) is limited by the serial operations. Hybridizing the pipeline with NS-SAR (NS-PiSAR) can extend the BW through parallel conversion, but the gain of the residue amplifier (RA) is critical. Gain error shaping (GES) is an effective method to address this issue [1]. Meanwhile, as shown in Figure 1(a), active residue transfer consumes amplification time, thereby limiting the BW to 40 MHz. In contrast, the passive residue transfer eliminates the amplification time, further enhancing the BW [2]. However, the charge-sharing method has a gain loss and requires a different reference voltage or additional attenuation capacitors to align with the quantization range. A potential solution to compensate for this gain loss is to use a multi-input comparator with a relative gain [3]. Nevertheless, digital calibration is still required to correct the fixed gain error caused by mismatches among input pairs. Moreover, the dynamic gain errors caused by variations of the transconductance (g_m) ratio due to different input amplitudes are challenging to correct, limiting the signal-to-noise and distortion ratio (SNDR) below 50 dB.

To address the issues above, this work presents a fully passive 1-0 multi-stage noise shaping (MASH) PiSAR ADC with GES, as illustrated in Figure 1(a). Both the residue transfer and NS are realized through the same passive operation, which inherently features low power consumption, high speed, and insensitivity to process, voltage, and temperature (PVT) variation. The MASH architecture is effective in shaping quantization noise and interstage gain errors, including dynamic and fixed gain errors. As a result, the gain loss that occurs during passive residue transfer can be efficiently compensated by a relative gain from a multi-input comparator without gain error calibration. Fabricated in a 28-nm CMOS process, the ADC prototype exhibits an SNDR of 67.6 dB and a BW of 100 MHz with an oversampling ratio (OSR) of 8. It consumes only 4.15 mW power under a 0.9-V supply, yielding an outstanding Schreier figure-of-merit (FoM$_s$) of 171.42 dB.

The gain error in multi-input comparator. Figure 1(a) shows the block diagrams of the proposed passive 1-0 MASH PiSAR ADC, which achieves an equivalent interstage gain G_{eq} consisting of the gain loss from charge sharing and relative gain from comparators. Thanks to the ratio-metric nature, the relative gain achieved from a g_m ratio (20:1) offers a robust amplification across PVT variation. However, the mismatch between the input pairs results in a fixed gain error. On the other hand, since the pre-amplifier of the dynamic comparator operates in open-loop integration mode, the relative gain varies with the gate voltage of the pre-amplifier. As depicted in Figure 1(b), both the 20× and 1× input pairs experience a large voltage variation at the gate, which results in a total 2.6% dynamic variation in the relative gain G_{20}/G_1. Therefore, the multi-input comparator-based NS-PiSAR ADC suffers from fixed and dynamic gain errors (Δ), resulting in noise leakage represented as $\Delta Q_1(z)$. Worse, since the gate voltage changes in each conversion cycle, extracting and calibrating the gain error becomes challenging.

Proposed 1-0 MASH PiSAR with gain error shaping. Thanks to the feedforward (FF)-NS SAR ADC introduced in the 1st stage as shown in Figure 1(a), the fixed and dynamic gain error caused by the multi-input comparator will be both shaped in the proposed 1-0 MASH PiSAR ADC. The transfer function indicates that the gain error and quantization noise are shaped by the 1st-stage NS, thereby reducing the sensitivity to gain variation and eliminating the need for calibration. To maintain the benefits of passive residue transfer, a passive integration scheme is implemented to achieve FF NS. Different from the previous mild passive shaping effect [4], the proposed passive NS strategically sets the zero at 0.8 to shape the gain error more effectively, forming an NTF of $1-0.8z^{-1}$. Figure 1(c) plots the NTF magnitude of the proposed work and compares it with that of the ideal 1st-order NS and the work [4]. It shows that the proposed work provides 4.4 dB more noise attenuation than [4]. To illustrate the GES capability, Figure 1(d) shows the simulation results of signal-to-quantization-noise ratio (SQNR) under conditions with and without GES. Given a 73 dB SQNR as the baseline, the 1-0 MASH structure extends the tolerable gain error range by 6-fold, which highlights the effectiveness of the proposed ADC in shaping the gain error.

Circuit implementation. The overall architecture and timing diagram of the proposed ADC are depicted in Figure 1(e). The ADC consists of a 4-bit NS SAR ADC in the 1st stage and a 6-bit SAR ADC in the 2nd stage, along with a 1-bit redundancy. The coarse-fine architecture is used in the 1st-stage SAR ADC to enhance conversion speed. At ϕ_S, the differential inputs are sam-

* Corresponding author (email: zhybor@163.com)

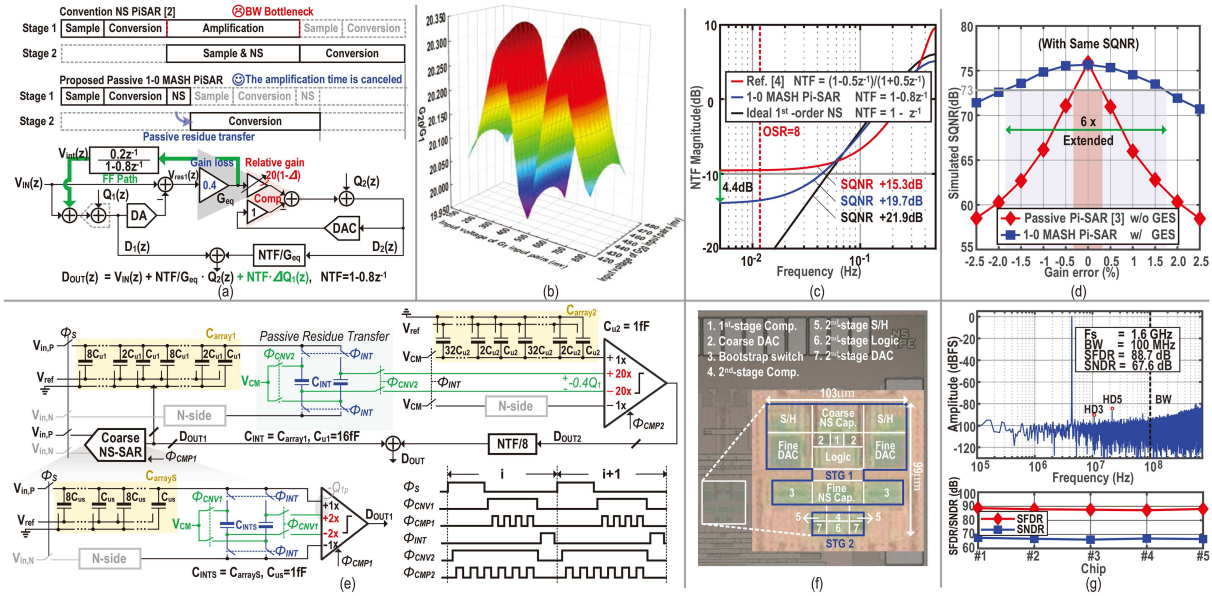

Figure 1 (Color online) (a) The operation timing and block diagrams of the proposed 1-0 MASH Pi-SAR ADC; (b) equivalent gain versus input amplitude; (c) NTF plot and comparison; (d) simulated SNDR varies with the gain error between two architectures; (e) the overall architecture and timing diagram of the proposed ADC; (f) die photograph; (g) measured FFT spectrum of chip #1 and measured SNDR and SFDR of 5 chips.

pled by the fine DAC (C_{array1}) and coarse DAC (C_{arrayS}). The coarse NS-SAR ADC gives a 4b decision to the C_{array1} to generate the residue voltage after ϕ_{CMP1}. Then, during ϕ_{INT}, the residue voltage (V_{res1}) from the 1st-stage fine SAR is passively integrated on C_{INT} in a differential way, obtaining a passive gain of 2×. The voltage hold on C_{INT} is expressed as $V_{int} = V_{res1} \cdot 0.4z^{-1}/(1-0.8z^{-1}) = -0.4Q_1$. It can be seen that the same charge-sharing process not only completes passive integration but also creates the quantization-like error ($-0.4Q_1$) simultaneously. The V_{int} is directly sent to the 2nd-stage multi-input comparator to finish the passive residue transfer. To compensate for the 0.4-fold attenuation and achieve an interstage gain of 8, the 2nd-stage comparator is designed with a gain ratio of 1:20 between the reference input and the residue input. The coarse and fine ADCs are required to perform the same NS operation for proper residue generation. Therefore, the C_{INTS} directly performs charge sharing with C_{arrayS} in a differential fashion. The voltage hold on C_{INTS} is then relatively 2× amplified by the two-input comparator, resulting in the same NTF of $1-0.8z^{-1}$. During ϕ_{INT}, the reference DAC (C_{array2}) is reset to V_{CM} at the same time. Then, the 2nd-stage SAR ADC performs SAR conversion together with C_{INT} at ϕ_{CNV2}. The 1st-stage and 2nd-stage SAR ADCs use the same full-swing reference voltage to reduce design complexity. The total capacitance of C_{arrayS}, C_{array1}, and C_{array2} is 32, 512, and 64 fF, respectively.

Measurement results. Figure 1(f) displays the micrograph, and the active area is about 0.01 mm^2. Operating at 1.6 GS/s, the total power consumption is 4.15 mW under a 0.9-V supply. The power consumption proportions for digital, analog, reference, and NS operations are 32%, 19%, 28%, and 21%, respectively. Figure 1(g) shows the FFT result with an input frequency close to 4.37 MHz. The bit weight mismatch from the DAC is calibrated in the digital domain [5]. The measured SNDR and spurious-free dynamic range (SFDR) are 67.6 and 88.7 dB over a BW of 100 MHz, respectively. Furthermore, the proposed ADC achieves the highest BW among other single-channel NS-SAR and per-channel TINS-SAR ADCs, with an increase of 60 MHz in BW and 3.55 dB in SNDR compared with the fastest single-channel NS-SAR ADC [4].

Acknowledgements This work was supported by National Key R&D Program of China (Grant No. 2023YFB4405002), National Natural Science Foundation of China (Grant Nos. 62574155, 62361166671), and Fundamental Research Funds for the Central Universities (Grant No. YJSJ25013).

References

1 Hsu C K, Tang X, Liu J, et al. A 77.1-dB-SNDR 6.25-MHz-BW pipeline SAR ADC with enhanced interstage gain error shaping and quantization noise shaping. IEEE J Solid-State Circuits, 2021, 56: 739–749
2 Huang H, Du L, Chiu Y. A 1.2-GS/s 8-bit two-step SAR ADC in 65-nm CMOS with passive residue transfer. IEEE J Solid-State Circuits, 2017, 52: 1551–1562
3 Shen Y, Hao J, Liu S, et al. An 8-bit 1.5-GS/s two-step SAR ADC with embedded interstage gain. IEEE Trans VLSI Syst, 2023, 31: 1870–1873
4 Lin Y-Z, Lin C-Y, Tsou S-C, et al. 20.2 A 40MHz-BW 320MS/s passive noise-shaping SAR ADC with passive signal-residue summation in 14nm FinFET. In: Proceedings IEEE International Solid-State Circuits Conference, 2019. 330–332
5 Catteau B, Rombouts P, Raman J, et al. An on-line calibration technique for mismatch errors in high-speed DACs. IEEE Trans Circuits Syst I, 2008, 55: 1873–1883