SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

March 2026, Vol. 69, Iss. 3, 132403:1–132403:8
https://doi.org/10.1007/s11432-025-4572-5

High ON/OFF and high FoM of $f_{\max}\times BV\times L_g$ InAlN/GaN HEMTs by using polycrystalline-AlN cap

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Received 15 March 2025/Revised 27 June 2025/Accepted 27 August 2025/Published online 14 January 2026

Abstract In this paper, we demonstrate the excellent performance of InAlN/GaN high electron mobility transistors (HEMTs) for high-voltage radio frequency (RF) application. By using a composite cap layer structure of GaN cap layer and polycrystalline (PC)-AlN cap layer, the gate leakage is effectively suppressed, resulting in a 0.5-μm InAlN/GaN HEMTs achieving a high current on/off ratio (ON/OFF) of 7×10^7 as well as a record breakdown voltage (BV) of 270 V. The device yields a high peak transconductance (G_m) of 350 mS/mm and a low sub-threshold swing (SS) of 80 mV/decade while virtually free of drain induced barrier lowering (DIBL) effect (about 2.5 mV/V). Besides, the InAlN/GaN HEMTs with composite cap layer structure exhibit a current gain cut-off frequency/ maximum oscillation frequency ($f_T/f_{\max}$) of 22/64 GHz. To the best of our knowledge, the device has the highest figure-of-merit (FoM = $f_{\max}\times BV\times L_g$) of 8.6 THz·V·μm compared to the InAlN/GaN HEMTs reported in the past. These results demonstrate that the design of the composite cap layer structure extends the RF InAlN/GaN HEMTs for high voltage applications.

Keywords InAlN/GaN, high-electron-mobility transistors, cap layer, breakdown voltage, radio frequency

Citation Li S M, Lu H, Yang L, et al. High ON/OFF and high FoM of $f_{\max}\times BV\times L_g$ InAlN/GaN HEMTs by using polycrystalline-AlN cap. Sci China Inf Sci, 2026, 69(3): 132403, https://doi.org/10.1007/s11432-025-4572-5

1 Introduction

With the rapid spread of 5G/6G communication technologies and the increased demand for high-resolution detection in radar systems, the performance requirements for high-frequency and high-power radio frequency (RF) devices are becoming increasingly stringent [1,2]. Traditional silicon-based devices are limited by material properties (e.g., low electron saturation velocity, low breakdown electric field), making it difficult to meet the dual requirements of high frequency and high power [3,4]. Gallium nitride (GaN)-based heterojunctions, on the other hand, with their high two-dimensional electron gas (2DEG) density ($>1\times10^{13}$ cm^{-2}), high breakdown electric field (>3 MV/cm), and high electron saturation velocity ($>2.5\times10^7$ cm/s), have made their based high-electron-mobility transistors (HEMTs) the most popular choice for 5G base station power amplifiers, satellite communication terminals and phased-array radars, and other scenarios [5–9].

Among them, InAlN/GaN HEMTs have attracted much attention due to a multitude of advantages [10,11]. On the one hand, InAlN and GaN can be lattice-matched, which enables InAlN/GaN HEMTs to exhibit excellent thermal stability and reliability [12,13]. On the other hand, a thin InAlN barrier layer (below 10 nm) alone has strong spontaneous polarization leading to a high 2DEG density in the InAlN/GaN heterojunction, which is conducive to enhancing the current density and output power of GaN-based HEMTs [14,15]. In addition, the thinner barrier layer means that the operating frequency of GaN-based HEMTs can be expanded by scaling down the gate length (L_g) while avoiding the short-channel effect [16]. There is a plethora of outstanding work on high-frequency InAlN/GaN reports. On the SiC substrate without a back-barrier structure, the 30-nm InAlN/GaN HEMTs achieved the highest current gain cut-off frequency (f_T) of 400 GHz with a maximum oscillation frequency ($f_{\max}$) of 40 GHz [17]. The 55-nm InAlN/GaN HEMTs on the Si substrate achieved a balanced $f_T/f_{\max}$ of 205/220 GHz through source-drain regrowth technique [18]. Although great progress has been made in high frequency by scaling down L_g of the InAlN/GaN HEMTs, this has led to a non-negligible problem of increasingly high off-state

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gate leakage in the device [19]. This can negatively impact the device performance, such as current on/off ratio (ON/OFF), sub-threshold swing (SS), power added efficiency (PAE), and noise figure [20–23].

There are many schemes such as cap layer structures, back barrier structures, and gate-recess etch that have been reported to reduce the off-state leakage current in InAlN/GaN HEMTs [24, 25]. These methods involve distinct design trade-offs, which are critical for practical implementation. Back barrier structures suppress leakage by confining carriers within the channel, but their high polarization mismatch with GaN buffer layers often degrades vertical heat dissipation. This thermal limitation can lead to device overheating under high-power operation, threatening long-term reliability [26]. Gate-recess etch enhances gate control by reducing the distance between the gate and channel, but the plasma or chemical etching process inevitably introduces interfacial damage, which may increase trap density and degrade subthreshold characteristics [27]. Cap layer structures are particularly suitable for InAlN/GaN HEMTs due to the inherent indium segregation in InAlN barrier layers, which causes surface roughening and leakage. A well-designed cap layer can both block indium diffusion and smooth the InAlN surface, thereby minimizing leakage without introducing significant thermal or interfacial penalties [28, 29]. Given these considerations, cap layer structure design emerges as an effective and fabrication-friendly approach to reduce off-state leakage in InAlN/GaN HEMTs.

In this study, we proposed a novel composite cap layer structure formed by GaN cap layer and polycrystalline (PC)-AlN cap layer for suppressing the off-state leakage phenomenon of the InAlN/GaN HEMTs. The InAlN/GaN HEMTs with composite cap layer structure with a L_g of 0.5 μm achieved a high ON/OFF of 7×10^7, low reverse gate leakage current (below 0.3 μA/mm), and a record breakdown voltage (BV) of 270 V. Additionally, the InAlN/GaN HEMT with excellent gate control achieved a peak transconductance (G_m) of more than 350 mS/mm with a low drain induced barrier lowering (DIBL) of 2.5 mV/V. Besides, the InAlN/GaN HEMTs obtained a $f_T/f_{\max}$ of 22/64 GHz and the highest figure-of-merit (FoM = $f_{\max} \times$ BV $\times$ L_g) of 8.6 THz·V·μm among present literature reports for InAlN/GaN HEMTs. The composite cap layer presented here is believed to expand the application of RF InAlN/GaN HEMTs in high voltage field.

2 Device structure and fabrication

As shown in Figures 1(a)–(e), the simulated off-state electric field distributions (−6 V, 15 V) of InAlN/GaN HEMTs using Silvaco TCAD are presented for devices with different cap layer structures: without cap layer, 2 nm cap layer (2 nm GaN), 4 nm cap layer (2 nm GaN + 2 nm PC-AlN), 8 nm cap layer (2 nm GaN + 6 nm PC-AlN), and 12 nm cap layer (2 nm GaN + 10 nm PC-AlN), respectively. The InAlN/GaN HEMTs without a cap layer suffer from severe current collapse and surface leakage [30]. As illustrated in Figure 1(a), a significant peak electric field is observed beneath the gate region, which increases the risk of device breakdown. Introducing a 2-nm-thick GaN cap layer can partially mitigate this issue: the negative polarization charges at the GaN cap/InAlN barrier interface deplete the channel underneath the gate and suppress the gate leakage current [31]. However, when the GaN cap layer exceeds 2 nm in thickness, it begins to adversely affect the 2DEG in the InAlN/GaN channel [32]. Therefore, a 2 nm GaN cap layer has become the mainstream choice in GaN HEMTs, as it effectively improves the electric field distribution, as shown in Figure 1(b). However, only a 2 nm GaN cap layer is not enough to achieve a qualitative change in the breakdown of GaN HEMTs [33, 34].

The PC-AlN cap layer, with its ultra-wide bandgap, serves as an excellent gate dielectric that simultaneously suppresses gate leakage current and improves surface morphology [35]. As demonstrated in Figure 1(d), the optimized 6 nm-thick PC-AlN layer provides superior electric field modulation compared to uncapped devices. While a thinner 2 nm PC-AlN layer proves insufficient for leakage suppression (Figure 1(c)), increasing the thickness to 10 nm (Figure 1(e)) leads to two critical trade-offs: (1) an enlarged gate-to-channel distance that suffers significant short-channel effects [36]; (2) degraded gate coupling efficiency manifesting as reduced transconductance and elevated contact resistance [29]. Based on these comprehensive considerations, a 6 nm PC-AlN layer was ultimately selected as the optimal gate dielectric thickness, achieving the best balance between leakage suppression and gate control efficiency.

The InAlN/GaN epitaxial structure is grown on a 3-inch semi-insulated SiC substrate by metal organic chemical vapor deposition (MOCVD). As shown in Figure 2(a), the control sample consists of a 350-μm SiC substrate, a 1-μm AlGaN buffer layer, a 100-nm intentional undoped GaN layer, a 1-nm AlN spacer layer, a 1-nm InAlN barrier layer, a 2-nm GaN cap layer, and a 6-nm AlN cap layer. Another InAlN/GaN epitaxial structure with a similar structure (heterojunction distinguished by having an 8-nm InAlN barrier layer, and lacking the AlN cap layer) is used as a reference sample, which is not shown. Two samples are observed with a Bruker AFM and the control sample has a lower surface roughness. Both samples are manufactured using the same standard manufacturing

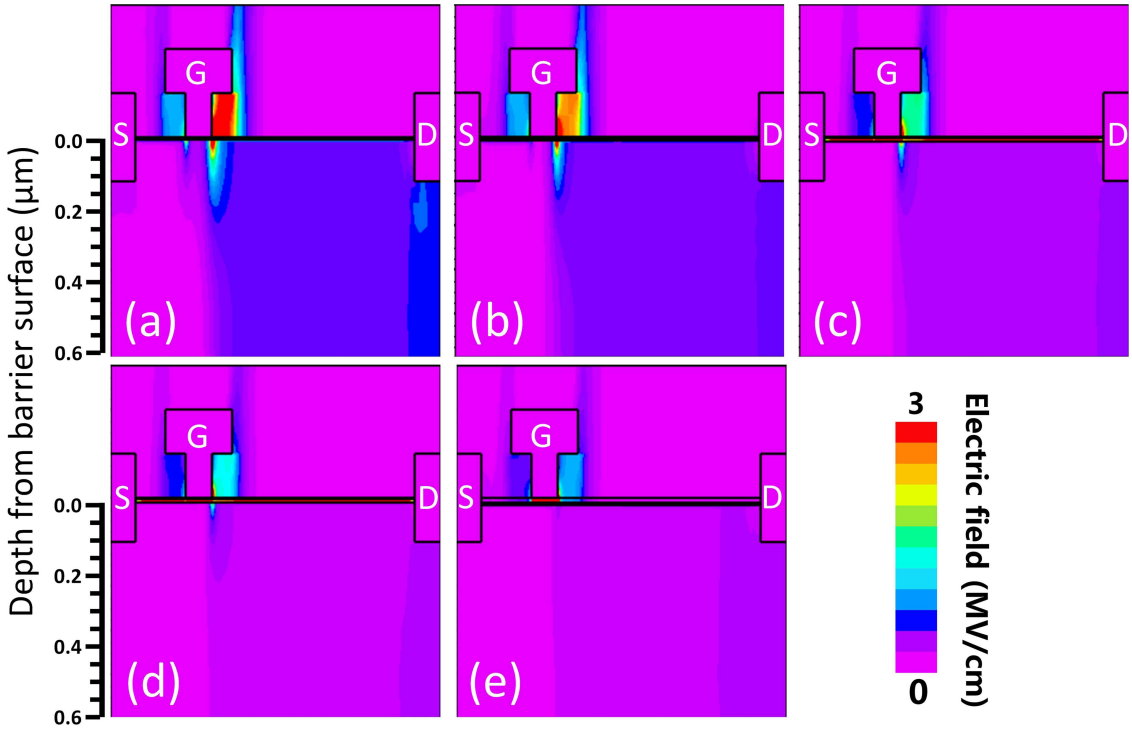

Figure 1 (Color online) The simulated off-state electric field distributions (−6 V, 15 V) of InAlN/GaN HEMTs with different cap layer structures: (a) no cap layer, (b) 2 nm cap layer (2 nm GaN), (c) 4 nm cap layer (2 nm GaN + 2 nm PC-AlN), (d) 8 nm cap layer (2 nm GaN + 6 nm PC-AlN), and (e) 12 nm cap layer (2 nm GaN + 10 nm PC-AlN).

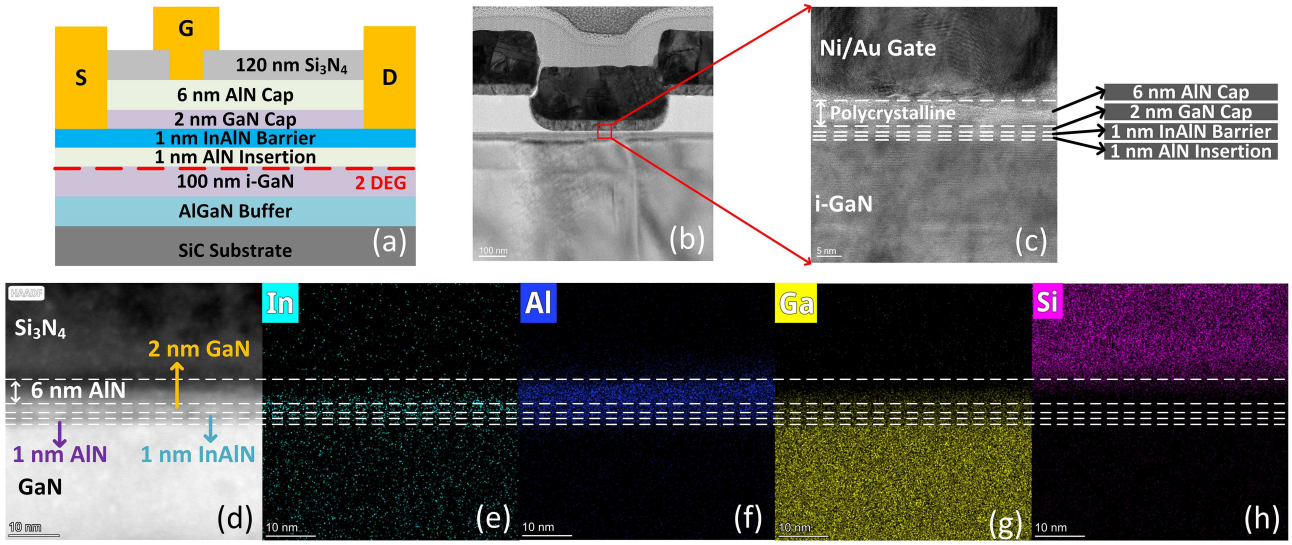

Figure 2 (Color online) (a) Schematic diagram of the InAlN/GaN HEMT with PC-AlN cap. (b) HRTEM image of the gate foot region. (c) Enlarged image of epitaxial layer structure at the gate foot region. (d) Angular Dark Field-Scanning TEM image of epitaxial layer structure. The distribution of elements analyzed by EDX mapping of (e) indium, (f) allium, (g) gallium, and (h) silicon.

process in the laboratory of Xidian University [37, 38]. The two samples have a L_g of 0.5 μm and a source-drain spacing (L_{sd}) of 5.5 μm.

For the control sample, the cross sections of the gate foot region (Figure 2(b)) and InAlN/GaN epitaxial structure region (Figure 2(c)) are observed using high-resolution transmission electron microscopy (HRTEM). As shown in Figure 2(c), the AlN cap layer growing above the GaN cap layer is polycrystalline. The elements in the InAlN/GaN epitaxial layer, including indium (Figure 2(e)), allium (Figure 2(f)), gallium (Figure 2(g)), and silicon (Figure 2(h)), are analyzed using energy dispersive X-ray spectroscopy (EDX). As shown in Figure 2(e), some of the indium from the InAlN barrier layer has segregated into the GaN cap layer, whereas there is no diffusion of indium has occurred

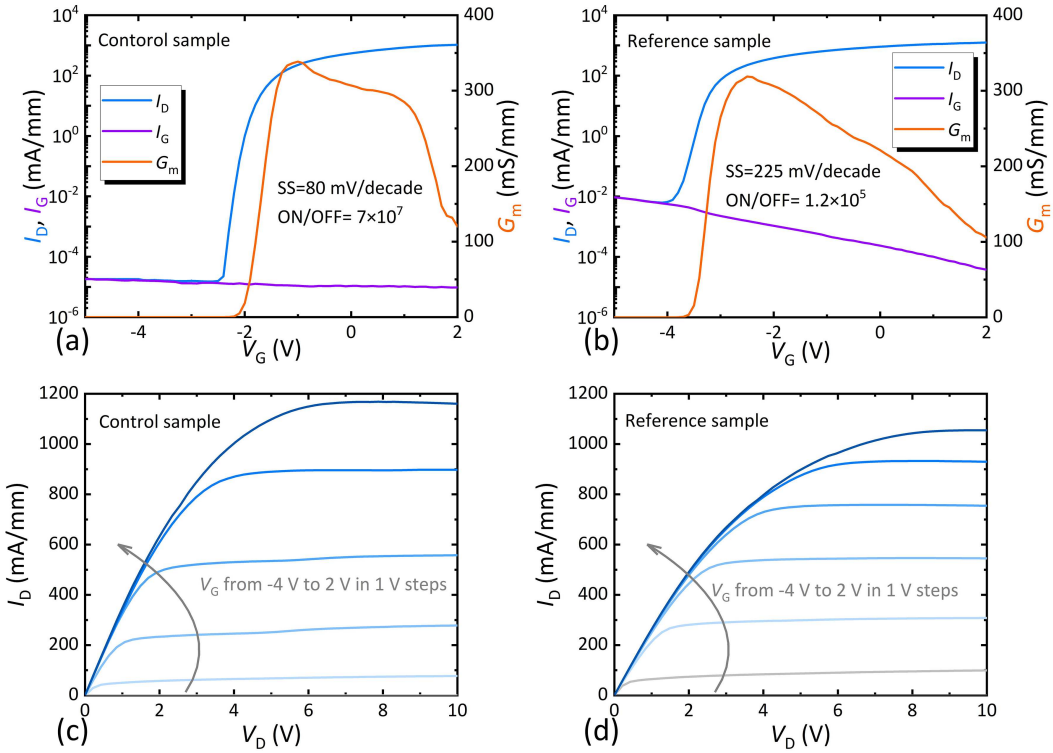

Figure 3 (Color online) Transfer characterization of the (a) control sample and (b) reference sample. The I-V output characteristics of the (c) control sample and (d) reference sample. The devices feature the same dimensions, L_g = 500 nm and L_{sd} = 5.5 μm.

in the PC-AlN cap layer. Therefore, the GaN cap layer can be regarded as a protective layer, which prevents the diffusion of indium elements into the AlN cap layer. Besides, the PC-AlN cap layer smooths the surface undulation of the InAlN barrier layer due to the segregation phenomenon [25].

3 Results and discussion

DC characterization and three-terminal breakdown characterization of the two samples were performed. The transfer characterization of both samples was featured when V_D = 10 V, the results were plotted in Figures 3(a) and (b), respectively. The I-V output characteristics of the control sample and the reference sample are shown in Figures 3(c) and (d), respectively. The test bias voltages for the output characteristics of the two samples were V_D from 0 to 10 V in 0.1 V steps and V_G from −4 to 2 V in 1 V steps. Although the cap layer structure was introduced above the InAlN barrier layer in both samples, the L_g of 0.5 μm resulted in an L_g/tbr (distance between gate and channel) exceeding 50. Good gate control resulted in a G_m close to 350 mS/mm in both samples. Besides, due to the design of the composite cap layer structure, the flattening of the surface of the InAlN barrier layer and the ultra-wide band gap (UWBG) AlN acting as the gate dielectric layer together led to a reduction in the leakage current [25,39]. As a result, the ON/OFF of the control sample was as high as 7×10^7, which was nearly three orders of magnitude higher than the reference sample. In addition, the control sample achieved a low SS of 80 mV/decade whereas the reference sample showed a SS of 225 mV/decade. The low SS of the control sample was mainly attributed to the effective suppression of leakage by the composite cap layer structure [40].

In order to characterize the DIBL effect of the both devices, the I_D-V_G characterization of the two samples at V_D = 1, 5, 10, 15, and 20 V were measured, and the variation of logarithmic I_D with V_G was plotted in Figure 4(a). The DIBL effect of the two samples was analyzed at I_D = 1 mA/mm. The control sample achieved a low DIBL of 2.5 mV/V, which was more than an order of magnitude lower than the values reported in [41,42], and the DIBL of the reference sample was 20 mV/V. The reverse I_G of the control sample was reduced by more than three orders of magnitude compared to the reference sample, and the forward I_G of the control sample was about 1 μA/mm@V_G = 2 V (Figure 4(b)). Therefore, the flattening of the InAlN barrier layer by the composite cap layer structure was beneficial in suppressing the gate leakage phenomenon of InAlN/GaN HEMTs.

In addition, the control sample achieved a high BV of 270 V, which was about three times that of the reference

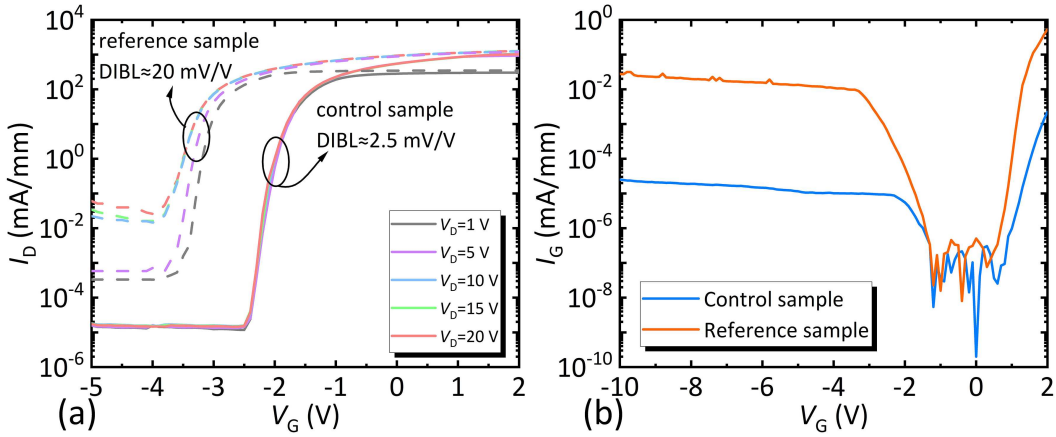

Figure 4 (Color online) (a) Transfer characteristics of the two samples at V_D = 1, 5, 10, 15, and 20 V; (b) Schottky characterization of V_G from −10 to 2 V for both samples.

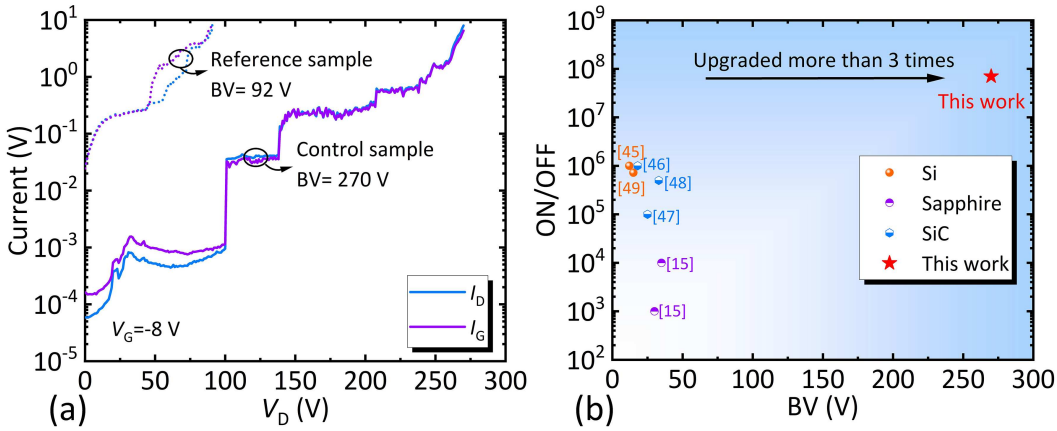

Figure 5 (Color online) (a) Variation of I_G and I_D with V_D for both samples at V_G = −8 V; (b) a summary of the relationship between BV and ON/OFF for InAlN/GaN HEMTs in recent years.

sample (Figure 5(a)). The current of the control sample showed an abrupt change near V_D = 100 V due to the crossing of electrons from the source to the substrate caused by the undoped buffer [43], which may be expected to be improved by Fe/C co-doped or other methods [44]. Figure 5(b) summarizes the ON/OFF versus BV for RF InAlN/GaN HEMTs benchmarked against the other reports [15, 45–49]. Thus, the design of the PC-AlN structure boosted the application voltage of InAlN/GaN HEMTs by more than three times, while featuring a record ON/OFF performance.

The S-parameters of the two samples were characterized from 0.1 to 40 GHz in steps of 0.1 GHz. Current gain (h21), maximum available gain (MAG), and Mason's unilateral gain (U) of the two samples are extracted from the gate bias corresponding to the peak G_m of the device when V_D = 10 V. The $f_T/f_{\max}$ can be obtained by linear extrapolation of the h21/MSG with a slope of 20 dB/decade. As shown in Figures 6(a) and (b), $f_T/f_{\max}$ of the control sample is 22/51.5 GHz and $f_T/f_{\max}$ of the reference sample is 20/47.5 GHz. When V_D = 10 V, the variation of f_T versus V_G for the control sample was depicted in Figure 6(c). Figure 6(d) shown the variation of $f_{\max}$ with V_D for both samples, and the $f_{\max}$ of the reference sample was tested only up to 20 V due to the BV limitation. Finally, the $f_T/f_{\max}$ of the control sample and the reference sample were 22/64 and 20/54 GHz, respectively. We introduce the FoM to evaluate the potential of the device operated at high-frequency and high-voltage applications. The benchmark of the relationship between the BV and the FoM among the RF InAlN/GaN HEMTs as illustrated in Figure 6(e) [12, 15, 19, 23, 33, 45, 46, 48–53]. Due to the effective suppression of leakage, the control sample with composite cap layer simultaneously achieved the highest BV 270 V as well as a record FoM of 8.6 THz·V·μm in InAlN/GaN HEMTs. Thus, the composite cap layer structure design facilitated the development of RF HEMTs towards higher voltage applications.

For next-generation high-power RF systems such as X-band radar and wireless base stations, RF power amplifiers typically should meet the following application requirements. (1) Operating voltage less than one third of break-

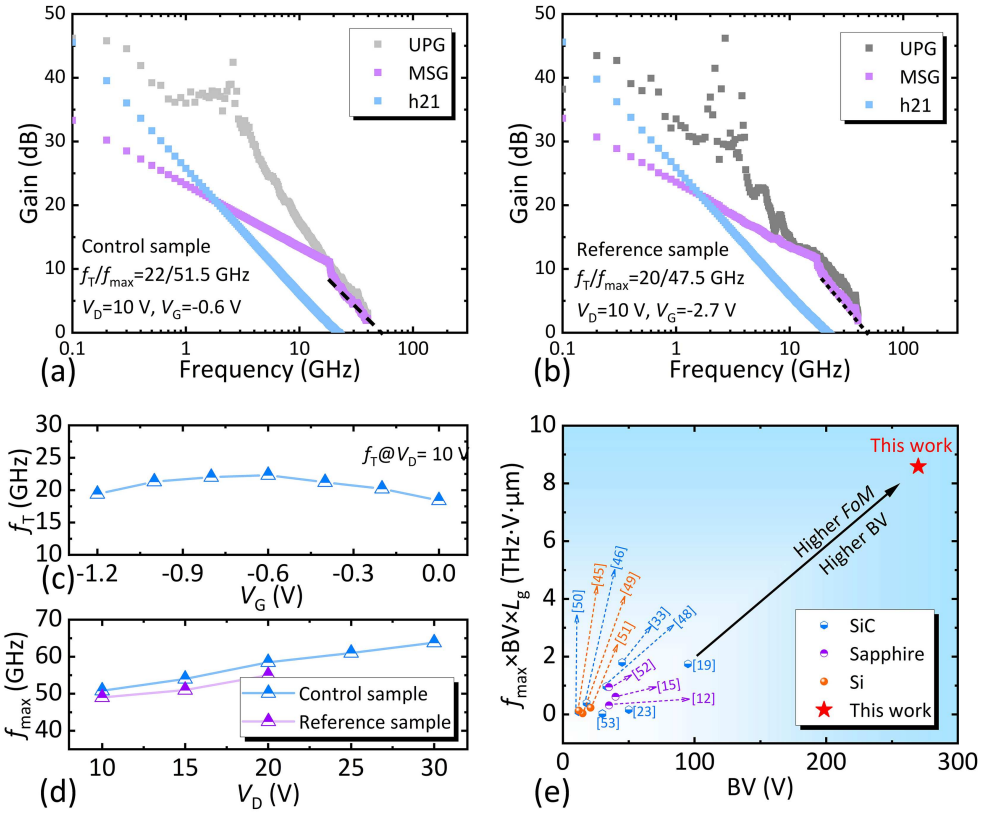

Figure 6 (Color online) Current gain (h21), maximum available gain (MAG), and Mason's unilateral gain (U) of (a) the control sample and (b) the reference sample when V_D = 10 V. (c) The f_T of the control sample varies with V_G at V_D = 10 V. (d) Variation of f_{max} with V_D for both samples. (e) Benchmark of FoM with BV for all InAlN/GaN HEMTs.

down voltage (typical operating voltage for wireless base stations and radars is 48 V), to sustain large RF voltage swings without device failure [54]. (2) Sufficient f_T/f_{max}, or even higher, to cover dedicated frequency bands for wireless communications (2–4 GHz) and radar (8–12 GHz) [8, 55]. (3) Low gate leakage and high ON/OFF ratio, ensuring high PAE and low standby power consumption [56]. (4) High FoM, to capture simultaneous voltage-handling and frequency performance while scaling gate length [44, 57]. The reported InAlN/GaN HEMTs with a 0.5 μm L_g exhibit a high BV of 270 V, low SS of 80 mV/decade while virtually free of DIBL effect (about 2.5 mV/V), together with f_T/f_{max} of 22/64 GHz and an ON/OFF ratio of 7×10^7 (gate leakage <0.3 μA/mm). These achievements culminate in a superior 8.6 THz·V·μm FoM, establishing these devices as premier candidates for high-voltage RF power amplification. Critical to this performance is the innovative GaN/PC-AlN composite cap layer, which uniquely enables simultaneous gate leakage suppression and high-frequency operation-exceeding all essential application requirements for next-generation high-power RF systems.

4 Conclusion

We demonstrate the potential of RF InAlN/GaN HEMTs for high voltage through the design of composite cap layer structure consisting of a GaN cap layer and a PC-AlN cap layer. Due to the effective suppression of gate leakage, the device achieved a high ON/OFF of 7×10^7 and a record BV of 270 V. The device exhibited a low SS of 80 mV/decade and a low DIBL of 2.5 mV/V. In addition, the device had a f_T/f_{max} of 22/64 GHz, and the highest FoM of 8.6 THz·V·μm. The design facilitates the future development of RF InAlN/GaN HEMTs at high voltage RF application.

Acknowledgements This work was supported by Fundamental Research Funds for the Central Universities (Grant No. YJSJ25013), National Natural Science Foundation of China (Grant Nos. 62234009, 62404165, 62090014, 62474135), Fundamental Research Funds for the Central Universities of China (Grant Nos. ZYTS25217, QTZX25069, XJSJ25013), Natural Science Basic Research Program of Shaanxi (Grant No. 2024JC-YBQN-0611), China Postdoctoral Science Foundation (Grant No. 2023M732730), and Postdoctoral Fellowship Program of CPSF (Grant No. GZB20230557).

References

1 Ren Z, Xu J, Le X, et al. Heterogeneous wafer bonding technology and thin-film transfer technology-enabling platform for the next generation applications beyond 5G. Micromachines, 2021, 12: 946
2 Xie H, Liu Z, Hu W, et al. GaN-on-Si HEMTs fabricated with Si CMOS-compatible metallization for power amplifiers in low-power mobile SoCs. IEEE Microw Wireless Compon Lett, 2021, 31: 141–144
3 Sun R, Lai J, Chen W, et al. GaN power integration for high frequency and high efficiency power applications: a review. IEEE Access, 2020, 8: 15529–15542
4 Wang M, Gao P, Shi F, et al. Advanced packaging technology of GaN HEMT module for high-power and high-frequency applications: a review. IEEE Trans Compon Packag Manufact Technol, 2024, 14: 1537–1550
5 Garg T, Kale S. Recent developments, reliability issues, challenges and applications of GaN HEMT technology. IEEE Electron Devices Rev, 2024, 1: 16–30
6 Mounika B, Ajayan J, Bhattacharya S, et al. Recent developments in materials, architectures and processing of AlGaN/GaN HEMTs for future RF and power electronic applications: a critical review. Micro NanoStruct, 2022, 168: 207317
7 Ajayan J, Nirmal D, Mohankumar P, et al. Challenges in material processing and reliability issues in AlGaN/GaN HEMTs on silicon wafers for future RF power electronics & switching applications: a critical review. Mater Sci Semicond Process, 2022, 151: 106982
8 Wang X, Lin Z Y, Sun Y H, et al. Suppression of the regrowth interface leakage current in AlGaN/GaN HEMTs by Fe doped GaN substrate. Sci China Inf Sci, 2024, 67: 169403
9 Chang Q Y, Hou B, Yang L, et al. High-voltage quasi-vertical GaN-on-Si Schottky barrier diode with edge termination structure of optimized multi-level N ion implantation. Sci China Inf Sci, 2024, 67: 229402
10 An S R, Mi M H, Wang P F, et al. A novel multi-threshold coupling InAlN/GaN double-channel HEMT for improving transconductance flatness. Sci China Inf Sci, 2024, 67: 119402
11 Kuzmik J. Power electronics on InAlN/(In)GaN: prospect for a record performance. IEEE Electron Device Lett, 2001, 22: 510–512
12 Medjdoub F, Carlin J-F, Gonschorek M et al. Can InAlN/GaN be an alternative to high power/high temperature AlGaN/GaN devices? In: Proceedings of International Electron Devices Meeting, 2006. 1–4
13 Gonschorek M, Carlin J-F, Feltin E et al. Two-dimensional electron gas density in $Al1_xIn_xN$/AlN/GaN heterostructures ($0.03 \leqslant x \leqslant 0.23$). J Appl Phys, 2008, 103: 093714
14 Crespo A, Bellot M M, Chabak K D, et al. High-power Ka-band performance of AlInN/GaN HEMT with 9.8-nm-thin barrier. IEEE Electron Device Lett, 2010, 31: 2–4
15 Kuzmik J, Ostermaier C, Pozzovivo G, et al. Proposal and performance analysis of normally off n^{++} GaN/InAlN/AlN/GaN HEMTs with 1-nm-thick InAlN barrier. IEEE Trans Electron Devices, 2010, 57: 2144–2154
16 Saunier P, Schuette M L, Chou T M, et al. InAlN barrier scaled devices for very high f_T and for low-voltage RF applications. IEEE Trans Electron Devices, 2013, 60: 3099–3104
17 Yue Y, Hu Z, Guo J, et al. Ultrascaled InAlN/GaN high electron mobility transistors with cutoff frequency of 400 GHz. Jpn J Appl Phys, 2013, 52: 08JN14
18 Tirelli S, Marti D, Sun H, et al. Fully passivated AlInN/GaN HEMTs with $f_{\mathrm{T}}/f_{\mathrm{MAX}}$ of 205/220 GHz. IEEE Electron Device Lett, 2011, 32: 1364–1366
19 Downey B P, Meyer D J, Katzer D S, et al. SiN_x/InAlN/AlN/GaN MIS-HEMTs with 10.8 THz·V Johnson figure of merit. IEEE Electron Device Lett, 2014, 35: 527–529
20 Lee D S, Gao X, Guo S, et al. 300-GHz InAlN/GaN HEMTs with InGaN back barrier. IEEE Electron Device Lett, 2011, 32: 1525–1527
21 Lee D S, Chung J W, Wang H, et al. 245-GHz InAlN/GaN HEMTs with oxygen plasma treatment. IEEE Electron Device Lett, 2011, 32: 755–757
22 Lee D S, Gao X, Guo S, et al. InAlN/GaN HEMTs with AlGaN back barriers. IEEE Electron Device Lett, 2011, 32: 617–619
23 Wang R, Li G, Laboutin O, et al. 210-GHz InAlN/GaN HEMTs with dielectric-free passivation. IEEE Electron Device Lett, 2011, 32: 892–894
24 Wang R, Saunier P, Xing X, et al. Gate-recessed enhancement-mode InAlN/AlN/GaN HEMTs with 1.9-A/mm drain current density and 800-mS/mm transconductance. IEEE Electron Device Lett, 2010, 31: 1383–1385
25 Ganguly S, Konar A, Hu Z, et al. Polarization effects on gate leakage in InAlN/AlN/GaN high-electron-mobility transistors. Appl Phys Lett, 2012, 101: 253519
26 Hickman A, Chaudhuri R, Bader S J, et al. High breakdown voltage in RF AlN/GaN/AlN quantum well HEMTs. IEEE Electron Device Lett, 2019, 40: 1293–1296
27 Hou B, Ma X H, Chen W W, et al. Using in-process measurements of open-gate structures to evaluate threshold voltage of normally-off GaN-based high electron mobility transistors. Appl Phys Lett, 2015, 107: 163503
28 Yu E T, Dang X Z, Yu L S, et al. Schottky barrier engineering in III-V nitrides via the piezoelectric effect. Appl Phys Lett, 1998, 73: 1880–1882
29 Selvaraj S L, Ito T, Terada Y, et al. AlN/AlGaN/GaN metal-insulator-semiconductor high-electron-mobility transistor on 4 in. silicon substrate for high breakdown characteristics. Appl Phys Lett, 2007, 90: 173506
30 Wang R, Li G, Guo J et al. Dispersion-free operation in InAlN-based HEMTs with ultrathin or no passivation. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2013
31 Jurkovic M, Gregusova D, Palankovski V, et al. Schottky-barrier normally off GaN/InAlN/AlN/GaN HEMT with selectively etched access region. IEEE Electron Device Lett, 2013, 34: 432–434
32 Charles M, Baines Y, Bouis R, et al. The characterization and optimization of GaN cap layers and SiN cap layers on AlGaN/GaN HEMT structures grown on 200 mm GaN on silicon. Phys Status Solidi, 2018, 255: 1700406
33 Tirelli S, Lugani L, Marti D, et al. AlInN-based HEMTs for large-signal operation at 40 GHz. IEEE Trans Electron Devices, 2013, 60: 3091–3098
34 Marti D, Tirelli S, Teppati V, et al. 94-GHz large-signal operation of AlInN/GaN high-electron-mobility transistors on silicon with regrown ohmic contacts. IEEE Electron Device Lett, 2015, 36: 17–19
35 Jia M, Hou B, Yang L, et al. Improved p-GaN/AlGaN/GaN HEMTs with magnetronsputtered AlN cap layer. Appl Surf Sci, 2025, 682: 161699
36 Wu S, Mi M, Zhang M, et al. A high RF-performance AlGaN/GaN HEMT with ultrathin barrier and stressor in situ SiN. IEEE Trans Electron Devices, 2021, 68: 5553–5558
37 Li S, Wu M, Yang L, et al. 15.1 W/mm power density GaN-on-GaN HEMT with high-gradient stepped-C doped buffer. IEEE Electron Device Lett, 2025, 46: 365–368
38 Liu S Y, Ma X H, Zhu J J, et al. Improved transport properties and mechanism in recessed-gate InAlN/GaN HEMTs using a self-limited surface restoration method. Sci China Inf Sci, 2022, 65: 202401
39 Wu Y, Liu S, Zhang J, et al. Novel in-situ AlN/p-GaN gate HEMTs with threshold voltage of 3.9 V and maximum applicable gate voltage of 12.1 V. IEEE Trans Electron Devices, 2023, 70: 424–428
40 Cui P, Mercante A, Lin G, et al. High-performance InAlN/GaN HEMTs on silicon substrate with high $f_T \times L_g$. Appl Phys Express, 2019, 12: 104001
41 Malmros A, Gamarra P, Di Forte-Poisson M A, et al. Evaluation of thermal versus plasma-assisted ALD Al_2O_3 as passivation for

InAlN/AlN/GaN HEMTs. IEEE Electron Device Lett, 2015, 36: 235–237
42 Cui P, Jia M, Chen H, et al. InAlN/GaN HEMT on Si with $f_{\max}$ = 270 GHz. IEEE Trans Electron Devices, 2021, 68: 994–999
43 Choi Y C, Pophristic M, Cha H Y, et al. The effect of an Fe-doped GaN buffer on off-state breakdown characteristics in AlGaN/GaN HEMTs on Si substrate. IEEE Trans Electron Devices, 2006, 53: 2926–2931
44 Wu M, Zhang M, Yang L et al. First demonstration of state-of-the-art GaN HEMTs for power and RF applications on a unified platform with free-standing GaN substrate and Fe/C co-doped buffer. In: Proceedings of International Electron Devices Meeting (IEDM), 2022
45 Li L, Nomoto K, Pan M, et al. GaN HEMTs on Si with regrown contacts and cutoff/maximum oscillation frequencies of 250/204 GHz. IEEE Electron Device Lett, 2020, 41: 689–692
46 Zhou Y, Zhu J, Mi M, et al. Analysis of low voltage RF power capability on AlGaN/GaN and InAlN/GaN HEMTs for terminal applications. IEEE J Electron Devices Soc, 2021, 9: 756–762
47 Xu D, Chu K K, Diaz J A, et al. 0.1-μm atomic layer deposition Al_2O_3 passivated InAlN/GaN high electron-mobility transistors for E-band power amplifiers. IEEE Electron Device Lett, 2015, 36: 442–444
48 Mi M, Zhang M, Wu S, et al. High performance InAlN/GaN high electron mobility transistors for low voltage applications*. Chin Phys B, 2020, 29: 057307
49 Xie H, Liu Z, Gao Y, et al. Deeply-scaled GaN-on-Si high electron mobility transistors with record cut-off frequency f_T of 310 GHz. Appl Phys Express, 2019, 12: 126506
50 Schuette M L, Ketterson A, Song B, et al. Gate-recessed integrated E/D GaN HEMT technology with $f_T/f_{\max}$ >300 GHz. IEEE Electron Device Lett, 2013, 34: 741–743
51 Tsou C W, Lin C Y, Lian Y W, et al. 101-GHz InAlN/GaN HEMTs on silicon with high Johnson's figure-of-merit. IEEE Trans Electron Devices, 2015, 62: 2675–2678
52 Lecourt F, Ketteniss N, Behmenburg H, et al. InAlN/GaN HEMTs on sapphire substrate with 2.9-W/mm output power density at 18 GHz. IEEE Electron Device Lett, 2011, 32: 1537–1539
53 Yue Y, Hu Z, Guo J, et al. InAlN/AlN/GaN HEMTs with regrown ohmic contacts and f_T of 370 GHz. IEEE Electron Device Lett, 2012, 33: 988–990
54 Formicone G, Burger J, Custer J. 150 V-bias RF GaN for 1 kW UHF radar amplifiers. In: Proceedings of IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), 2016. 1–4
55 Nakajima S. GaN HEMTs for 5G base station applications. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), 2018
56 Jimenez J L, Chowdhury U. X-band GaN FET reliability. In: Proceedings of IEEE International Reliability Physics Symposium (IRPS), 2008. 429–435
57 Zheng X, Guidry M, Li H, et al. N-polar GaN MIS-HEMTs on sapphire with high combination of power gain cutoff frequency and three-terminal breakdown voltage. IEEE Electron Device Lett, 2016, 37: 77–80