SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

March 2026, Vol. 69, Iss. 3, 132402:1–132402:9
https://doi.org/10.1007/s11432-025-4698-1

Ultrahigh thermal-stable p-type WSe_2 transistors with silicon processing-compatible metal-semiconductor contacts

Junlin HUANG[1,2†], Li GAO[1,2†], Zhangyi CHEN[1,2], Zeen JIA[1,2], Yuyin LIN[1,2], Mengyu HONG[1,2], Huihui YU[1,2], Xiankun ZHANG[1,2*], Zheng ZHANG[1,2*] & Yue ZHANG[1,2*]

[1]*Academy for Advanced Interdisciplinary Science and Technology, Key Laboratory of Advanced Materials and Devices for Post-Moore Chips Ministry of Education, State Key Laboratory for Advanced Metals and Materials, University of Science and Technology Beijing, Beijing 100083, China*
[2]*Future Chip Materials & Technology Innovation Center, School of Future Technology, School of Materials Science and Engineering, Beijing Key Laboratory for Advanced Energy Materials and Technologies, University of Science and Technology Beijing, Beijing 100083, China*

Received 20 July 2025/Revised 12 September 2025/Accepted 25 November 2025/Published online 7 January 2026

Abstract High-performance p-type transistors are a fundamental and arduous challenge for the development of two-dimensional (2D) semiconductors in CMOS integrated circuits. The lack of a p-type modulation strategy that combines high hole transport and excellent stability seriously hinders the development of 2D p-type transistors. Here, we report a spontaneous oxidation intercalation technique for metal/semiconductor contact interfaces, which achieves high hole transport and excellent thermal stability of tungsten diselenide (WSe_2) transistor. A tungsten oxide (WO_x) buffer layer is constructed between the contact interface of metal and WSe_2 by spontaneous oxidation after plasma etching. This metal-WO_x-WSe_2 contact interface enhances hole transport and significantly reduces the contact resistance by 10^3. Furthermore, the WO_x buffer layer with high thermal stability ensures that the WSe_2 transistor maintains almost non decaying p-type characteristics even after long-term annealing up to 400°C, meeting the thermal budget for back-end-of-line integration. This contact strategy is compatible with silicon-based processes and has been successfully applied to the construction of homogeneous WSe_2 CMOS inverters.

Keywords WSe_2 transistors, p-type modulation, contact engineering, oxide layer intercalation, thermal stability

Citation Huang J L, Gao L, Chen Z Y, et al. Ultrahigh thermal-stable p-type WSe_2 transistors with silicon processing-compatible metal-semiconductor contacts. Sci China Inf Sci, 2026, 69(3): 132402, https://doi.org/10.1007/s11432-025-4698-1

1 Introduction

Two-dimensional (2D) transition metal dichalcogenide (TMDCs) semiconductors are considered ideal channel materials for post-silicon-era electronics due to their high carrier mobility and superior electrical properties [1–3]. However, achieving p-type transport in most 2D TMDCs remains significantly more challenging than achieving n-type transport due to the Fermi-level pinning effect and the strong electron doping caused by intrinsic structural defects [4–6]. The performance mismatch between n-FET and p-FET hinders the realization of high-performance complementary metal-oxide-semiconductor (CMOS) logic devices based on 2D TMDCs [7], posing a major obstacle to building 2D integrated circuits. Therefore, achieving high-performance hole transport in 2D transistors is a critical issue that must be resolved to develop CMOS integrated circuits.

The p-type modulation methods for 2D TMDCs transistors can be primarily categorized into channel doping and contact engineering. Channel doping faces challenges such as carrier scattering-induced mobility degradation and low stability [8, 9]. In contrast, contact engineering demonstrates unique advantages by mitigating the Fermi-level pinning effect and improving carrier injection efficiency [10–12]. On the other hand, for practical applications, two compatibility issues must be given special attention. First, the fabrication processes for 2D semiconductor devices must be compatible with mature silicon-based micro/nanofabrication technologies [13, 14]. Second, the stability of a 2D semiconductor device must be maintained during processing [15]. A critical performance metric is whether

* Corresponding author (email: zhangxiankun@ustb.edu.cn, zhangzheng@ustb.edu.cn, yuezhang@ustb.edu.cn)
† These authors contributed equally to this work.

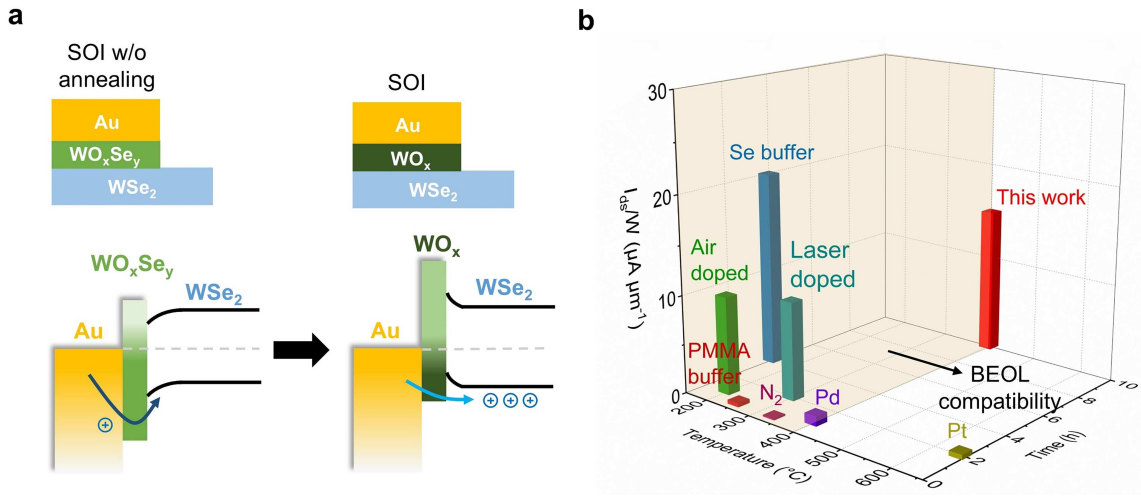

Figure 1 (Color online) Effect of SOI contact modulation. (a) Schematic diagram of SOI control mechanism at metal/semiconductor contact interface. Annealing reduces the hole Schottky barrier of the contact interface and promotes hole transport. (b) Comparison of electrical performance and thermal stability of our SOI modulation transistors and other reported p-type WSe_2 transistors [40–47].

devices can remain stable under the thermal budget of 400°C required for back-end-of-line (BEOL) integration processes [16, 17].

At present, the commonly used methods for p-type regulation in the metal-semiconductor contact regions of 2D TMDCs include van der Waals (vdW) electrode contacts (such as transferred electrodes [18–21], 2D semimetal contacts [22–26], and surface charge transfer doping [27–32]). However, vdW electrode contacts face challenges in compatibility with mature silicon-based integration processes due to their complex fabrication. Transferred electrodes rely on mechanical alignment, leading to poor device uniformity and difficulty in meeting high-density integration requirements [33]. 2D semimetal contacts predominantly utilize metastable-phase metallic 2D TMDCs, which undergo phase transitions under high-temperature annealing [34–36]. Meanwhile, surface charge transfer doping struggles to maintain stable performance in silicon-based processes, as high-temperature annealing during fabrication induces desorption of dopants [37]. Therefore, achieving thermally stable, high-performance p-type metal-semiconductor contact interfaces compatible with silicon-based processes remains a critical challenge [38, 39].

Here, we report a p-type modulation method for spontaneous oxidative intercalation (SOI) of WSe_2 transistors in the metal-semiconductor contact regions with high hole transport and excellent thermal stability. The contact interface modulation mechanism is demonstrated in Figure 1(a). An oxide buffer layer is constructed between the metal and WSe_2 through Ar plasma etching and spontaneous oxidation. After high-temperature annealing, the oxide layer transforms from WO_xSe_y to WO_x with increased oxygen content, leading to a significant enhancement in work function and thermal stability. This change induces significant band bending at the contact interface, thus enabling efficient hole injection and reducing the Schottky barrier height to 26.3 meV. Figure 1(b) demonstrates the exceptional thermal stability of this contact interface. Compared to other p-type WSe_2 transistors, this method exhibits nearly undegraded p-type modulation effectiveness even after 400°C high-temperature annealing. Furthermore, the device performance remains stable after prolonged 10 h annealing at 300°C. Finally, we demonstrate the fabrication of homogeneous CMOS inverters on WSe_2 using this contact modulation strategy.

2 Materials and methods

Material preparation: Firstly, before preparing the WSe_2 sample, it is necessary to clean the 300 nm SiO_2/p^{++} Si substrate with acetone and isopropanol, followed by a secondary cleaning of the silicon wafer surface using oxygen plasma etching. Then, WSe_2 nanosheets (HQ Graphene) were stripped onto the substrate. Subsequently, spin coat polymethyl methacrylate (PMMA) and define regular WSe_2 stripes using electron beam lithography (EBL) and plasma (SF_6) etching processes.

SOI contact modulation: Firstly, spin coat PMMA on the surface of WSe_2 and define the source/drain using EBL. After development, Ar plasma was used to etch the WSe_2 contact area for different periods of time at 4 W and 5 sccm. Then, 30 nm Au electrodes were deposited under ultra-high vacuum (10^{-8} Torr) using physical vapor deposition (PVD) equipment. Finally, the constructed WSe_2 transistor was annealed at 300°C for 1 h in a low vacuum (1 mbar) Ar atmosphere to complete the p-type modulation of the WSe_2 metal-semiconductor contact

region.

Material characterization and device electrical measurement: The electrical performance of the device was measured using the Keysight B1500A semiconductor parameter analyzer in Lakeshore. The Raman and photoluminescence spectroscopy (PL) spectra of the sample were measured using a Witec Raman microscope at a laser wavelength of 532 nm and a laser power of 1 mW. The morphology and surface potential of the sample were characterized using an atomic force microscope (AFM) paired with an SCM-PIT probe. Morphology was measured in peak force mode and surface potential was measured in tapping mode. The binding energy of the material was characterized by X-ray photoelectron spectroscopy (XPS) using Thermo Scientific Nexsa G2. And the band information of the material was characterized by UPS, and the ultraviolet light source used was a He I source (21.22 eV).

3 Result and discussion

The SOI contact modulation strategy combines nanolithography technology with the etching-oxidation-annealing (EOA) processing technique. As shown in Figure 2(a), the fabrication process involves several key steps. First, the source/drain patterned areas are then etched using Ar plasma. The high-energy plasma bombardment during etching disrupts both the surface structure and chemical bonds of WSe_2. Subsequently, exposure to ambient air causes the damaged material surface to rapidly react with oxygen, forming an amorphous oxide layer. Finally, the device with constructed electrodes was annealed in an Ar atmosphere to modulate contact performance. The device we constructed is shown in Figure 2(b). Here, we constructed two transistors of the same size on the same WSe_2 nanosheet. One metal-semiconductor contact area is untreated, the other uses EOA to treat the contact interface, which can be used to compare the performance changes of the transistor before and after modulation.

The transfer characteristics of the WSe_2 transistor are shown in Figure 2(c). For the pristine WSe_2 device, the transfer characteristic curve exhibits ambipolar transport behavior with an n-type preference due to the Fermi-level pinning effect in WSe_2 [48]. After SOI modulation without annealing, specifically after etching-oxidation, the transistor demonstrates enhanced n-type transport characteristics, with the electron current increasing by approximately one order of magnitude. Then after annealing, the threshold voltage shifts to the right, and the hole current increases from 83 nA to 1.4 μA, while the electron current decreases by six orders of magnitude, achieving a transition from n-type to p-type transport dominance. This is attributed to the improvement of the quality of the contact interface oxide layer, which enhances the hole transport in WSe_2 transistors. From the output characteristics in Figures 2(d) and (e), the SOI transistor without annealing does not show an obvious enhancement of hole current. After annealing, the hole current increases, indicating a significant reduction in the transport barrier of holes. The nonlinearity factor N, which serves as a quantitative indicator of metal-semiconductor contact quality, is defined as $N = \dfrac{d^2 I_{ds}/dV_{ds}^2}{2\,(dI_{ds}/dV_{ds})}$. A higher N value corresponds to stronger nonlinearity and a larger Schottky barrier. As shown in Figure 2(f), the pristine transistors exhibit substantial nonlinearity (high Schottky barrier), whereas in SOI modulation transistors, the nonlinearity drastically decreases. Notably, the nonlinearity approaches zero when $V_{ds} > -1\,\mathrm{V}$, confirming ohmic contact behavior in the annealed WSe_2 transistor. In addition, we also used the transfer-length-method (TLM) to measure the contact resistance of the pristine and SOI-WSe_2 transistors, as shown in Figure 2(g). It was observed that the contact resistance of SOI-WSe_2 transistors decreased from 46 MΩ·μm to 58 kΩ·μm, a decrease of about 3 orders of magnitude. This indicates that SOI modulation greatly improves WSe_2 hole contact performance.

To investigate the performance variation of SOI-WSe_2 transistors, we used metal Pt and Pd with different work functions as source and drain electrodes, and the transfer characteristic curve is shown in Figure S1. It can be observed that the hole current in Pt and Pd contact transistors shows no significant difference compared to Au contacts. This indicates that the work function of the electrode has almost no effect on the p-type modulation effect of SOI transistors, and the contact oxide layer dominates the carrier transport. For the influence of annealing environment on SOI modulation, we used different atmospheres to anneal the SOI modulation transistor. The transfer characteristic curves of transistors before and after annealing are shown in Figure S2. Low vacuum (1 mbar) annealing, high vacuum (10^{-5} mbar) annealing, and annealing after 20 nm Sb_2O_3 packaged in Ar atmosphere can all produce p-type modulation effect. This indicates that the p-type modulation effect during annealing is independent of the environment during the annealing process. We then used oxygen plasma etching for the EOA process. We found that the transmission performance of the transistor after oxygen plasma etching is inferior to that after Ar plasma etching and oxidation. The possible reason is that oxygen plasma causes excessive damage to the material, destroys the quality of the WO_x buffer layer, and affects the transport of hole carriers (Figure S3). For transistors

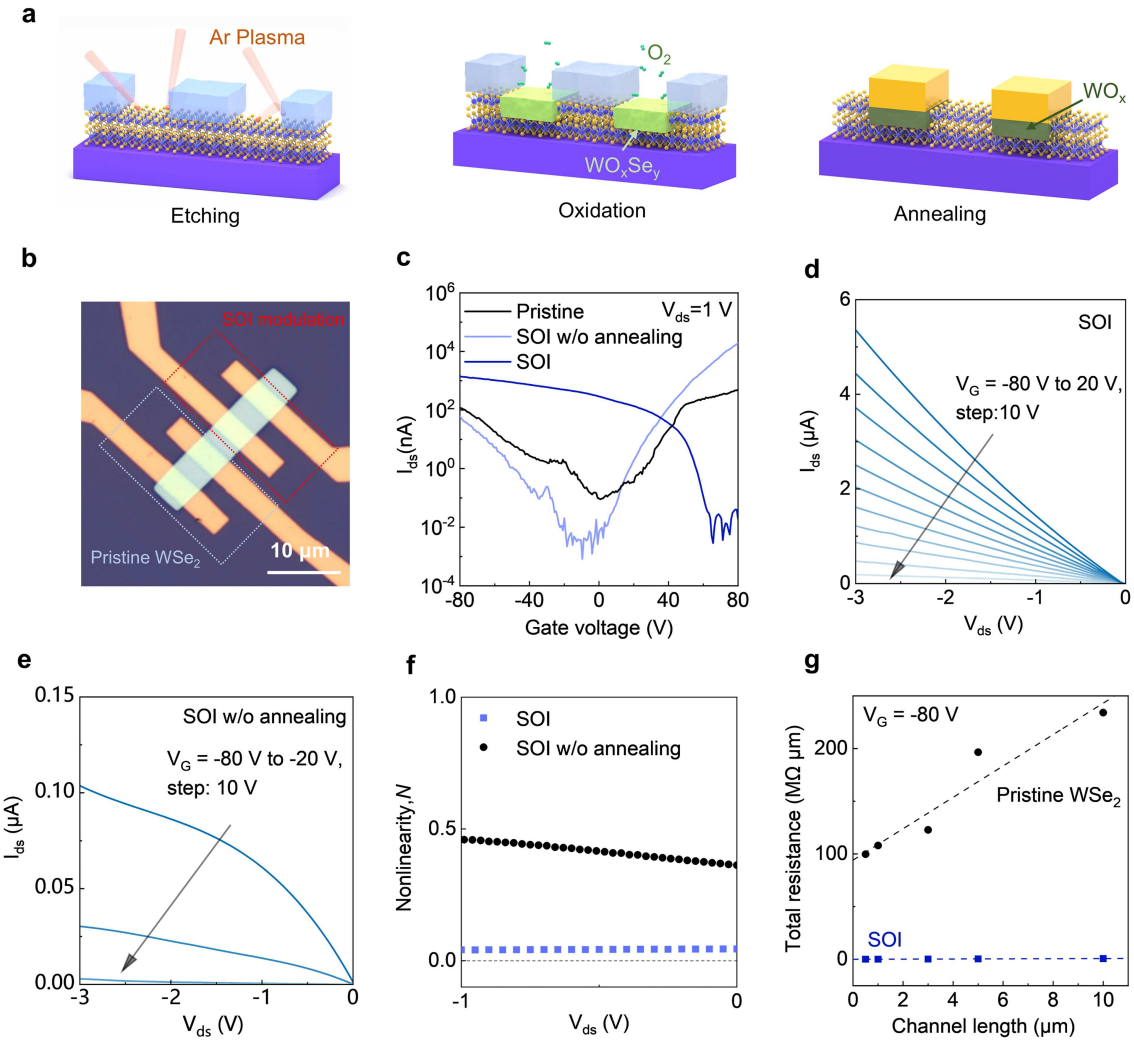

Figure 2 (Color online) Construction and electrical properties of SOI-WSe_2 transistors. (a) SOI-WSe_2 transistor fabrication process; (b) optical microscopy image of pristine and SOI-WSe_2 transistors; (c) transfer characteristic curves of intrinsic, SOI without annealing, and SOI with annealing WSe_2 transistors; output characteristic curves of transistors (d) after and (e) before annealing; (f) relationship between nonlinearity and gate voltage of the output curves of SOI modulation transistors before and after annealing; (g) contact resistance of intrinsic and SOI-WSe_2 transistors measured by TLM.

with different Ar etching times, it can be seen that the optimal performance is achieved when the etching time is 10 s. As the etching time continues to increase, the mobility and hole current of the transistor decrease due to the worsening of the contact interface damage. To characterize the barrier at the metal-semiconductor contact interface after SOI modulation, the Schottky barrier height was measured using a variable temperature transport, as shown in Figure S4. It can be seen that after SOI modulation, the hole Schottky barrier reaches an ultra-low value of 26.3 meV. It is because the WO_x buffer layer with a high work function achieves a good energy band matching and improves the hole transport efficiency at the WSe_2 contact interface, which also effectively reduces the Fermi level pinning effect caused by direct contact between metal and WSe_2. This low Schottky barrier also has advantages compared to other research of p-type contact WSe_2 transistor [49–52]. It can also be seen from the output characteristic curve that the device can maintain ohmic contact at low temperature, as shown in Figure S5. This indicates its extremely low Schottky barrier.

To characterize the p-type modulation mechanism of the SOI contact method, we first performed high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) characterization on the metal-semiconductor contact interface subjected to SOI contact modulation, as shown in Figure 3(a). After SOI modulation, it can be seen from the energy dispersive spectroscopy (EDS) that the Se element content in the contact area has significantly decreased, while oxygen elements have been enriched, as shown in Figure 3(b). It is indicated that the two layers of WSe_2 on the surface have transformed into an amorphous oxide layer after etching-oxidation. From the atomic force microscope (AFM) characterization, it can be seen that the material thickness increased

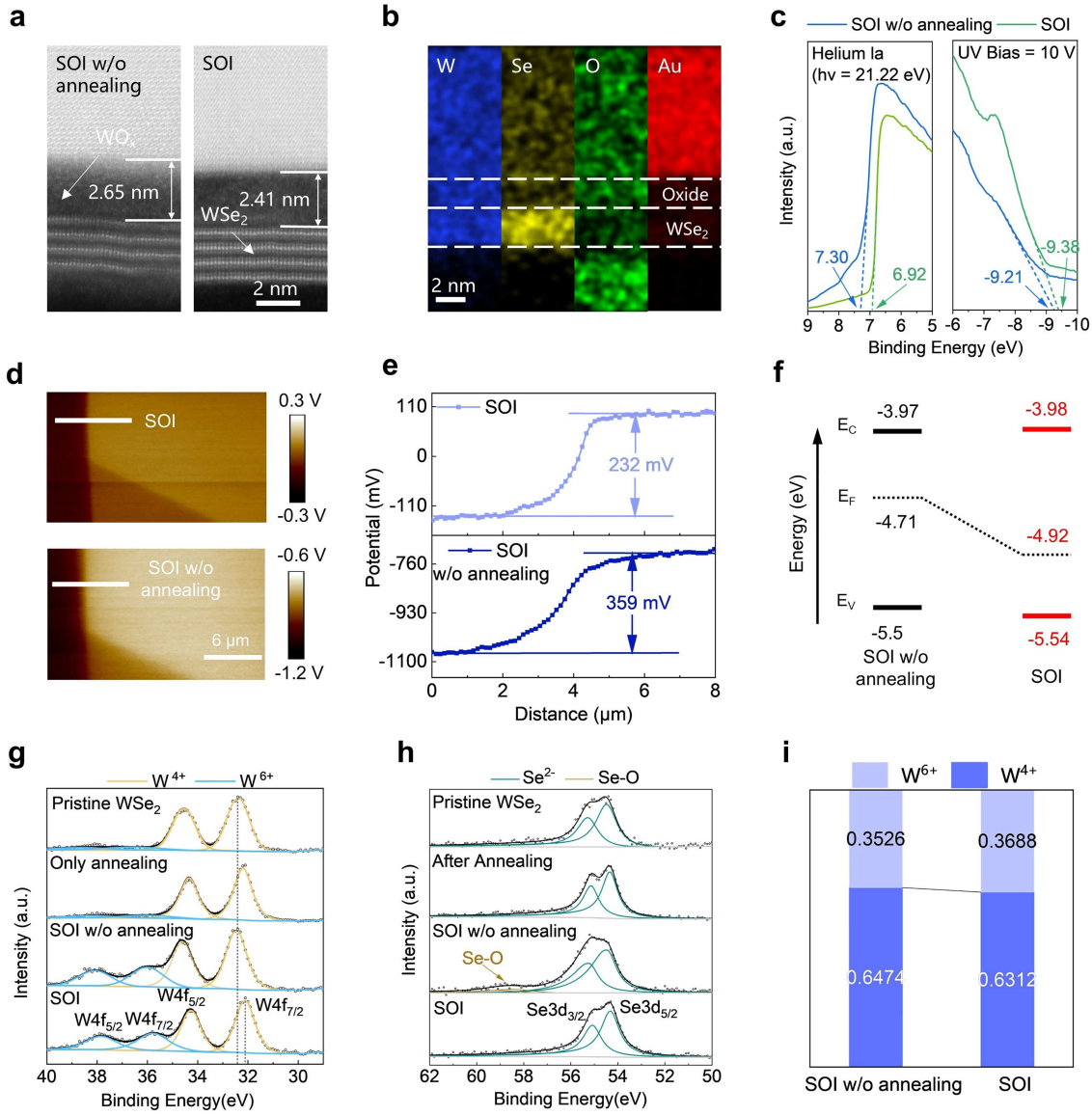

Figure 3 (Color online) Mechanism analysis of SOI modulation WSe_2. (a) Cross-sectional STEM image of SOI modulation WSe_2 metal-semiconductor contact interface before and after annealing; (b) EDS map of SOI modulation WSe_2 contact interface; (c) UPS characterization of SOI modulation WSe_2 before and after annealing; (d) KPFM map of SOI modulation WSe_2 before and after annealing; (e) surface potential of SOI modulation WSe_2 before and after annealing measured by KPFM; (f) energy level diagram of SOI modulation WSe_2 before and after annealing; XPS spectra of (g) W 4f and (h) Se 3d of pristine and SOI modulation WSe_2 before and after annealing; (i) W^{4+} and W^{6+} ratios of SOI modulation WSe_2 before and after annealing.

by 1.355 nm after etching, as shown in Figure S6, which also indicates the formation of the oxide layer. After annealing, the thickness of the oxide layer decreased from 2.65 to 2.41 nm, indicating that the oxide layer became denser and its chemical composition changed. And it is interesting that WSe_2 becomes smoother after annealing, which may also contribute to the improvement of hole transport. Ultraviolet photoelectron spectroscopy (UPS) is an effective method for characterizing the band structure of materials, as shown in Figures 3(c) and (f). The energy of ultraviolet light is 21.22 eV. To meet the testing requirements, we applied a bias voltage of 10 V to the energy spectrum during measurement. The work function of the material is given by $\phi = h\nu - (E_{\mathrm{Cutoff}} - E_{\mathrm{Fermi}})$. It can be calculated that the work function of the SOI modulation WSe_2 increases from 4.75 eV before annealing to 4.90 eV after annealing. Moreover, the difference between the Fermi level (E_F) and the valence band top (E_{VBM}) shifts from 0.89 to 0.69 eV, and the downward shift of the Fermi level also represents the transfer of electrons from WSe_2 to the oxide layer after annealing. Based on this, the energy level diagram of SOI modulation WSe_2 before and after annealing can be plotted. And from the Kelvin probe force microscopy (KPFM) characterization before and after annealing, it can be measured that the potential difference between materials is given by $\Delta V = \frac{\phi_{\mathrm{sample2}} - \phi_{\mathrm{sample1}}}{e}$.

The potential difference decreased from 359 mV before annealing to 232 mV after annealing. Taking the work function of Au as 5.1 eV, as shown in Figures 3(d) and (e), the calculated work function of SOI modulation WSe_2 before annealing was 4.741 eV, and after annealing was 4.862 eV, which is consistent with the measurement results of UPS. High temperature annealing can increase the work function of the oxide layer formed by the etching-oxidation, thereby achieving a p-type modulation effect on WSe_2.

WSe_2 before and after SOI modulation was characterized by X-ray photoelectron spectroscopy (XPS). As shown in Figures 3(g) and (h), the peak position of W^{6+} (corresponding to WO_3) appears after SOI modulation without annealing, indicating the oxidation of WSe_2. The ratio of peak area to sensitivity factor in XPS can characterize the relative content of elements and valence states. For WSe_2 after SOI modulation, the percentage content of W^{6+} increased from 35% to 37% before and after annealing, as shown in Figure 3(i). This indicates an increase in the valence of the W element in the oxide layer. For tungsten oxide, the increase in the valence state of metal ions leads to an increase in effective nuclear charge and electronegativity, resulting in an increase in the work function of tungsten oxide [53], which is consistent with the characterization of UPS and KPFM mentioned earlier. As for the change in binding energy of Se 3d, a new peak can be observed at 59 eV after SOI modulation without annealing, representing the formation of Se-O bonds. This indicates that Se in WSe_2 forms bonds with O to form WO_xSe_y compounds. After annealing, the peak of the Se-O bond at 59 eV disappeared, indicating that the Se element no longer exists in an oxidized state after annealing. During the annealing process, WO_xSe_y is converted to WO_x, and the valence of the W element increases, resulting in an increase in the work function, which is consistent with the increase in the percentage content of W^{6+}. This phenomenon is consistent with the reported high-temperature decomposition of W-Se-O compounds [54].

We also characterized the Raman and PL spectra of WSe_2 during SOI modulation. As shown in Figure S7, it can be observed that the E^1_{2g} peak of the Raman spectrum of SOI modulation WSe_2 shows a blue shift, which is related to the increase in hole concentration of WSe_2 [55]. It can also be observed that a new broad peak appeared at 134 cm^{-1} after etching, which is consistent with the peak phase of WO_2 in [56]. For PL spectra, the peak intensity decreases significantly after SOI modulation, and the peak position shifted from 1.53 eV before annealing to 1.56 eV after annealing, representing the increase in hole concentration of WSe_2 [57].

Next, this work investigates the thermal stability of the SOI modulation metal-semiconductor interfaces. The SOI-WSe_2 transistors were annealed under Ar atmosphere at varying temperatures for 1 h and then tested at room temperature. The transfer characteristic curve is shown in Figure 4(a). As the annealing temperature increases, the hole on-state current of the device continues to increase, while the electron current continues to decrease. When the annealing temperature reaches 300°C, the on-state current reaches 1.45 μA. When the annealing temperature reaches 350°C, the off-state current reaches the lowest value of 1 pA. Moreover, when the annealing temperature reaches 400°C, the performance of the transistor does not significantly degrade. The output characteristic curve is shown in Figure S8. It can be seen that the output characteristic curve of the SOI modulation transistor annealed at 200°C saturates at a bias voltage of −0.2 V, while the saturation of the transistor annealed at 400°C shows a left shift and the output current increases significantly. For the mobility of transistors, as shown in Figure 4(b), the electron field-effect mobility gradually decreases with increasing annealing temperature, while the hole mobility reaches its highest value of 19 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 350°C and only slightly decreases at 400°C. Carrier polarity is an important indicator for measuring the carrier transport behavior of transistors. Here, we use the current ratio of I_{-80V} to I_{80V} to characterize carrier polarity, which represents the majority carrier type. As shown in Figure 4(c), it can be observed that with the increase of annealing temperature, I_{-80V}/I_{80V} continuously increases, indicating a clear process dominated by n-type transport to p-type transport. The threshold voltage also shifts to the right continuously with the increase of annealing temperature, representing the continuous increase of hole carrier concentration in WSe_2. Due to the rapid annealing at 400°C required by the BEOL process, the high-temperature stability of this metal-semiconductor contact interface proves that this method is compatible with the BEOL process and meets the conditions for building CMOS logic circuit integration.

To demonstrate the stability of this p-type modulation during long-term high-temperature treatment, the SOI-WSe_2 transistors were annealed in an Ar atmosphere at 300°C for varying durations. As shown in the transfer characteristic curve of Figure 4(d), it can be seen that increasing annealing time has almost no effect on the performance of SOI modulation transistors. Remarkably, the initial on-state current was preserved even after 10 h of annealing. The output characteristics curves presented in Figure S9 further confirm this stability, showing no significant variation with increasing annealing duration. These observations collectively indicate that the SOI modulation metal-semiconductor interface maintains robust ohmic contact characteristics across different annealing temperatures. The hole mobility at different annealing times shown in Figure 4(e) also exhibits small fluctuations. It is speculated that this fluctuation in mobility is caused by defects generated at the channel during the annealing process. Moreover, the polarity of carriers and the threshold voltage have a stable effect on the annealing time,

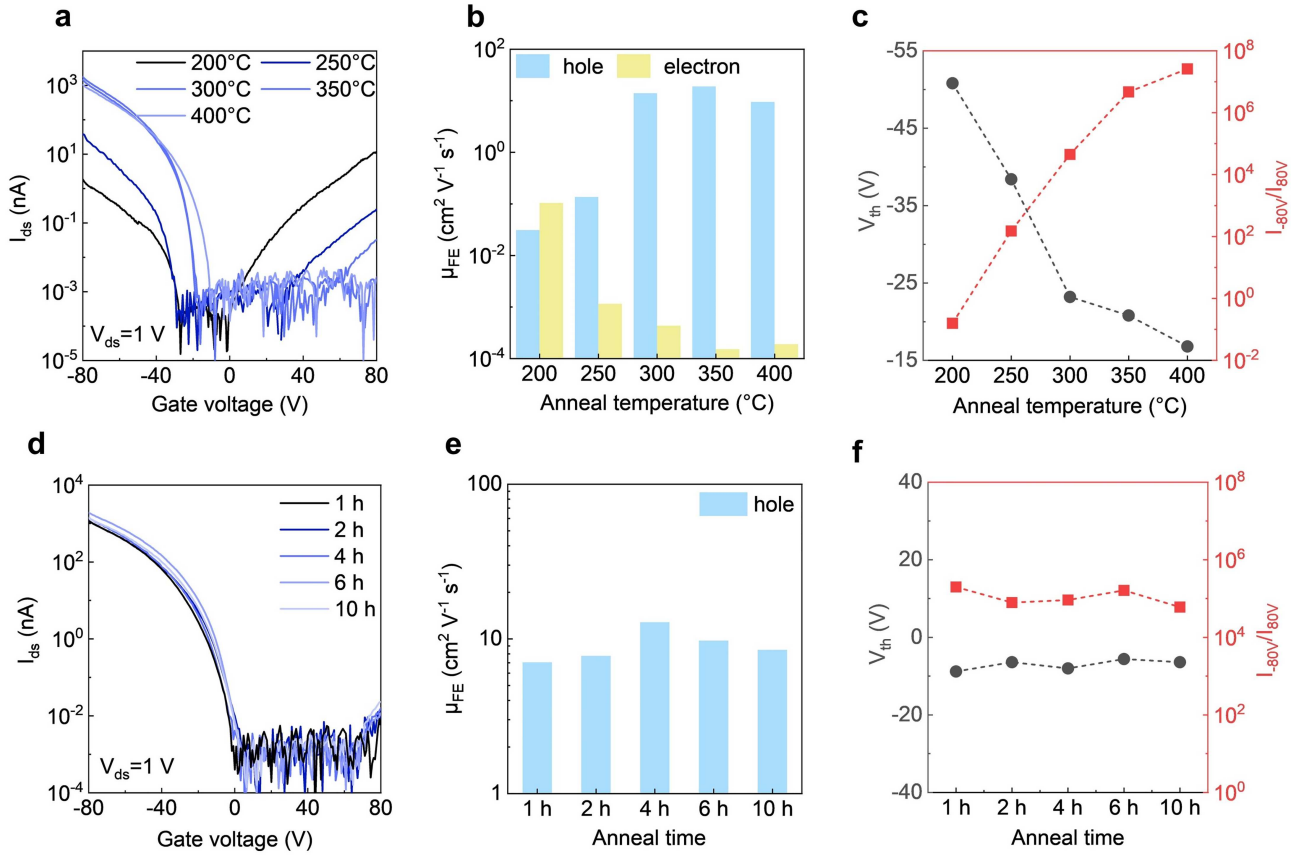

Figure 4 (Color online) Thermal stability characterization of SOI-WSe_2 transistors. (a) Transfer characteristic curve of SOI-WSe_2 transistors after 1 h annealing at different annealing temperatures; (b) mobility of SOI-WSe_2 transistors with annealing temperature; (c) threshold voltage and carrier polarity of SOI-WSe_2 transistors with annealing temperature; (d) transfer characteristic curves of SOI-WSe_2 transistor after annealing at 300°C for different times; (e) mobility of SOI-WSe_2 transistors with annealing time; (f) threshold voltage and carrier polarity of SOI-WSe_2 transistors with annealing time.

as shown in Figure 4(f). This highly stable threshold voltage is very advantageous for constructing CMOS logic circuits. Due to the excellent thermal stability of the WO_x buffer layer formed after annealing, this is also the reason why the p-type modulation effect of the transistor can be maintained stable with increasing annealing temperature.

Accurate control of carrier transport polarity is an essential process for constructing CMOS logic circuits on a single material. Compared to heterogeneous CMOS structures, homogeneous CMOS can achieve more uniform performance using simpler processes. Here, we demonstrate the construction of a WSe_2 homogeneous CMOS inverter based on the contact SOI modulation method, as shown in Figure S10(a). The p-FET of this inverter is constructed using the SOI contact modulation. n-FET is constructed by SOI modulation without annealing. The construction process of the CMOS inverter is to first perform the EOA process on the contact area of the p-FET, and finally construct the n-FET through Ar etching to complete the inverter construction. Figure S10(b) shows the transfer characteristic curves of p-FET and n-FET in the CMOS inverter, which demonstrates the implementation of high switching ratio and high subthreshold slope n-type and p-type modulation. The threshold voltages of the two transfer characteristic curves are both around −40 V with a small difference, achieving performance matching for p-FET and n-FET. Figures S10(c) and (d) show the voltage transfer characteristics curves and gain curves of the inverter under different voltage biases (V_{DD}). The inverter can achieve a clear logic output and fast switching between logic states. A gain of 1.2 can be achieved at V_{DD} = 5 V. Due to its compatibility with silicon-based processes and high potential for modulation uniformity, this p-type modulation method has great potential for constructing CMOS logic circuits.

4 Conclusion

In conclusion, we propose a p-type contact modulation method for WSe_2 with high performance and high thermal stability based on the etching-oxidation-annealing synergistic process. This modulation method achieves the

transition of the transport polarity of the WSe_2 transistor from n-type to p-type through spontaneous-oxidation-intercalation. We have revealed that the mechanism of the p-type modulation is the spontaneous oxidation of the contact area WSe_2 by Ar plasma etching with air to form an oxide buffer layer. After high-temperature annealing, the work function of the oxide layer increases, resulting in p-type modulation of the WSe_2. The SOI modulation transistor exhibits excellent p-type ohmic characteristics, with a Schottky barrier as low as 26.3 meV. This metal-semiconductor contact interface has very high stability, and the transistor can maintain almost nondecaying p-type modulation effect even after high-temperature annealing at 400°C. Long-term annealing at 300°C for 10 h can also ensure stable device performance. Finally, we also demonstrated the construction of a homogeneous CMOS inverter based on this modulation method on WSe_2. We believe that this highly thermally stable p-type modulation method, which is compatible with silicon-based processes, has great application value in the construction of 2D CMOS logic circuits.

Acknowledgements This work was supported by National Natural Science Foundation of China (Grant Nos. 52250398, 92463308, 62322402, 52188101, 52225206, 92163205, 52350301, 62204012, 52303362, 62304019, 52302162, 52402169), National Key Research and Development Program of China (Grant Nos. 2022YFA1203803, 2023YFF1500401), Beijing Nova Program (Grant Nos. 20220484145, 20230484478), and Young Elite Scientists Sponsorship Program by CAST (Grant No. 2022QNRC001).

Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Qiu H, Yu Z H, Zhao T G, et al. Two-dimensional materials for future information technology: status and prospects. Sci China Inf Sci, 2024, 67: 160400
2 Liu Y, Duan X, Shin H J, et al. Promises and prospects of two-dimensional transistors. Nature, 2021, 591: 43–53
3 Xu M S, Wang Y W, Liu J W, et al. Progress on the program of Si-compatible two-dimensional semiconductor materials and devices. Sci China Inf Sci, 2024, 67: 160401
4 Kim J, Park H, Yoo S H, et al. Defect-engineered n-doping of WSe_2 via argon plasma treatment and its application in field-effect transistors. Adv Mater Inter, 2021, 8: 2100718
5 Zhang X, Shao Z, Zhang X, et al. Surface charge transfer doping of low-dimensional nanostructures toward high-performance nanodevices. Adv Mater, 2016, 28: 10409–10442
6 Zhang X, Liao Q, Kang Z, et al. Hidden vacancy benefit in monolayer 2D semiconductors. Adv Mater, 2021, 33: 2007051
7 Tosun M, Chuang S, Fang H, et al. High-gain inverters based on WSe_2 complementary field-effect transistors. ACS Nano, 2014, 8: 4948–4953
8 Lee D, Choi Y, Kim J, et al. Recessed-channel WSe_2 field-effect transistor via self-terminated doping and layer-by-layer etching. ACS Nano, 2022, 16: 8484–8492
9 Ho P H, Chang J R, Chen C H, et al. Hysteresis-free contact doping for high-performance two-dimensional electronics. ACS Nano, 2023, 17: 2653–2660
10 Wang Y, Kim J C, Li Y, et al. P-type electrical contacts for 2D transition-metal dichalcogenides. Nature, 2022, 610: 61–66
11 Durán Retamal J R, Periyanagounder D, Ke J J, et al. Charge carrier injection and transport engineering in two-dimensional transition metal dichalcogenides. Chem Sci, 2018, 9: 7727–7745
12 Xiao J, Kang Z, Liu B, et al. Record-high saturation current in end-bond contacted monolayer MoS_2 transistors. Nano Res, 2022, 15: 475–481
13 Pendurthi R, Sakib N U, Sadaf M U K, et al. Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. Nat Nanotechnol, 2024, 19: 970–977
14 O'Brien K P, Naylor C H, Dorow C, et al. Process integration and future outlook of 2D transistors. Nat Commun, 2023, 14: 6400
15 Wu Y, Xin Z, Zhang Z, et al. All-transfer electrode interface engineering toward harsh-environment-resistant MoS_2 field-effect transistors. Adv Mater, 2023, 35: 2210735
16 Chou A-S, Wu T, Cheng C-C, et al. Antimony semimetal contact with enhanced thermal stability for high performance 2D electronics. In: Proceedings of IEEE International Electron Devices Meeting (IEDM), San Francisco, 2022
17 Liu Z Z, Zhang Q, Huang X H, et al. Contact engineering for temperature stability improvement of Bi-contacted MoS_2 field effect transistors. Sci China Inf Sci, 2024, 67: 160402
18 Liu Y, Guo J, Zhu E, et al. Approaching the Schottky-Mott limit in van der Waals metal-semiconductor junctions. Nature, 2018, 557: 696–700
19 Kong L, Zhang X, Tao Q, et al. Doping-free complementary WSe_2 circuit via van der Waals metal integration. Nat Commun, 2020, 11: 1866
20 Jung Y, Choi M S, Nipane A, et al. Transferred via contacts as a platform for ideal two-dimensional transistors. Nat Electron, 2019, 2: 187–194
21 Zhang X, Kang Z, Gao L, et al. Molecule-upgraded van der Waals contacts for Schottky-barrier-free electronics. Adv Mater, 2021, 33: 2104935
22 Song S, Yoon A, Jang S, et al. Fabrication of p-type 2D single-crystalline transistor arrays with Fermi-level-tuned van der Waals semimetal electrodes. Nat Commun, 2023, 14: 1–14
23 Zhang X, Yu H, Tang W, et al. All-van-der-Waals barrier-free contacts for high-mobility transistors. Adv Mater, 2022, 34: 2109521
24 Jang J, Ra H, Ahn J, et al. Fermi-level pinning-free WSe_2 transistors via 2D van der Waals metal contacts and their circuits. Adv Mater, 2022, 34: 2109899
25 Zhao B, Shen D, Zhang Z, et al. 2D metallic transition-metal dichalcogenides: structures, synthesis, properties, and applications. Adv Funct Mater, 2021, 31: 2105132
26 Zheng J, Miao T, Xu R, et al. Chemical synthesis and integration of highly conductive $PdTe_2$ with low-dimensional semiconductors for p-type transistors with low contact barriers. Adv Mater, 2021, 33: 2101150
27 Zou T, Kim H, Kim S, et al. High-performance solution-processed 2D p-type WSe_2 transistors and circuits through molecular doping. Adv Mater, 2023, 35: 2208934
28 Fang H, Chuang S, Chang T C, et al. High-performance single layered WSe_2 p-FETs with chemically doped contacts. Nano Lett, 2012, 12: 3788–3792
29 Yu L, Zubair A, Santos E J G, et al. High-performance WSe_2 complementary metal oxide semiconductor technology and integrated circuits. Nano Lett, 2015, 15: 4928–4934

30 Li H M, Lee D, Qu D, et al. Ultimate thin vertical p-n junction composed of two-dimensional layered molybdenum disulfide. Nat Commun, 2015, 6: 6564
31 Liu S Y, Xiong X, Wang X, et al. Hole mobility enhancement in monolayer WSe_2 p-type transistors through molecular doping. Sci China Inf Sci, 2024, 67: 160406
32 Zhang Y, Ma K, Zhao C, et al. An ultrafast WSe_2 photodiode based on a lateral *p-i-n* homojunction. ACS Nano, 2021, 15: 4405–4415
33 Liu L, Cai Z, Xue S, et al. A mass transfer technology for high-density two-dimensional device integration. Nat Electron, 2025, 8: 135–146
34 Ma Y, Liu B, Zhang A, et al. Reversible semiconducting-to-metallic phase transition in chemical vapor deposition grown monolayer WSe_2 and applications for devices. ACS Nano, 2015, 9: 7383–7391
35 Sung J H, Heo H, Si S, et al. Coplanar semiconductor-metal circuitry defined on few-layer $MoTe_2$ via polymorphic heteroepitaxy. Nat Nanotech, 2017, 12: 1064–1070
36 Empante T A, Zhou Y, Klee V, et al. Chemical vapor deposition growth of few-layer $MoTe_2$ in the 2H, 1T′, and 1T phases: tunable properties of $MoTe_2$ Films. ACS Nano, 2017, 11: 900–905
37 Li S, Ma Y, Ouedraogo N A N, et al. p-/n-type modulation of 2D transition metal dichalcogenides for electronic and optoelectronic devices. Nano Res, 2022, 15: 123–144
38 Xiong Y, Xu D, Feng Y, et al. P-type 2D semiconductors for future electronics. Adv Mater, 2023, 35: e2206939
39 Gao L, Chen Z, Chen C, et al. Silicon-processes-compatible contact engineering for two-dimensional materials integrated circuits. Nano Res, 2023, 16: 12471–12490
40 Liu B, Ma Y, Zhang A, et al. High-performance WSe_2 field-effect transistors via controlled formation of in-plane heterojunctions. ACS Nano, 2016, 10: 5153–5160
41 Smyth C M, Walsh L A, Bolshakov P, et al. Engineering the palladium-WSe_2 interface chemistry for field effect transistors with high-performance hole contacts. ACS Appl Nano Mater, 2019, 2: 75–88
42 Khan M A, Mehmood M Q, Massoud Y. High-temperature annealing effects on atomically thin tungsten diselenide field-effect transistor. Appl Sci, 2022, 12: 8119
43 Kim H, Park H, Lee G, et al. Intimate Ohmic contact to two-dimensional WSe_2 via thermal alloying. Nanotechnology, 2019, 30: 415302
44 Chen J, Wang Q, Sheng Y, et al. High-performance WSe_2 photodetector based on a laser-induced p-n junction. ACS Appl Mater Interfaces, 2019, 11: 43330–43336
45 Nipane A, Choi M S, Sebastian P J, et al. Damage-free atomic layer etch of WSe_2: a platform for fabricating clean two-dimensional devices. ACS Appl Mater Interfaces, 2021, 13: 1930–1942
46 Kwon G, Choi Y H, Lee H, et al. Interaction- and defect-free van der Waals contacts between metals and two-dimensional semiconductors. Nat Electron, 2022, 5: 241–247
47 Kong L, Wu R, Chen Y, et al. Wafer-scale and universal van der Waals metal semiconductor contact. Nat Commun, 2023, 14: 1014
48 Sotthewes K, van Bremen R, Dollekamp E, et al. Universal Fermi-level pinning in transition-metal dichalcogenides. J Phys Chem C, 2019, 123: 5411–5420
49 Kong L, Liu H, Wang X, et al. Precisely tailoring WSe_2 polarity via van der Waals bismuth-gold modulated contact. Nano Lett, 2024, 24: 10949–10956
50 Cho H, Sritharan M, Ju Y, et al. Se-vacancy healing with substitutional oxygen in WSe_2 for high-mobility p-type field-effect transistors. ACS Nano, 2023, 17: 11279–11289
51 Chiang C C, Lan H Y, Pang C S, et al. Air-stable p-doping in record high-performance monolayer WSe_2 devices. IEEE Electron Device Lett, 2022, 43: 319–322
52 Le H V, Le Cerf D. Colloidal polyelectrolyte complexes from hyaluronic acid: preparation and biomedical applications. Small, 2022, 18: 2204547
53 Greiner M T, Chai L, Helander M G, et al. Transition metal oxide work functions: the influence of cation oxidation state and oxygen vacancies. Adv Funct Mater, 2012, 22: 4557–4568
54 Soloviev A A, Grigoriev S N, Fominski D V, et al. Structural and electrochemical properties of W-Se-O layers prepared by pulsed laser pre-deposition and thermal posttreatment. J Phys-Conf Ser, 2016, 747: 012046
55 Kang D H, Shim J, Jang S K, et al. Controllable nondegenerate p-Type doping of tungsten diselenide by octadecyltrichlorosilane. ACS Nano, 2015, 9: 1099–1107
56 Liu Y, Tan C, Chou H, et al. Thermal oxidation of WSe_2 nanosheets adhered on SiO_2/Si substrates. Nano Lett, 2015, 15: 4979–4984
57 Chen S, Zhang Y, King W P, et al. Extension doping with low-resistance contacts for p-type monolayer WSe_2 field-effect transistors. Adv Electron Mater, 2025, 11: 2400843