

# A 1-10 GHz frequency-agile high-power GaN linear photoconductive semiconductor switch

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## Appendix A Material information and device fabrication process

Fe-doped GaN was grown by the hydride vapor phase epitaxy (HVPE) (Suzhou Nanowin Science and Technology Co., Ltd). The wafer size is  $\Phi$  50.78 mm, the thickness is 350  $\mu\text{m}$ , the surface orientation (0001) toward  $A$ -axis  $0.01^\circ \pm 0.12^\circ$  and  $M$ -axis  $0.34^\circ \pm 0.1^\circ$ , the surface state is double-side-polished, and surface roughness  $R_a < 0.3$  nm. The doping concentrations of Fe, Si and O measured by secondary ion mass spectrometry (SIMS) were  $3.73 \times 10^{18} \text{ cm}^{-3}$ ,  $7.38 \times 10^{17} \text{ cm}^{-3}$  and  $1.51 \times 10^{16} \text{ cm}^{-3}$  (Suzhou Weifen Technology Co., Ltd). The resistivity of 2" SI-GaN:Fe measured by contactless measurement is  $2.2 \times 10^8 \Omega\text{-cm}$ . The fabrication process of the lateral GaN PCSS with shallow trench is as follows. Firstly, the photoresist is used as a mask to selectively etch GaN to form the shallow trenches via inductively coupled plasma etcher, with dimensions of  $4 \times 2$  mm and a depth of 1  $\mu\text{m}$ , separated by a horizontal gap of 1.5 mm. Secondly, multi-layer metals (Ti/Al/Ni/Au: 20/160/55/45 nm) were deposited in the trenches by electronic beam evaporation, and annealed at 860  $^\circ\text{C}$  in nitrogen atmosphere for 1 min to form an ohmic contact. Thirdly, Ti/Au (50/500 nm) was deposited to fill the trenches by RF magnetron sputtering. Finally, a 200 nm  $\text{Si}_3\text{N}_4$  passivation layer was deposited on the GaN surface using plasma-enhanced chemical vapor deposition to prevent surface flashover and breakdown.

## Appendix B Breakdown voltage under different doping concentrations

We prepared two GaN samples with different Fe doping concentrations, named GaN-1 and GaN-2. SIMS test results are shown in Figure B1. Fe doping concentration of GaN-1 is  $3.73 \times 10^{18} \text{ cm}^{-3}$ , while GaN-2 is  $1.49 \times 10^{19} \text{ cm}^{-3}$ . Next, we used the UHV SMU (Keysight B1505A) to test the high voltage performance of GaN-1 and GaN-2. The evolution of the leakage current with the voltage is shown in Figure B2. Neither GaN-1 nor GaN-2 experience breakdown at 10 kV. The results show GaN-2 with higher Fe doping concentration has lower leakage current compared with GaN-1. We think a higher Fe doping concentration is beneficial to improving the breakdown electric field of the device in the bias range of 0-10 kV.

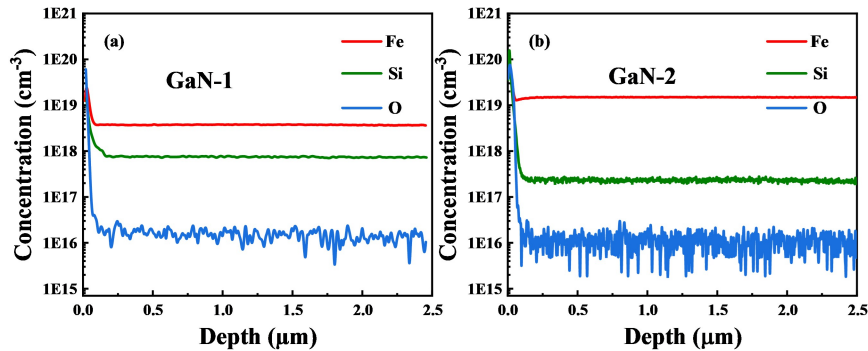
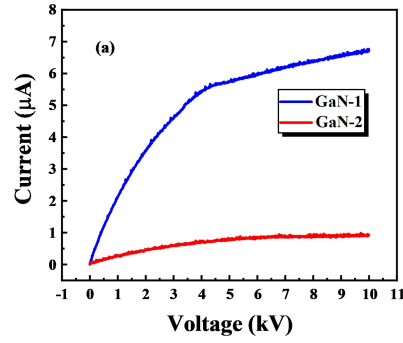


Figure B1 SIMS of (a) GaN-1, and (b) GaN-2.

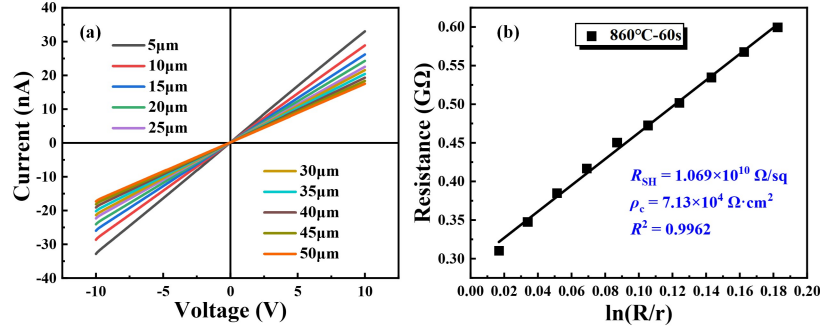
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**Figure B2** Leakage current test of GaN-1 and GaN-2.

### Appendix C Analysis of ohmic contact performance of semi-insulating GaN

We used the circular transfer length method (CTLM) to measure specific contact resistivity ( $\rho_c$ ). The gap spacings between the inner and outer circles range from 5 to 50  $\mu\text{m}$ , while maintaining the outer circle's radius at 300  $\mu\text{m}$ . Figure C1 shows the electrical characteristics for the SI-GaN ohmic contact annealed at 860  $^{\circ}\text{C}$ , 60s. The current-voltage (I-V) characteristics were measured using a semiconductor parameter analyzer (Keithley 4200) at room temperature. The I-V curves exhibit good linearity, and their slopes show reasonable variations for different electrode spacings, indicating the forming of Ohmic contact. Figure C1(b) shows the sheet resistance  $R_{SH}=1.069\times 10^{10}$   $\Omega/\text{sq}$  and specific contact resistivity  $\rho_c=7.13\times 10^4$   $\Omega\cdot\text{cm}^2$ , with a determination coefficient  $R^2=0.9962$ . The specific contact resistivity is certainly much higher than conventional GaN devices such as HEMT, SBD as so on. We think that the higher  $\rho_c$  and  $R_{SH}$  is ascribed to the extremely low carrier concentration and high bulk resistivity of SI-GaN.



**Figure C1** (a) I-V characteristics of CTLM annealed at 860  $^{\circ}\text{C}$  for 1 minute. (b) Linear fitting of Resistance versus  $\ln(R/r)$ .

### Appendix D Microwave experimental circuit

The test circuit includes a DC voltage source adjustable from 0 to 10 kV and a 10 nF energy storage capacitor. When the modulated laser beam triggers the PCSS, the capacitor begins to discharge through it. The input signal is a 532 nm modulated laser with a pulse envelope width of 50 ns, an adjustable energy range of 1 to 8 mJ and a 1-10 GHz frequency-agile range. The fabricated GaN PCSS is mounted on a microstrip circuit board. After the laser beam triggers, the output electrical signals with different response frequencies are attenuated by a 60 dB coaxial attenuator and then fed into a directional coupler. A digital oscilloscope is used to characterize the output microwave signal.

### Appendix E Effects of parasitic parameters on high frequency signals

A circuit simulation model was established using ADS software. Specifically, we analyzed possible parasitic parameters coming from device packaging, microstrip line test board, bonding wires and so on. Figure E1 shows the schematic of ADS circuit simulation. The bias voltage is 3 kV and the signal source frequency is 10 GHz. The parasitic capacitance of device can be obtained by electromagnetic simulation software as shown in Figure E2. Four groups of simulation parameter designs were carried out according to the research content, as shown in Table E1. The simulation waveforms are shown in Figure E3. We find that the output voltage and modulation depth of the device decrease as the amount of introduced parasitic parameters increases. We list the specific data results and remarks in Table E1. These results show that parasitic inductance and capacitance introduced by bond wires and device packaging might be main issues hindering high-frequency

signal transmission, increasing energy loss, and reducing high-frequency response capabilities. In future, shortening the length of the bonding wires, reducing the distance of the output transmission line, and selecting low dielectric constant material packaging are needed to reduce parasitic parameters, for better transmission of high-frequency signals.

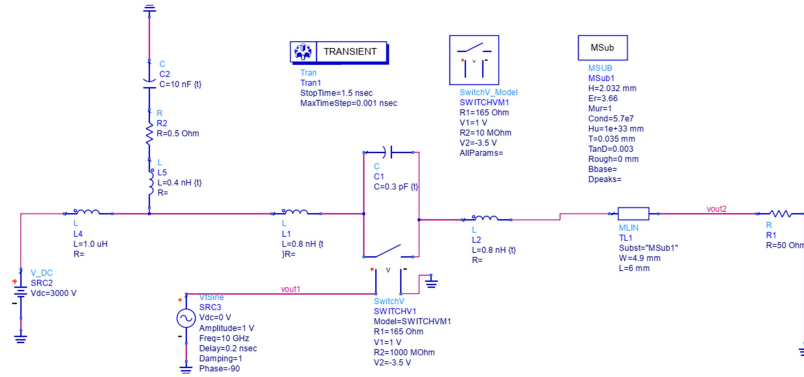


Figure E1 Schematic of ADS circuit simulation.

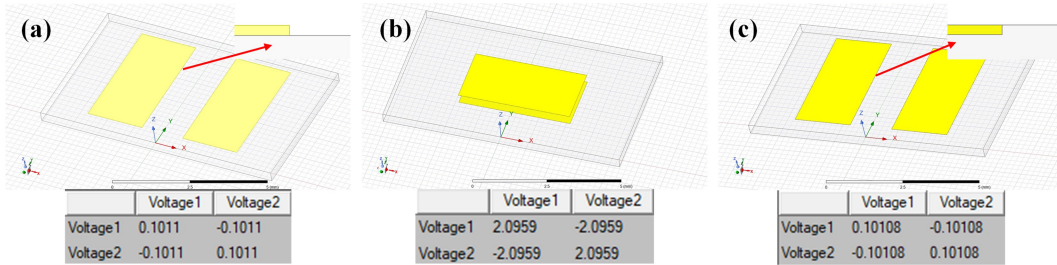


Figure E2 Electromagnetic simulations of different structures. (a) Lateral PCSS. (b) Vertical PCSS. (c) Shallow Trench PCSS.

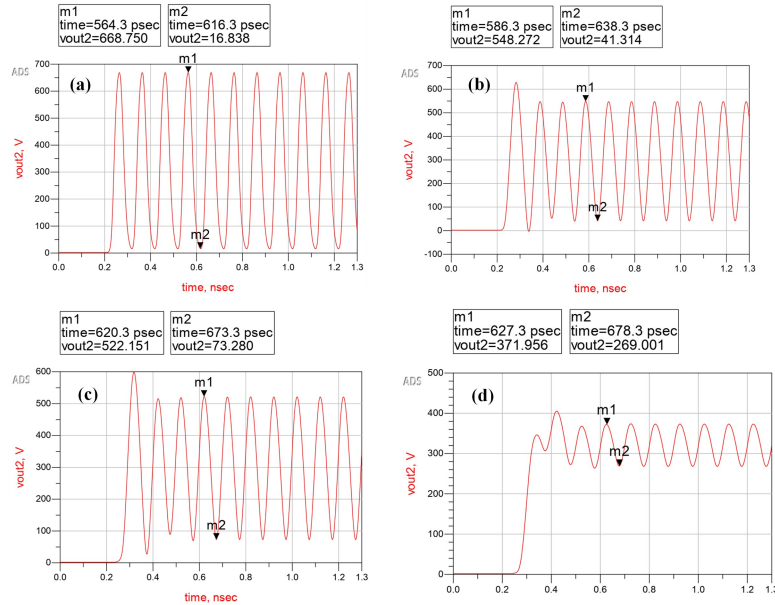


Figure E3 Output voltage waveforms of (a) Group 1. (b) Group 2. (c) Group 3. (d) Group 4.

Table E1 SIMULATION PARAMETERS AND RESULTS

|                            | L1/L2 (nH) | TL1 | C1 (pF) | Results                                   | Remarks                                        |
|----------------------------|------------|-----|---------|-------------------------------------------|------------------------------------------------|
| Group 1 (idea)             | 0.1/0.1    | N   | 0.3     | Vmax=668.75 V<br>Modulation depth=97.48%  | /                                              |
| Group 2 (bonding wires)    | 0.8/0.8    | N   | 0.3     | Vmax=548.272 V<br>Modulation depth=92.46% | Decreased by ~18%<br>(compared with Group 1)   |
| Group 3 (microstrip line)  | 0.8/0.8    | Y   | 0.3     | Vmax=522.151 V<br>Modulation depth=85.97% | Decreased by ~4.8%<br>(compared with Group 2)  |
| Group 4 (device packaging) | 0.8/0.8    | Y   | 1       | Vmax=371.956 V<br>Modulation depth=27.68% | Decreased by ~28.8%<br>(compared with Group 3) |