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Variation-aware optimization of salicide-enhanced tunnel FET technology based on 300 mm foundry platform

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It is difficult for traditional MOSFET devices to reduce the off-state current ($I_{\rm OFF}$) and operating voltage ($V_{\rm DD}$) when the technology node is scaled down due to short-channel effects, gate-induced drain leakage (GIDL), and the theoretical limit of subthreshold swing. Besides affecting power consumption, the impact of device variability also increases as the technology node scales down, thereby limiting the scaling down of $V_{\rm DD}$ and further restricting power reduction. Compared with MOSFET, the Si tunnel FET (TFET) has a gate-controlled p–i–n structure and band-to-band tunneling (BTBT) mechanism, and it exhibits lower $I_{\rm OFF}$ and $V_{\rm DD}$, enabling a considerable reduction in power consumption [1]. Moreover, the Si-TFET has been shown to have better CMOS compatibility, scalability, and reliability than emerging device technologies. A novel complementary dopant-segregated TFET (C-DS-TFET) was recently proposed and monolithically integrated with baseline CMOS technology on a 12-inch foundry platform; it achieved a record $I_{\rm ON}/I_{\rm OFF}$ ratio among TFETs manufactured by industry without incurring a performance penalty with CMOS devices [2]. Additionally, a sub-100 nA ultralow leakage MCU embedded with a 1 kbit TFET-gated-ground static random-access memory (TGG-SRAM) [2] was successfully fabricated on the same foundry platform, and this demonstrated that Si-TFETs have great potential to reduce power consumption in large-scale integrated circuits. However, while dopant-segregation technology enhances the TFET performance, it also introduces additional variation sources into the DS-TFET [3], compromising its low-power advantages. Therefore, co-optimizing the performance variability of DS-TFETs is critically important.

In this study, the impact of process conditions on the variability of DS-TFET and the optimization strategies are thoroughly investigated. Source ion implantation with lower energy and higher dose as well as a thicker silicide layer is recommended according to the device structure and dopant-segregation mechanism. Through co-optimizing the variability and performance of DS-TFET, an optimized process flow with an isolation well and last self-aligned silicide block (SAB) process is also proposed. This study provides a variation-aware optimization direction for DS-TFET, paving the way for reducing power in ultra large-scale integrated circuits.

Fabrication of DS-TFETs. The DS-TFET is designed with a self-aligned dopant-segregated source junction for high $I_{\rm ON}$ and a drain underlap region for low $I_{\rm OFF}$ through an asymmetrical gate spacer as shown in Figure 1(a). To increase the doping concentration of the TFET source extension region and reduce the thermal budget of the TFET, the MOSFET lightly doped drain (LDD) implantation process is separated from it. To self-align the dopant-segregation junction with the gate edge, the ON spacer at the source side of TFET is removed before the ion implantation and annealing process for the source and drain extension regions of TFET. Prior to conducting the silicide process, an SAB process is required to fabricate the mask layer for devices with high resistance. Finally, the silicide process is performed to form the contact layer and dopant-segregated junction.

Experimental results. Figure 1(b) compares the measured $I_{\rm ON}$ distributions in conventional TFETs and DS-TFETs employing different process conditions. Although dopant-segregation technology can improve the performance of the TFET, it also introduces additional variation sources, resulting in larger variability. Though modulating the ion implantation conditions, variability in DS-TFETs can be suppressed as demonstrated in Figure 1(c). However, the DS-TFETs with small variability in Figure 1(c) also exhibit lower on-state currents. Because of the dopant segregation effect [2], the peak position of the dopant profile can be pushed to the NiSi/Si junction. Therefore, the variation of $I_{\rm ON}$ can originate from three dominant sources as shown in Figure S1. The peak position of the segregated dopant profile is affected by the roughness of the NiSi/Si junction ($\sigma L_{\rm junc}$), which is determined by the variation of offset spacer thickness at the source side ($\sigma L_{\rm spac}$) and the variation of the lateral extension length of NiSi ($\sigma L_{\rm NiSi}$). The segregated dopant concentration profile is related to both the peak dopant concentration ($N_{\rm A,MAX}$) and the doping gradient of the dopant profile (DG). The variation of the TDG at the gate edge of DS-TFET is thus dominated by $\sigma N_{\rm A,MAX}$, $\sigma L_{\rm junc}$, and

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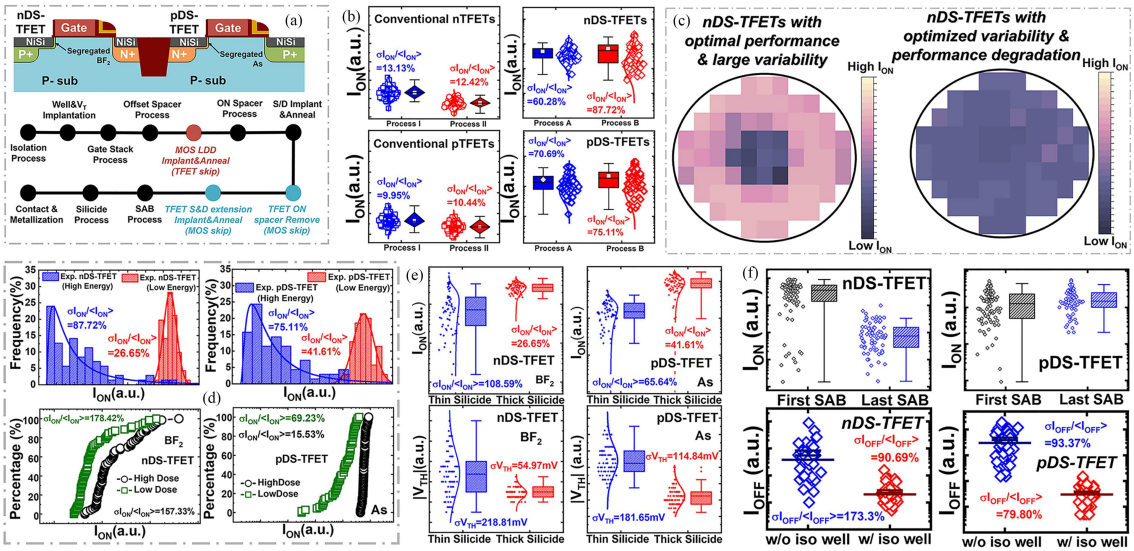

Figure 1 (Color online) (a) Device schematic and process flow of DS-TFET; (b) measured I_{ON} distributions in TFETs and DS-TFETs with different process conditions; (c) measured I_{ON} of nDS-TFETs across 12-inch wafer; (d) measured I_{ON} distributions with different implantation energies and doses; (e) measured V_{TH} and I_{ON} distributions with different NiSi thicknesses; (f) measured I_{ON} distributions from the "First SAB" and "Last SAB" processes, and I_{OFF} distributions w/ & w/o isolation well.

σDG

Lower implantation energy and higher implantation dose result in higher doping concentration near the silicon surface. This leads to a pocket layer with higher doping concentration at the NiSi/Si junction near the channel surface, which can suppress the impact of the random dopant fluctuation [4]. Therefore, source ion implantation with lower energy and higher dose is recommended for enhancing device performance and suppressing variability as shown in Figure 1(d). When the source overlaps with the gate in DS-TFET, the effect of σL_{junc} and σDG can be eliminated because the gate electric field can directly control the tunnel junction at the peak dopant position. Therefore, a thicker silicide layer can suppress DS-TFET variability due to the smaller source underlap length or it can even help to achieve the source overlap region as shown in Figure 1(e). Since a smaller source underlap length can also enhance gate controllability and the source doping concentration at the gate edge, a thicker silicide layer is also recommended to enhance device performance

The SAB process is used to form a hard mask for high-resistance devices on the same wafer where the NiSi is not required. However, as shown in Figure S2, a residual SAB mask due to incomplete etching may adhere to the gate spacer at the source side of DS-TFET. This residual hard mask can act as the hard mask for ion implantation and NiSi formation of the source tunnel junction. If the SAB process is performed before the removal of the ON spacer as shown in the case of "First SAB", the spacer etching process can remove the residual SAB mask, thereby reducing the source underlap length and enhancing device performance. Nevertheless, both the implantation of the source extension region and the lateral extension of the NiSi will be affected by the residual SAB mask, resulting in larger variability as shown in Figure 1(f). If the SAB process is performed following the formation of the source and drain extension regions of the TFET as shown in the case of "Last SAB", only the lateral extension of NiSi is affected by the residual SAB mask. The process flow in the case of "Last SAB" will then result in suppressed variability but also slightly lower I_{ON} as shown in Figure 1(f).

As the bulk Si-based TFET is a three-terminal device fabricated on a lightly doped substrate, a parasitic current path exists between the substrate and the source/drain regions that have the same doping type as the substrate [5]. This parasitic current path can be suppressed by fabricating an isolation well under the TFET [5]. As shown in Figure 1(f), the suppression of this parasitic current path can also suppress variations in the off-state current.

Conclusion. This work thoroughly investigates the impact of process conditions on the variability of DS-TFETs. Optimization strategies, such as source ion implantation with lower energy and higher dose, a thicker silicide layer, process integration with an isolation well, and a last SAB process, are recommended for co-optimizing variability and performance. This work provides a variation-aware optimization direction for DS-TFETs, facilitating the application of DS-TFETs in large-scale low-power circuits.

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Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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