Supplementary Material

This supplementary material presents the mentioned schematic of variation sources and process flow from the main text.

As mentioned in the main text, the doping gradient of source tunnel junction (TDG) in DS-TFET is located at the gate edge after dopant segregation. Therefore, the variation of TDG can originate from three dominant sources as shown in Fig. S1. The peak position of the segregated dopant profile is affected by the roughness of the NiSi/Si junction (σL_{junc}), which is determined by the variation of offset spacer thickness at source side (σL_{spac}) and the variation of the lateral extension length of NiSi (σL_{NiSi}). The segregated dopant concentration profile is related to both the peak dopant concentration ($N_{A,MAX}$) and the doping gradient of the dopant profile (DG). The variation of the TDG at the gate edge of DS-TFET is thus dominated by $\sigma N_{A,MAX}$, σL_{junc} and σDG.

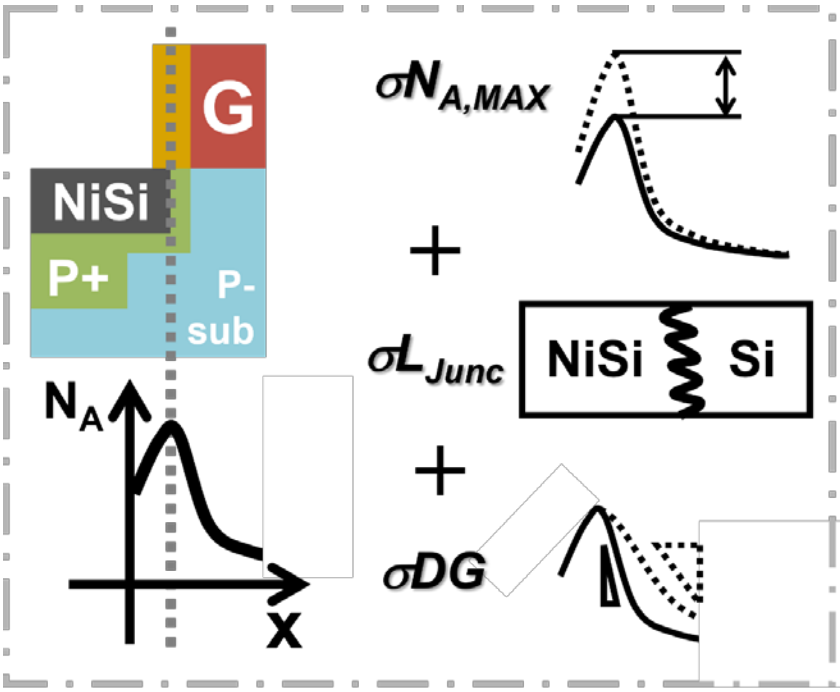

Figure S1. Schematic of the variation sources of the dopant segregated tunnel junction.

As mentioned in the main text, the SAB process is used to form hard mask for high-resistance devices on the same wafer where NiSi is not required. However, as shown in Fig. S2, residual SAB mask due to incompletely etching may adhere to the gate spacer at the source side of DS-TFET. This residual hard mask can act as the hard mask for ion implantation and NiSi formation of source tunnel junction. If SAB process is performed before the removal of ON spacer as shown in the case of "First SAB", the spacer etching process can remove the residual SAB mask, thereby reducing the source underlap length and enhancing the device performance.

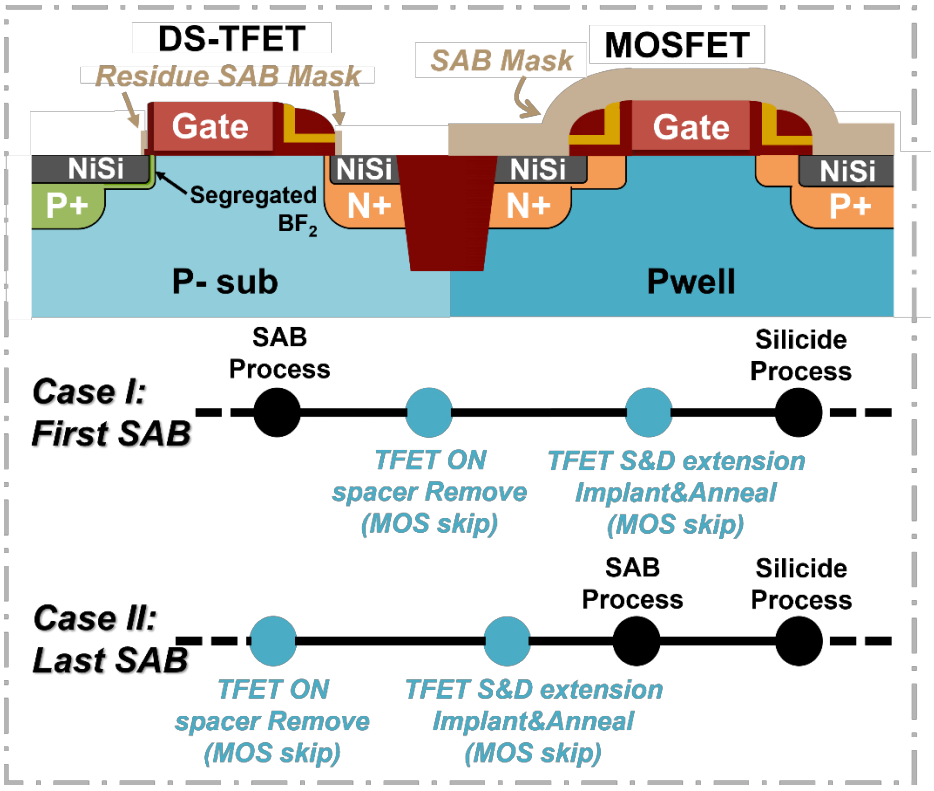

Figure S2. Schematic of DS-TFET with residue SAB mask and the process flow of "First SAB" & "Last SAB".