SCIENCE CHINA
Information Sciences

• PERSPECTIVE •

December 2025, Vol. 68, Iss. 12, 226401:1–226401:3
https://doi.org/10.1007/s11432-025-4590-5

IC + AI: a no-human-in-loop design paradigm?

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Received 23 July 2025/Accepted 10 September 2025/Published online 24 October 2025

Citation Liu C J, Yang J. IC + AI: a no-human-in-loop design paradigm? Sci China Inf Sci, 2025, 68(12): 226401, https://doi.org/10.1007/s11432-025-4590-5

Integrated circuit (IC) design has long been constrained by two critical pain points: exorbitant labor costs and protracted R&D cycles, which are increasingly becoming the primary bottlenecks for innovation in this field. The development of a complex chip typically involves hundreds of engineers working collaboratively over a timeframe of 12 to 24 months. Each phase of the development process, including digital architecture design, register-transfer level (RTL) coding, verification, and physical implementation in the digital domain, as well as analog circuit topology selection, transistor-level implementation, and layout generation in the analog domain-relies heavily on the expertise of senior engineers [1,2]. In addition, the reuse rate of existing circuits remains extremely low. Under new process nodes or new specification requirements, circuits need to be redesigned, which further consumes a significant amount of human resources. These prohibitive design costs and extended development timelines have emerged as the foremost constraints on IC design innovation. The root cause lies in the stagnation of electronic design automation (EDA) methodologies amid the exponential growth of chip design complexity. Digital design still adheres to the last century's logic synthesis and IP reuse paradigms, while analog design methodology has seen no fundamental evolution. This stagnation has long been recognized by both academia and industry. The intelligent design of electronic assets (IDEA) program funded by DARPA [3] attempted to address this by developing a general-purpose compiler for "human-out-of-the-loop" chip design, but no groundbreaking progress has been achieved to date.

The prolonged development cycle and sluggish performance improvement of AI chips are increasingly becoming the bottleneck that hinders the rapid development of artificial general intelligence (AGI). From a technological evolution perspective, AGI primarily relies on the iterative progress of AI chips, AI models, and data. An ideal technological ecosystem requires the establishment of a closed-loop characterized by "AI designs chips – chips train new generation AI". Within this framework, an AI model endowed with autonomous learning capabilities can automatically complete complex tasks in chip design through massive historical design data, breaking through the cognitive limitations of human engineers when dealing with billion-gate-level circuits and achieving great improvements in chip performance. In turn, high-performance AI chips facilitate the training of more powerful large language models (LLMs). However, at present, the improvement in computing capability facilitated by the advancement of semiconductor technology remains relatively limited. At the same time, the current research and development speed of AI chips is extremely slow, and AI chips have become the weakest link in the evolution of AGI [4].

Therefore, integrating AI, particularly LLMs, throughout the entire chip design process not only addresses current pain points in chip development but also represents the key to unlocking a new era of AI.

Opportunities. The novel capabilities introduced by LLMs are creating unprecedented opportunities. While traditional electronic design automation (EDA) tools have automated critical aspects of chip design, enabling the design of million-gate-level circuits, the knowledge-intensive core tasks still require significant human intervention. Currently, LLMs are driving transformative advancements across at least three key dimensions:

Firstly, LLMs serve as a powerful tool for knowledge representation, extraction, and organization. In the field of IC design, data often includes structured, semi-structured, and unstructured documents. Faced with a vast amount of design documents, millions of lines of hardware description language (HDL) code, extensive simulation and verification reports, complex physical design constraints, and dynamically updated process library files and other multi-source and heterogeneous data, traditional methods are often inadequate. Endowed with deep semantic understanding and cross-modal pattern recognition capabilities, LLMs can efficiently and accurately represent, extract, and organize various knowledge elements from complex, multi-source, heterogeneous, and multi-modal data [5], and can even transform them into a computable system for simulation [6].

Secondly, LLMs can solve complex optimization problems

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within the natural language framework. Traditional EDA optimization methods require prior modeling: transforming engineering problems into formal optimization problems, and then finding an appropriate solver. However, numerous challenges in circuit design are difficult to model precisely. For example, many practical design scenarios in analog circuits are beyond the scope of traditional optimization methods. On the one hand, LLMs can be regarded as a kind of heuristic algorithm to a certain extent. Their capabilities can be further enhanced through the evolutionary-algorithm paradigm, enabling them to achieve optimization capabilities comparable to those of human engineers [7]. On the other hand, LLMs can also generate targeted optimization algorithms, which can be directly used to solve large-scale engineering problems [8].

Finally, models trained with reinforcement learning (RL) are also effective means for reasoning about professional and complex knowledge. DeepSeek R1 [9] has demonstrated that, through RL, it is possible to handle high-dimensional and complex knowledge reasoning, and that such models have reached the proficiency level of senior engineers in terms of mathematical and coding abilities. The same principle is applicable to the field of circuit design: by leveraging RL, models can mimic the decision-making processes of human experts. Specifically, they can learn optimal solutions within extensive design spaces through repeated trial-and-error, autonomously explore extreme verification scenarios during functional verification, predict potential functional failures, and significantly accelerate both the convergence of chip design processes and breakthroughs in chip performance.

The aforementioned tasks of knowledge summarization, optimization, and decision-making, which were mainly done by engineers before, can now be carried out by LLMs. Therefore, in the future, it may be possible to build a truly no-human-in-the-loop IC design environment based on LLMs.

Challenges. First, the hallucination problem of LLMs [10] and their inherent instability conflict with the high-precision requirements of chip design. For example, LLMs may generate digital or analog circuits that violate fundamental circuit principles. Moreover, due to the absence of a traceable logical explanation in the LLM's decision-making process, such errors are often difficult to locate and rectify. A possible solution is to combine LLM decision-making with EDA tool simulation. In IC design, transistor-level simulation can ensure functional correctness, while physical verification can guarantee compliance with manufacturing specifications. This forms a closed-loop system encompassing data generation, automated verification, and quality annotation, thereby ensuring the accuracy of the LLM-generated results.

Second, the acute data scarcity challenge in the circuit domain [11] conflicts with the massive data requirements of LLMs. Circuit-related data is predominantly stored in unstructured formats like expert knowledge and technical documents, posing significant challenges for structured parsing. Compounded by stringent industrial confidentiality requirements, intellectual property protections, and the absence of an open-source culture, inter-enterprise data remains highly siloed. A possible solution is to establish a simulation-based data flywheel system and build a labeled dataset through massive simulations. This forms a closed-loop system of data generation, automated verification, and quality annotation, effectively generating a large number of verified datasets.

Third, LLMs are only suitable for making top-level decisions within a natural language environment, which is in conflict with the need for detailed operations in chip design. LLMs are only proficient in knowledge extraction, understanding, and generation based on natural language, but have poor capabilities when dealing with detailed numerical or image data, which are common data types in circuit design [12, 13]. This means that LLMs alone cannot achieve precise control over IC design tools and thus cannot enable end-to-end circuit design. A suitable approach is to have LLMs assume the role of decision-makers, in conjunction with many basic customized point tools, such as optimization algorithms [14, 15], or other multi-modal AI models for front-end embedding [16, 17] and back-end generation [18]. The combination of LLMs and basic AI systems can automate more complex circuit-design processes.

Applications. LLMs demonstrate unparalleled potential in revolutionizing IC design, particularly in domains that have historically relied on intensive human expertise. The following breakthrough areas are poised for transformation.

LLM-driven complex logic circuit verification. Traditional RTL verification demands extensive manual effort to develop test cases across diverse scenarios, often creating bottlenecks in CPU, GPU, and communication chip development. Future LLM-based solutions will enable: the interpretation of design specifications to automatically generate verification cases; the debugging of RTL code through human-like logical reasoning [19]; the execution of functional safety analysis for critical applications (e.g., automotive electronics); and the integration of diverse extreme verification scenarios within the design space to achieve fully automated exploratory verification.

LLM-empowered exploration and optimization of high-performance processor architectures. The design of high-performance processor architectures depends on many implementation details, as well as the trade-offs made by architecture designers. LLMs will achieve automatic design in high-performance processor architectures [20–22]. By learning from historical architecture data, LLMs can build the relationships among design knowledge, architecture parameters, and performance in the design space. Compared with traditional trial-and-error design methods, LLMs not only rapidly generate high-potential architecture solutions based on existing design experience but also predict the performance under different workloads. This enables intelligent decision-making in key aspects such as micro-architecture parameter adjustment, cache hierarchy optimization, and instruction set expansion.

LLM-driven automated analog circuit design. Traditional analog circuit design suffers from extremely low automation, with critical aspects, including topology selection and layout design, relying heavily on manual iteration [2]. Future LLM-based solutions will revolutionize this field by: (1) knowledge extraction: analyzing vast design documents and simulation reports to construct comprehensive circuit knowledge graphs [23–26]; (2) intelligent layout: converting expert knowledge (e.g., common-centroid matching) into executable layout constraints for agile implementation [27]; (3) parasitic-aware design: proactively compensating for layout-induced performance degradation during schematic design by anticipating parasitic effects.

LLM-driven high-level logic synthesis. Traditional logic synthesis methods convert RTL code into gate-level circuits [28–30] while balancing the three metrics of performance, power, and area (PPA). However, due to the vast search space, these methods cannot find the globally optimal so-

lution, resulting in unnecessary sacrifices in PPA. With the help of LLMs, it is promising to enable the learning of the relationship between circuit functions and underlying gate-level circuits. Combined with the process information in the process library, LLMs can predict the logic synthesis methods suitable for specific algorithms and application scenarios, thus achieving a better PPA trade-off point that better aligns with application scenarios.

Shift left in the design and verification procedure. The circuit design process is long-chained, making it difficult to directly predict downstream circuit design indicator results during upstream design links. For example, in digital circuit design, it is hard to predict the area and power consumption of the back-end layout at the RTL stage. Traditional AI models [31–33], limited by data formats and differences in circuit representation methods between different stages, can usually only predict in some parts of the process. They lack generality and cannot be flexibly combined with the actual application scenarios of circuits. However, the large circuit model (LCM) [16], trained with substantial multimodal data from various circuit design stages, holds the promise of achieving multimodal data alignment across all stages. It also shows great potential in learning from existing circuit design history libraries and multimodal information, such as circuit netlists and layout information. Thus, LCMs can predict downstream results in the upstream design process, achieving shift-left in the design and verification procedure, greatly improving the iterative optimization efficiency of circuit design.

In summary, LLMs are expected to leverage their advantages in knowledge organization, complex problem optimization, and professional knowledge reasoning to realize human-free circuit design.

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