SCIENCE CHINA
Information Sciences

• RESEARCH PAPER •

December 2025, Vol. 68, Iss. 12, 220305:1–220305:10
https://doi.org/10.1007/s11432-025-4651-9

Special Topic: Terahertz Communications for 6G and Beyond: How Far Are We?

A 285–310 GHz four-channel transceiver with 22.6 dBm EIRP supporting 64QAM modulation in 130-nm SiGe process

Si-Yuan TANG[1†], Zekun LI[1†], Sidou ZHENG[1], Zheng YAN[1], Yuxiang LU[1], Dawei TANG[1], Jiayang YU[1], Rui ZHOU[1], Chen-Yu DING[1], Wentao ZHU[1], Peigen ZHOU[1*], Zhe CHEN[1*], Pinpin YAN[1], Jixin CHEN[1,2*] & Wei HONG[1,2]

[1]*State Key Laboratory of Millimeter Waves, Southeast University, Nanjing 210096, China*
[2]*Purple Mountain Laboratories, Nanjing 210096, China*

Received 30 April 2025/Revised 23 August 2025/Accepted 23 October 2025/Published online 18 November 2025

Abstract A 300-GHz four-channel transmitter and receiver integrated with on-chip antennas in a 130-nm SiGe process are proposed for next-generation wireless communication. The fundamental-mixer-last architecture is utilized for high-order modulation, and the four-channel topology is introduced to achieve a high equivalent isotropically radiated power (EIRP). The scalable, highly-integrated transceiver contains high-gain lens-loaded on-chip antennas, fundamental up- and down-mixers, high-power local oscillator (LO) chains, and miniaturized power distribution networks, which are jointly considered for achieving attractive performance. For the on-chip antenna, an additional slab is introduced between the chip and the silicon lens to significantly improve the gain. Thereafter, the interference of the RF balun of the mixers is switched to achieve 0°/180° phase for the on-chip antenna element. To support a high output power of the up-mixer, a high-power LO chain is realized by using a two-way power-combining topology. Furthermore, the intermediate frequency (IF) power distribution network is embedded into the antenna array, and the LO 1-to-4 power divider is miniaturized for achieving a compact layout. Finally, the proposed transmitter and receiver are fabricated and measured, achieving a record EIRP of 22.6 dBm at 302 GHz compared to previously reported silicon-based transmitters with fundamental-mixing topology around 300 GHz. Moreover, 16/64QAM modulation wireless communication is realized at a 20 cm distance, making the transceiver suitable for next-generation communication.

Keywords 130-nm SiGe, four-channel, next-generation wireless communication, on-chip antenna, transceiver

Citation Tang S-Y, Li Z K, Zheng S D, et al. A 285–310 GHz four-channel transceiver with 22.6 dBm EIRP supporting 64QAM modulation in 130-nm SiGe process. Sci China Inf Sci, 2025, 68(12): 220305, https://doi.org/10.1007/s11432-025-4651-9

1 Introduction

With the rapid development of communication technology, traditional communication has faced several challenges owing to the crowding of the spectrum resources in the microwave and even millimeter-wave frequency bands. Thus, exploring new frequency bands for next-generation wireless communication is essential. The terahertz frequency bands have great potential owing to their wide range of undeveloped frequency bands, which are highly suitable for next-generation, high-speed wireless communication [1,2]. Among the terahertz frequency bands, the 300-GHz band is attractive because of its potentially larger bandwidth [3,4]. Moreover, transceivers play a critical role as components of communication systems [5]. However, designing highly integrated transceivers for communication becomes more challenging owing to the increased frequency. For instance, the atmospheric attenuation is increased compared to that in the lower frequency band, and the limited cutoff frequency of the transistor decreases the output power and increases the noise figure.

In recent decades, multiple silicon-based transceivers have been proposed for use in the 300-GHz band [6–11]. In [7,8], the transceivers were packaged in waveguide modules, and wireless links in 16 and

* Corresponding author (email: pgzhouseu@seu.edu.cn, zhechen@seu.edu.cn, jxchen@seu.edu.cn)
† These authors contributed equally to this work.

32QAM were realized with 4 and 3 cm distances, respectively. Moreover, CMOS-based transceivers with antennas-on-printed-circuit-board (PCB) were developed by flip-chip bonding techniques for realizing high-speed communication [9, 10]. However, the link distances of these studies were limited to within 5 cm because of the relatively low equivalent isotropically radiated power (EIRP), which greatly limits the application within a relatively closed area. Moreover, waveguide- or PCB-based antennas decrease the integration level of the system, making their use in small-scale equipment difficult.

Hybrid integration is a promising solution to these critical issues, wherein power amplifiers in InP HBT technology have been integrated in 300-GHz on-chip systems [12, 13]. The EIRP could be enhanced by the InP-based power amplifier and on-chip antenna, and the link distance was significantly increased to 20 cm or more. However, the InP-based chip is much more expensive than chips based on silicon technology, and is less easily integrated with digital circuits. Furthermore, previous studies [12, 13] considered only on-chip transmitters, and a commercial-based module was utilized as the receiver, which lowered the integration level. In summary, developing a scalable silicon-based transceiver with high integration and a long communication distance is an essential research target.

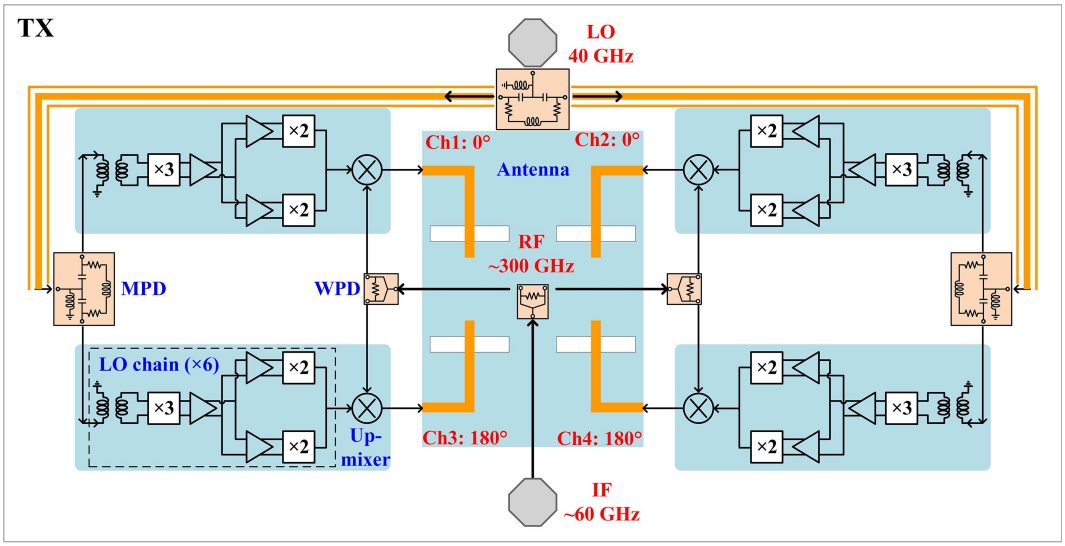
In this study, a 300-GHz transceiver with an on-chip antenna is proposed for next-generation communication. The proposed transmitter and receiver adopt a mixer-last and four-channel architecture, which contains high-gain on-chip antennas, fundamental up- and down-mixers, high-power ×6 local oscillator (LO) chains, and miniaturized power distribution networks. By jointly considering and integrating these devices, a highly integrated transceiver with attractive performance is realized. As a proof-of-concept, the proposed transceiver is fabricated and measured, affording an EIRP of 22.6 dBm and a wireless link in 16/64QAM modulation with 20 cm distance.

2 Transmitter and receiver

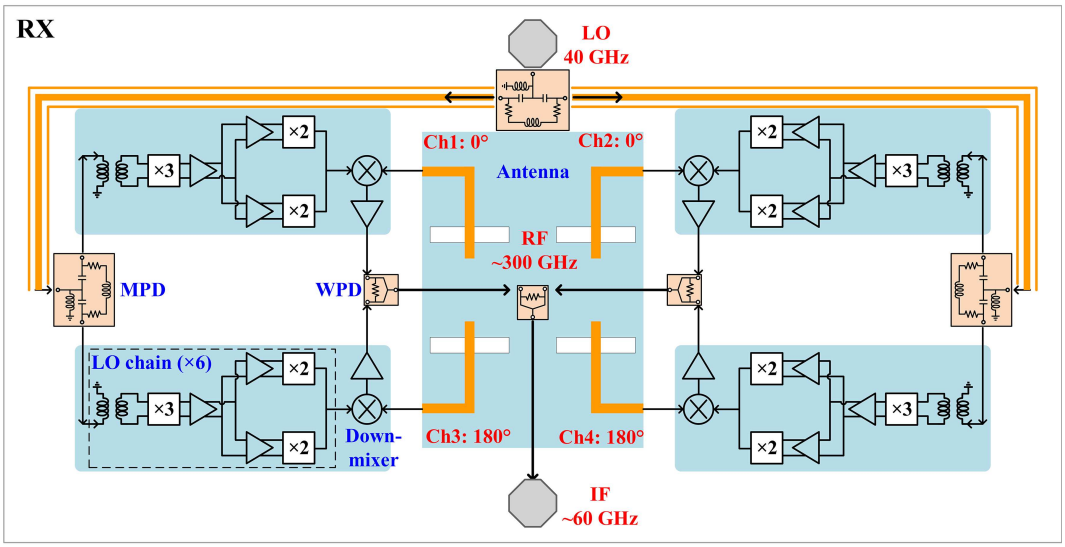
2.1 Architecture

Firstly, the architecture of the silicon-based transceiver for 300-GHz communication is discussed. An amplifier-last architecture is commonly used to boost the output power and lower the noise figure of transceivers. However, when the operating frequency approaches 300 GHz, the maximum achievable gain of silicon-based devices ($G_{\max}$) is low and the transistor model lacks accuracy, leading to limited performance. For instance, the output power of a reported amplifier was only roughly 4 dBm at 300 GHz [14]. Alternatively, the amplifier could be replaced by a multiplier as the last component in the transceiver before the antenna, and comparable output power could also be realized [15]. However, as a series of drawbacks, the multiplier-last architecture suffers from a low spectral purity and difficulty in multi-bit digital modulation [16]. Consequently, the mixer-last architecture is utilized in the proposed transceiver to prospectively achieve high-order modulation, where the power consumption could be greatly reduced if the amplifier is not introduced, which is beneficial for heat dissipation. Moreover, to compensate for the relatively low output power of the mixer, multiple channels could be introduced to realize power combining. Previous studies [17] demonstrated that the on-chip multi-fed antenna array exhibits more stable radiation patterns than the antenna element.

Thus, four-channel transmitter and receiver integrated with on-chip antennas are proposed, as shown in Figure 1. For the transmitter, the four-element on-chip slot array antenna with a silicon lens loading is fed with the same magnitude and 0°/0°/180°/180° phases provided from four active channels. Moreover, each channel consists of a fundamental up-mixer and a high-power ×6 LO chain. The receiver shares a similar on-chip antenna, a fundamental down-mixer integrated with an IF amplifier, and the same LO chain. Furthermore, the intermediate frequency (IF) signals of the four channels for both the transmitter and receiver are distributed by a conventional 1-to-4 Wilkinson power divider (WPD), which is located in the gap between the antenna elements. In contrast, the LO signals of the four channels are distributed by a miniaturized power divider (MPD), which is placed on the periphery of the active circuits. Moreover, the channel number of the proposed transceiver could be scaled to $2\times N$, which is similar to the previous studies [18, 19].



(a)



(b)

Figure 1 (Color online) Block diagram of the proposed four-channel transceiver. (a) Transmitter; (b) receiver.

2.2 Building blocks

2.2.1 *High-gain on-chip antenna array*

In contrast with the traditional patch antenna with broadside radiation, the on-chip antenna is a slot array antenna with a silicon lens for backside radiation (-z direction). It can be divided into two parts, i.e., on-chip and off-chip components. To miniaturize the chip, the slot antenna with backside radiation is chosen for the on-chip part because of its small aperture. Herein, four slots are etched on the ground plane, and four microstrip lines are introduced to excite the slot array antenna. To obtain a symmetrical radiation pattern, the excitations of four ports of the slot array are set as 0°/0°/180°/180°, respectively. The off-chip hemispherical silicon lens is then attached beneath the chip, as seen in Figure 2(a). It could transform the surface waves into backside radiated waves, enabling gain and efficiency improvements [20]. Moreover, by inserting an additional slab between the standard hemispherical lens and chip, the backside gain could be maximized [21]. Taking the on-chip antenna in the transmitter as an example, the backside gain is heavily dependent on the thickness of the silicon slab, as seen in Figure 2(b). Consequently, the thickness of the silicon slab is set as 2 mm to obtain a maximum gain of 23.4 dBi at 300-GHz. In this case, the antenna efficiency is 54%. For ease of packaging, the fabricated lens could be integrated with the slab.

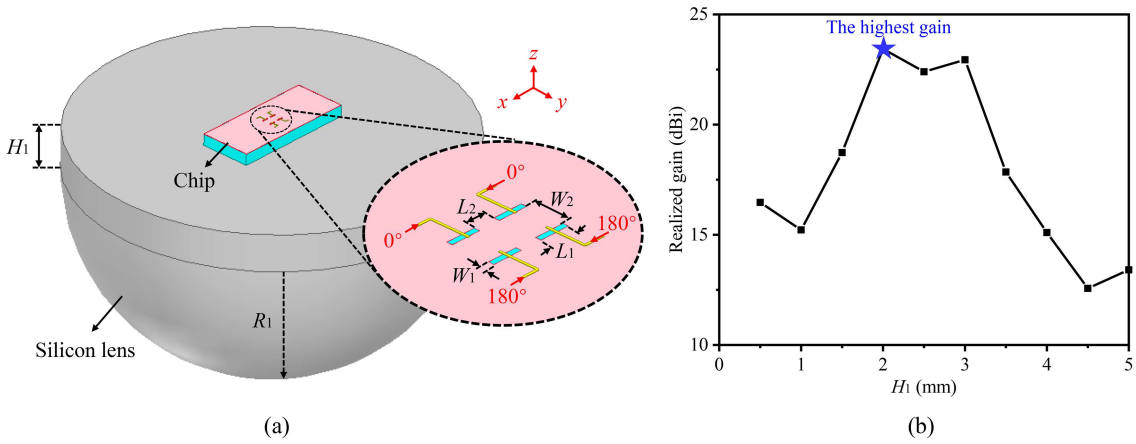


Figure 2 (Color online) Proposed on-chip antenna with a silicon lens loading. (a) 3-D geometry ($L_1 = 0.16$, $L_2 = 0.115$, $W_1 = 0.03$, $W_2 = 0.195$, $H_1 = 2$, $R_1 = 7.5$, units: mm); (b) backside gain at 300 GHz with a variable thickness of silicon slab (H_1).

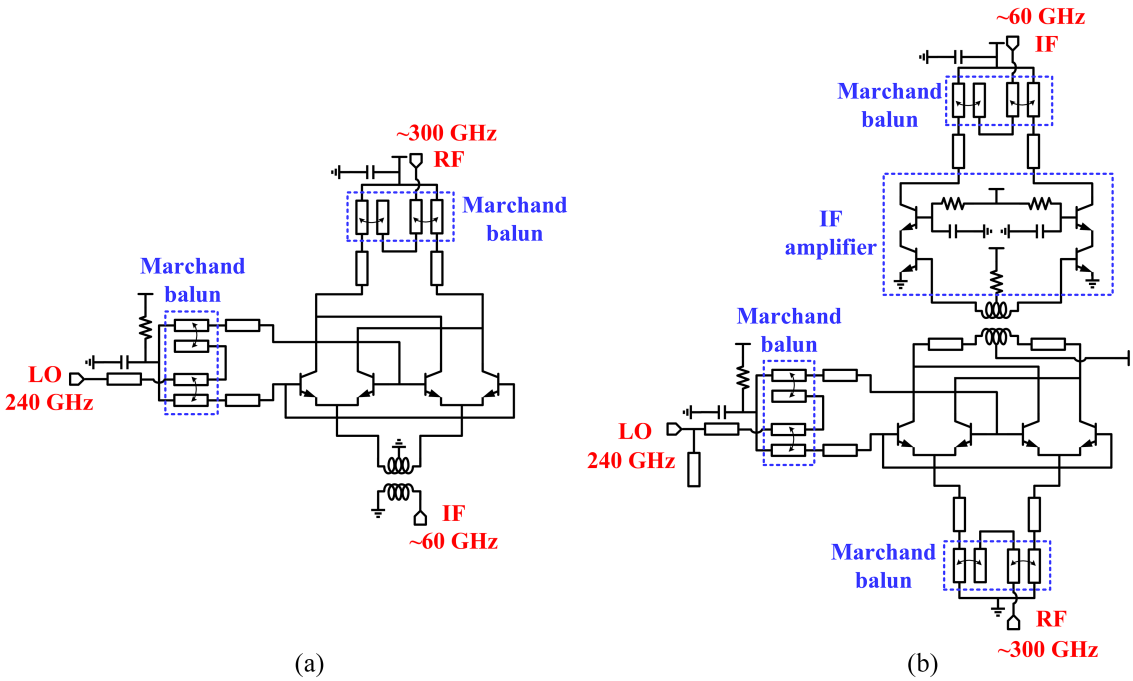


Figure 3 (Color online) Circuit schematics of the proposed 300 GHz mixers. (a) Up-mixer; (b) down-mixer.

2.2.2 *Fundamental up- and down-mixer*

The fundamental-mixing topology shown in Figure 3 is utilized for both the up-mixer and down-mixer, with an IF frequency of approximately 60 GHz. The differential double balanced mixer core is introduced into the up-mixer shown in Figure 3(a) [22] to enhance the isolation and suppress common-mode signals, and a low-impedance transmission line is utilized to decrease the loss of the matching network. Moreover, to determine the desired LO power, the saturated output power and conversion gain of the up-mixer versus with the input LO power are shown in Figure 4. It could be seen that the input LO power of the up-mixer should be maintained at roughly 9 dBm to simultaneously obtain high output power and conversion gain. As a result, a simulated −1 dBm peak output power and approximately −9 dB conversion gain (CG) are realized when the LO power is set as 9 dBm. The topology of the down-mixer in Figure 3(b) is similar to that of the up-mixer, with an additional IF amplifier for enhancing the conversion gain. By this arrangement, a peak conversion gain of approximately 20 dB is obtained.

Additionally, there are 180° phase difference requirements between channels 1–2 and 3–4, which are met by properly selecting the interface of the RF balun of the mixer. As seen in Figure 5(a), there are

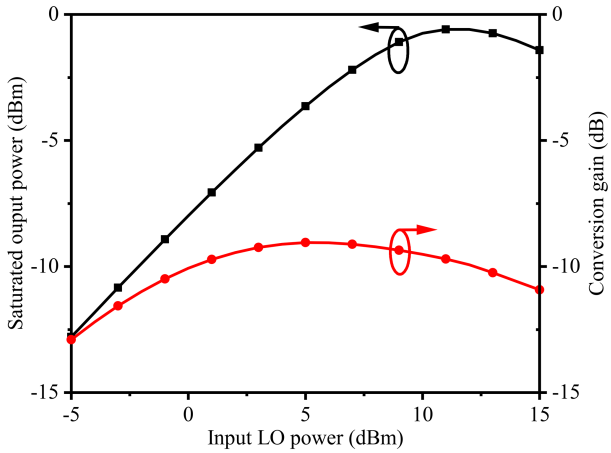


Figure 4 (Color online) Saturated output power and conversion gain of up-mixer with variable input LO power as LO = 40 GHz and IF = 60 GHz.

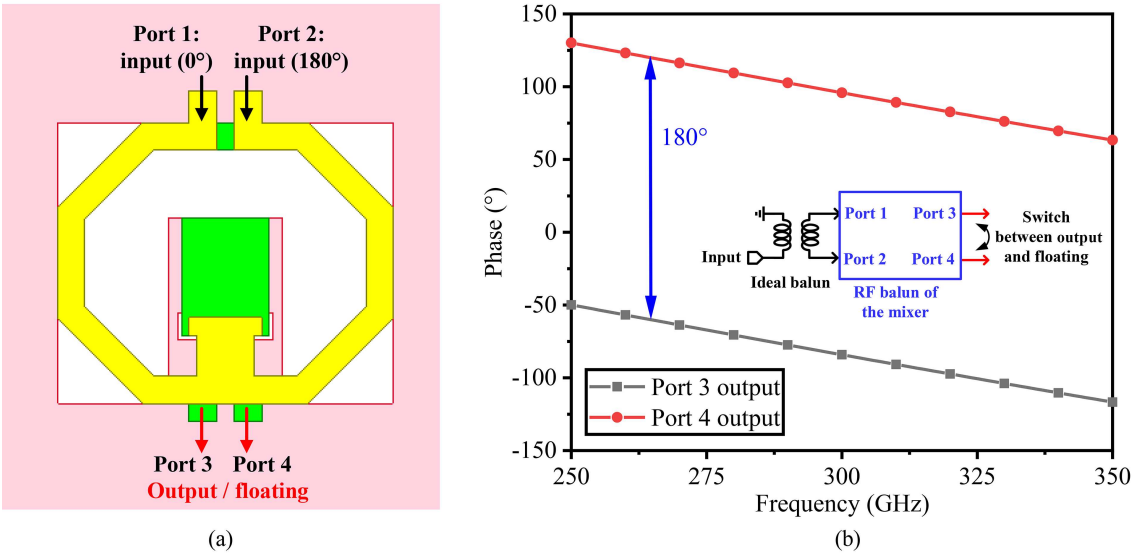


Figure 5 (Color online) Realization of different phases by the RF Marchand balun in the mixer. (a) Sketch; (b) simulated phases.

four ports in the RF Marchand balun of the mixer. The differential input signals from ports 1 and 2 can be transformed into a single-ended signal sent to port 3, while port 4 remains floating. Moreover, when the port 3 is switched to floating, the output signal from port 4 would have an inherent 180° phase difference compared to that from port 3 in Figure 5(b). Using this arrangement, phase differences between the different channels could be achieved without any additional devices, which optimizes the layout and reduces losses.

2.2.3 *High-power ×6 LO chain*

As discussed above, a high LO power is vital for increasing the output power of the up-mixer. An LO chain is proposed herein for providing 240 GHz signals [23], and a multiplication factor of 6 is selected to maintain a relatively low input frequency (40 GHz). To realize a high harmonic rejection and efficiency, the ×6 multiplier consists of an F-band tripler, an F-band driver amplifier, two F-band power amplifiers, and a G-/J-band push-push doubler. To obtain a high output power, the doubler is realized using a two-way power combining topology. On this basis, a high simulated output power of 8.9 dBm is obtained, and all the harmonic rejections exceed 20 dBc. Moreover, the input power is set to approximately −5 dBm to achieve a high output power and conversion gain. These attractive features make the ×6 multiplier suitable for providing LO signals in both the transmitter and receiver.

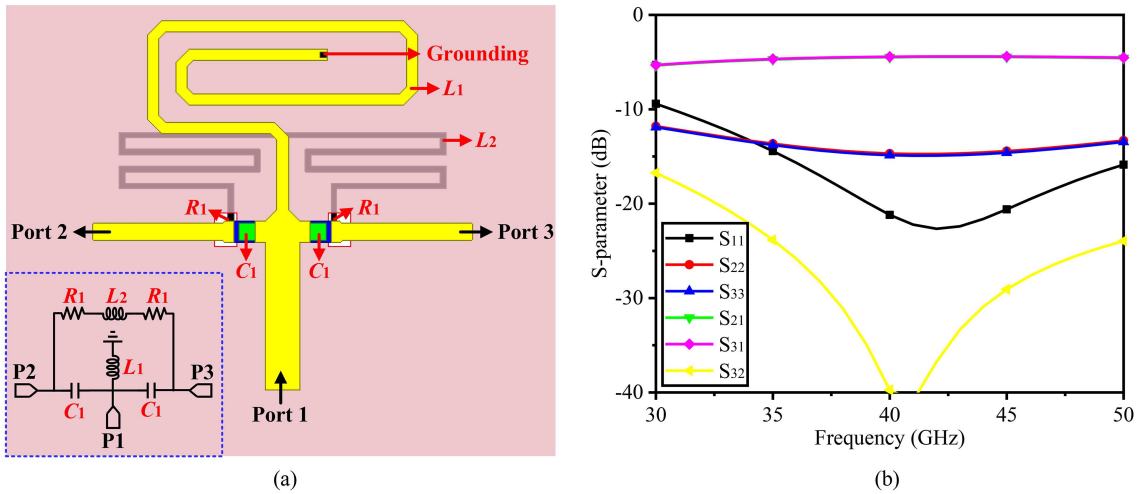


Figure 6 (Color online) Proposed 1-to-2 miniaturized power divider for LO signal. (a) Circuit schematic and geometry; (b) simulated S-parameters.

2.2.4 *Miniaturized power distribution network*

The power dividers realized on-chip are vital for distributing the LO and IF signals from the external signal source into multiple channels. As seen in Figure 2, the 1-to-4 Wilkinson power divider of the IF signal is embedded into the on-chip antenna, which is located in the gap between the slot antenna elements. This arrangement has a slight effect on the performance of the antenna because the proposed antenna is designed with backside radiation.

However, the power splitter of the LO signal is placed at the periphery of the chip, and it is vital for miniaturization. The reasons are given as follows: on the one hand, it is cost-effective as fabrication of chip is expensive, and on the other hand, chip with a larger overall size would decrease the radiation efficiency of the on-chip slot antenna [24]. As such, a 1-to-4 MPD consisting of three 1-to-2 MPDs is introduced, and the circuit schematic and detailed structure of 1-to-2 MPD are presented in Figure 6(a). By introducing lumped components, the quarter wavelength lines in the conventional Wilkinson power divider could be replaced, thus reducing the size of the divider. The proposed divider contains a shunt inductor L_1, two capacitors C_1, isolation resistors R_1, and an isolation inductor L_2. Inductor L_1 is implemented by the top metal layer and grounded by vias. Thereafter, inductor L_2 is realized by the bottom metal layer to avoid overlap with the routing line. Moreover, the capacitors C_1 are realized by the MIM capacitors in silicon technology. Herein, the detailed values of these components could be calculated based on [25]:

$$L_1 = L_2 = 50/\omega = 198.9 \text{ pH}, \tag{1}$$

$$C = 1/(50\omega) = 79.6 \text{ fF}, \tag{2}$$

$$R = 25\ \Omega, \tag{3}$$

where ω=2$\pi \times f$, and f is set as 40 GHz. In Figure 6(b), 1-to-2 MPD is simulated for verification, demonstrating that all the ports are well matched. Moreover, an isolation higher than 30 dB is obtained, ranging from 37.9 to 44.7 GHz, with a minimum loss of 4.4 dB.

3 Experimental results and discussion

For demonstration, the proposed transmitter and receiver are fabricated using the 130-nm SiGe process, and the photograph is shown in Figure 7. Moreover, the proposed transceiver is packaged with a PCB and a silicon lens for measurement.

3.1 On-wafer measurement

The single-channel performance of the transmitter chip without the on-chip antenna is demonstrated on-wafer, and the block diagram of the measurement is shown in Figure 8.

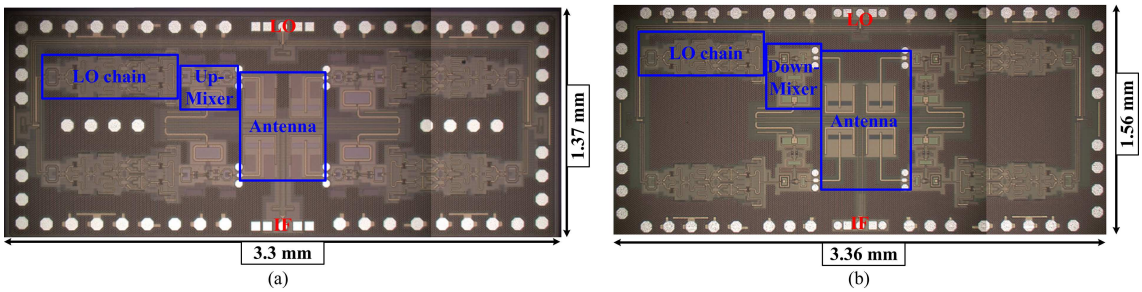


Figure 7 (Color online) Photograph of the proposed transceiver. (a) Transmitter; (c) receiver.

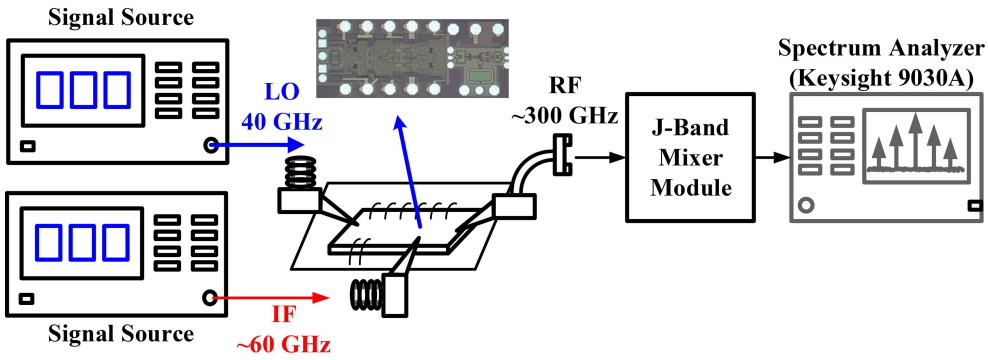


Figure 8 (Color online) Block diagram of on-wafer measurement.

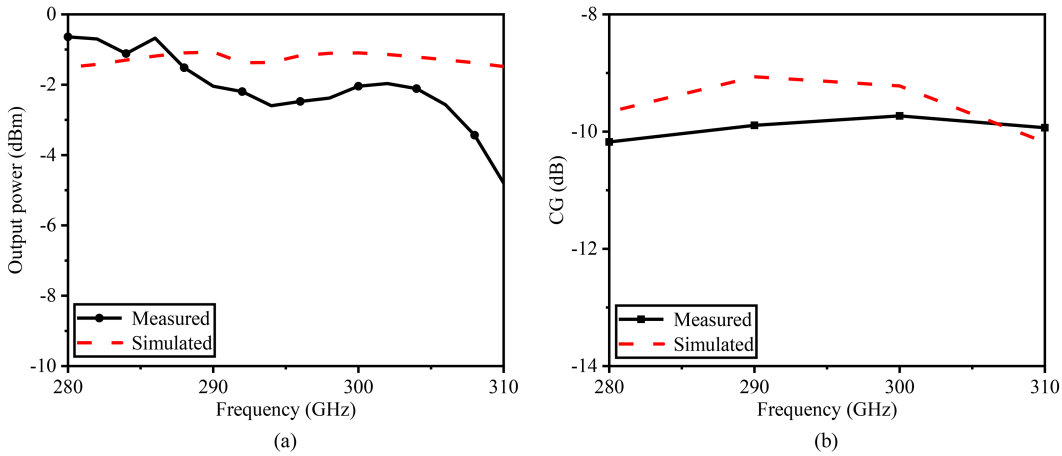


Figure 9 (Color online) Measured and simulated results. (a) Output power of the single-channel transmitter; (b) CG of the single-channel transmitter.

The LO and IF signals are provided by two external signal sources from GSG probes, while the RF signal is exported to a J-band mixer module and then a spectrum analyzer to determine the electrical level. The measured P_{out} and CG of the transmitter are shown in Figures 9(a) and (b), where a peak output power of −0.6 dBm and CG of −9.7 dB are obtained when the LO frequency is set as 40 GHz.

3.2 Over-the-air (OTA) measurement

The OTA measurement is performed, and the EIRP of the four-channel transmitter is verified individually. Herein, the LO and IF signals of the proposed transmitter are provided by two respective signal sources. The radiated power of the transmitter is received by a J-band mixer module with a standard horn antenna, and the spectrum analyzer is introduced to determine the electrical level of the received signal. The EIRP is then calibrated by replacing the proposed transmitter with a J-band multiplier module and a standard horn antenna. Figure 10 shows the measured EIRP of the proposed transmitter with the fixed LO signal of 40 GHz and variable IF frequency, where a peak EIRP of 22.6 dBm and a 3-dB bandwidth

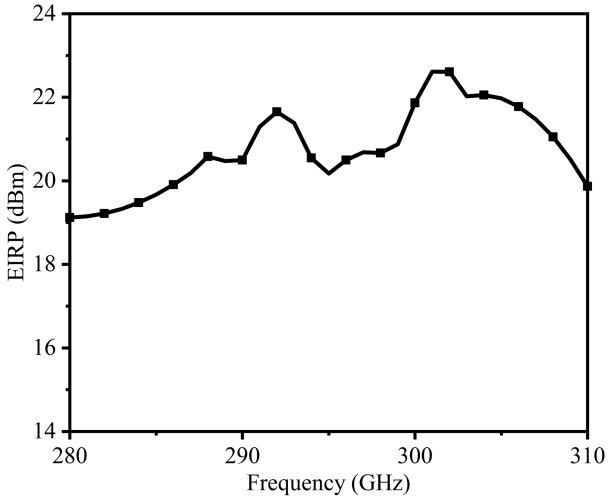


Figure 10 Measured EIRP of the proposed four-channel transmitter.

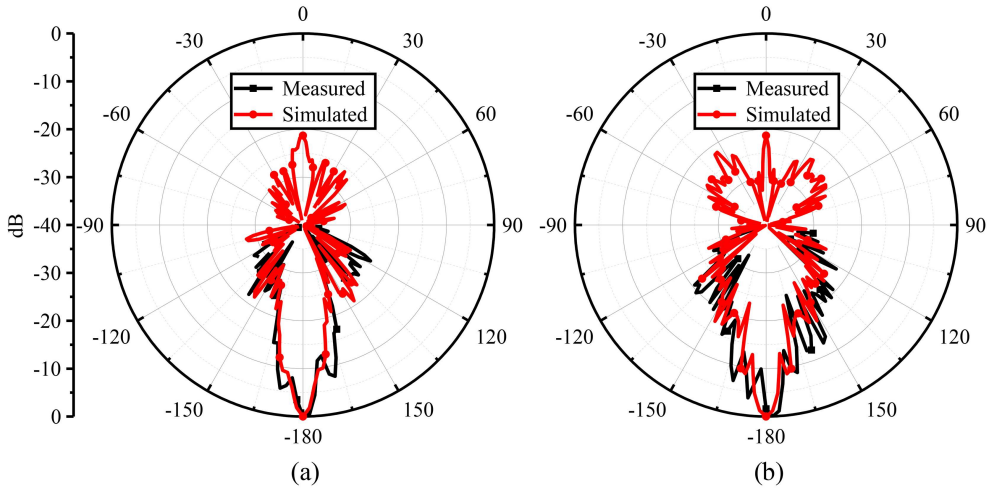


Figure 11 (Color online) Measured and simulated normalized radiation patterns of the four-channel transmitter at 300-GHz. (a) *xoz*-plane; (b) *yoz*-plane.

spanning 285 to 310 GHz is obtained, benefiting from the four-channel topology and the loading of the silicon lens. Moreover, the normalized far-field radiation patterns of the transmitter at 300 GHz are plotted in Figure 11. The measured and simulated results are consistent, where the slight asymmetry in the measured radiation pattern is attributed to assembly errors.

The wireless link transmission is demonstrated using the proposed four-channel transmitter and receiver, where the corresponding measurement block diagram and environment are depicted in Figure 12. The IF signal of the transmitter chip is provided by a V-band I/Q transmitter module[1)] because it is difficult to provide a 60-GHz modulated signal using the arbitrary waveform generator (AWG). As such, the LO and IF signals of the V-band transmitter module are provided by a signal source and the AWG, respectively, and an additional signal source is introduced to provide the LO signal for the proposed transmitter. Similarly, the LO signal of the proposed receiver chip is obtained from a signal source, and its IF signal is exported to a V-band I/Q receiver module[2)]. Finally, the IF signal of the V-band receiver module is received by the oscilloscope. Note that the wireless link transmission is achieved without any additional external lens apart from the integrated silicon lens, which further improves the integration of the transceiver. Consequently, an 800 Mbaud symbol rate in 16QAM modulation and a 50 Mbaud symbol rate in 64QAM modulation are achieved. In fact, the data rate is restricted by two factors. (i) The cascading of multiple modules, i.e., V-band I/Q transmitter and power amplifier, reduces the flat-

1) https://www.atmicrowave.com/uploads/PDF/AT-VTX-5766.pdf.
2) https://www.atmicrowave.com/uploads/PDF/AT-VRX-5766.pdf.

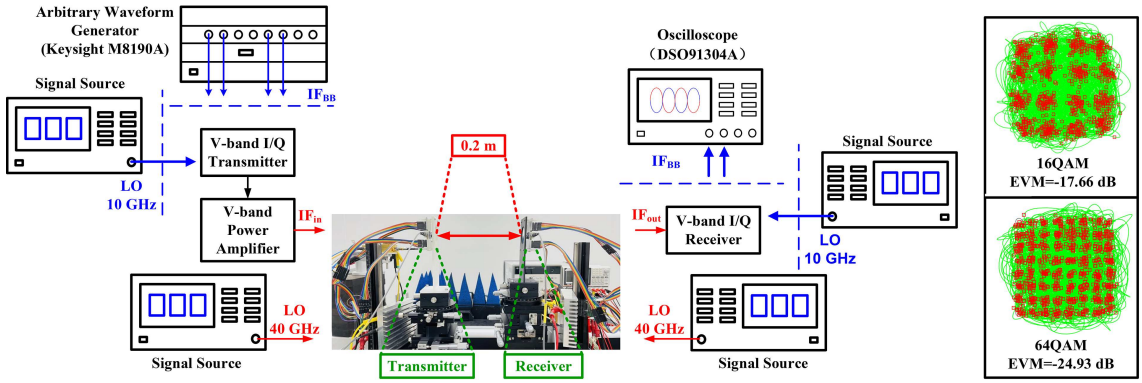


Figure 12 (Color online) Measurement block diagram and constellation diagrams of the wireless transmission.

Table 1 Comparison of the proposed work with silicon-based transceivers for communication. "–" represents not available. "*" represents power consumption of the signal channel.

Ref.	Technology	Topology/ channel number	Antenna type	Frequency (GHz)	TX EIRP (dBm)	Modulation type	Link distance (cm)	P_{DC} (W)
[7]	65-nm CMOS	TRX(1)	Waveguide-based	278–304	–	QPSK 16QAM	4	0.27(TX) 0.14(RX)
[8]	40-nm CMOS	TRX(1)	Waveguide-based	252–279	–	QPSK 16QAM 32QAM	3	0.89(TX) 0.897(RX)
[9]	40-nm CMOS	TX(4)	PCB-based	263–279	−6.9	16QAM	5	3.7(TX)
[10]	65-nm CMOS	TRX(4)	PCB-based	256	–	QPSK	3.5	0.75(TX)* 0.75(RX)*
[12]	65-nm CMOS+ 250-nm InP	TX(4)	On-chip	220–265	8.4	QPSK 16QAM	50	2.64(TX)
[13]	130-nm SiGe+ 700-nm InP	TX(1)	On-chip	280–300	21.9	QPSK	20	0.72(TX)
Proposed	130-nm SiGe	TRX(4)	On-chip	285–310	22.6	16QAM 64QAM	20	1.845(TX) 2.152(RX)

ness of the output signal. (ii) The low-noise amplifier is not introduced in the receiver, which influences the signal-to-noise ratio.

3.3 Discussion

Finally, the proposed transceiver is compared with previous silicon-based studies for wireless communication in Table 1. A high operating frequency of 285–310 GHz with a high EIRP of 22.6 dBm is achieved, which supports a link distance as long as 20 cm. More importantly, a high integration level is realized by integrating fully-silicon-based TRX and on-chip antennas.

4 Conclusion

A four-channel transmitter and receiver implemented in 130-nm SiGe process are proposed in this study. The transceiver contains high-gain lens-loaded on-chip antennas, fundamental up- and down-mixers, a high-power ×6 LO chain, and miniaturized power distribution networks, demonstrating a high integration level. The proposed transceiver is fabricated and measured, which shows a peak EIRP of 22.6 dBm within 285–310 GHz, supporting a wireless link in 64QAM modulation over a 20 cm distance. These attractive performance metrics make the proposed transceiver a good candidate for next-generation wireless communication.

Acknowledgements This work was supported in part by Major Project of Jiangsu Province (Grant No. BG2024034), National Natural Science Foundation of China (Grant Nos. 62188102, 62171128), and ZTE Industry-University-Institute Cooperation Funds.

References

1 Wei Y, Yu J J, Wang M X, et al. Experimental demonstration of 220-GHz terahertz signals wireless transmission over 4.6 km. Sci China Inf Sci, 2025, 68: 114301
2 Jiang N, He P Y, Liu H Q, et al. A D-band CMOS eight-channel I/Q transmitter with enhanced LO feed-through suppression. Sci China Inf Sci, 2025, 68: 179401

3 Wang K H, Yu J J, Li W P, et al. Demonstration of DSM-OFDM-1024QAM transmission over 400 m at 335 GHz. Sci China Inf Sci, 2023, 66: 189302
4 Zhu M, Zhang J, Yu J J, et al. Demonstration of record-high 352-Gbps terahertz wired transmission over hollow-core fiber at 325 GHz. Sci China Inf Sci, 2022, 65: 127301
5 Fang K, Chen J X, Zhu H, et al. Explainable-AI-based two-stage solution for WSN object localization using zero-touch mobile transceivers. Sci China Inf Sci, 2024, 67: 170302
6 Al-Eryani J, Knapp H, Kammerer J, et al. Fully integrated single-chip 305-375-GHz transceiver with on-chip antennas in SiGe BiCMOS. IEEE Trans THz Sci Technol, 2018, 8: 329–339
7 Abdo I, Fujimura T, Miura T, et al. A 300 GHz wireless transceiver in 65 nm CMOS for IEEE802.15.3d using push-push subharmonic mixer. In: Proceedings of 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020. 623–626
8 Lee S, Hara S, Yoshida T, et al. An 80-Gb/s 300-GHz-band single-chip CMOS transceiver. IEEE J Solid-State Circ, 2019, 54: 3577–3588
9 Takano K, Beppu S, Yagi H, et al. A 300-GHz-band 40-Gb/s 2D phased-array CMOS transmitter with near-half-wave antenna pitch. In: Proceedings of 2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2024. 335–338
10 Abdo I, da Gomez C, Wang C, et al. A bi-directional 300-GHz-band phased-array transceiver in 65-nm CMOS with outphasing transmitting mode and LO emission cancellation. IEEE J Solid-State Circ, 2022, 57: 2292–2308
11 Deng X D, Li Y, Li J, et al. A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology. IEEE Trans THz Sci Technol, 2015, 5: 930–940
12 Abdo I, Jyo T, Pander A, et al. 300-GHz-band four-element CMOS-InP hybrid phased-array transmitter with 36° Steering Range. IEEE Microw Wireless Tech Lett, 2023, 33: 887–890
13 Lu H, Chen J, Yan P, et al. 280-300 GHz SiGe-InP hybrid-integrated transmitter with 21.9 dBm EIRP and 10 Gbps data rate. IET Microw Antenna P, 2024, 18: 878–884
14 Li X, Chen W, Zhou P, et al. A 250-310 GHz power amplifier with 15-dB peak gain in 130-nm SiGe BiCMOS process for terahertz wireless system. IEEE Trans THz Sci Technol, 2022, 12: 1–12
15 Breun S, Schrotz A M, Dietz M, et al. A 268-325 GHz 5.2 dBm Psat frequency doubler using transformer based mode separation in SiGe BiCMOS technology. In: Proceedings of IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2021. 1–4
16 Katayama K, Takano K, Amakawa S, et al. A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels. IEEE J Solid-State Circ, 2016, 51: 3037–3048
17 Sengupta K, Hajimiri A. Designing optimal surface currents for efficient on-chip mm-wave radiators with active circuitry. IEEE Trans Microwave Theor Techn, 2016, 64: 1976–1988
18 Li S, Zhang Z, Rebeiz G M. An eight-element 136–147 GHz wafer-scale phased-array transmitter with 32 dBm peak EIRP and >16 Gbps 16QAM and 64QAM operation. IEEE J Solid-State Circ, 2022, 57: 1635–1648
19 Yang M, Song C, Wu L. A 334-to-348-GHz 7×2 radiator array with coupled-line-based mode-decoupling harmonic enhancement and chip-to-waveguide interface achieving 30-dBm EIRP. In: Proceedings of IEEE Custom Integrated Circuits Conference (CICC), 2024. 1–2
20 Han R, Afshari E. A CMOS high-power broadband 260-GHz radiator array for spectroscopy. IEEE J Solid-State Circ, 2013, 48: 3090–3104
21 Jalili H, Momeni O. A 0.46-THz 25-element scalable and wideband radiator array with optimized lens integration in 65-nm CMOS. IEEE J Solid-State Circ, 2020, 55: 2387–2400
22 Zheng S, Li Z, Zhou P, et al. A 300-GHz upconverter with 0-dBm Psat and 44-GHz bandwidth in 130-nm SiGe BiCMOS. IEEE Microw Wireless Tech Lett, 2023, 33: 1646–1649
23 Li Z, Chen J, Tang D, et al. A 205-273-GHz frequency multiplier chain (×6) with 9-dBm output power and 1.92% DC-to-RF efficiency in 0.13-μm SiGe BiCMOS. IEEE Trans Microwave Theor Techn, 2023, 71: 2909–2919
24 Gao L, Chan C H. A 0.68–0.72-THz 2-D scalable radiator array with –3-dBm radiated power and 27.3-dBm EIRP in 65-nm CMOS. IEEE J Solid-State Circ, 2022, 57: 3114–3124
25 Li Z, Chen J, Li H, et al. A 220-GHz sliding-IF quadrature transmitter and receiver chipset for high data rate communication in 0.13-μm SiGe BiCMOS. IEEE J Solid-State Circ, 2023, 58: 1913–1927