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Highly efficient Doherty power amplifier with peak/backoff joint matching

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With the rapid development of modern wireless systems, modulation schemes with high peak-to-average power ratios (PAPRs) are widely adopted. As a crucial part of the wireless front-end, power amplifiers (PAs) are desired to maintain high efficiency in the wide output power backoff (OBO) region to transmit modulation signals. At the base station side, Doherty PAs (DPAs) [1] become widely used architectures due to their high efficiency and ease of implementation.

To improve the average efficiency of DPA when driving high-PAPR modulation signals, several techniques have been exploited. The complex combining load (CCL) DPA is proposed in [2] to realize an extended OBO range. However, the CCL DPA exhibits a lack of research on matching at the OBO point, which causes relatively low efficiency at the OBO point. In the study, the peak/backoff joint matching (JM)-CCL techniques are employed to improve average efficiency.

CCL analysis. To extend the OBO region, asymmetric power cells or dividers are often used. However, these methods rely on either an under-utilized carrier PA or an enlarged peaking PA, which results in a lower power utilization factor. The CCL DPA offers a new degree of freedom to boost the OBO region while circumventing the issues.

Figure 1(a) is a simplified CCL DPA, which shows the impedance transformation at the peak point (red) and the OBO point (green) individually. The combined load impedance is a complex value of $R_{\rm L}$ + j$X_{\rm L}$ that is transformed from 50 Ω. $I_{\rm P,sat}$ and $I_{\rm C,sat}$ represent the currents of peaking PA and carrier PA, respectively, within an ideal model where $V_{\rm dc}$ assumes a maximum voltage swing. The ratio of these currents is α. $I_{\rm C,bo}$ is the current of carrier PA at the OBO point, and the ratio of $I_{\rm C,sat}$ to $I_{\rm C,bo}$ is defined as β. The relationship between these two currents can be given by [3] (x_n is the ratio of $X_{\rm L}$ to $R_{\rm L}$)

$$\beta=\frac{\left(1+\sqrt{\frac{\alpha^2+(\alpha x_n)^2}{(\alpha+2)^2+(\alpha x_n)^2}}\right)}{\left(1-\sqrt{\frac{\alpha^2+(\alpha x_n)^2}{(\alpha+2)^2+(\alpha x_n)^2}}\right)}. \tag{1}$$

The OBO region of the CCL DPA can be predicted by

$$\begin{aligned}\mathrm{OBO}&=10\log\left(\frac{0.5(I_{\rm C,sat}+I_{\rm P,sat})V_{\rm dc}}{0.5I_{\rm C,bo}V_{\rm dc}}\right)\\&=10\log[(1+\alpha)\beta].\end{aligned} \tag{2}$$

As shown in (1) and (2), the CCL coefficient x_n offers a new degree of freedom that can be utilized to boost the OBO region. For example, to achieve a CCL DPA with an OBO of 8.5 dB, the design parameters are provided in Figure 1(a). The parameters designated in green font are determined by the characteristics of the devices. The design goal is indicated in black. The freedom of design is indicated in red, and the parameters in blue are derived by solving (1) and (2) and the RC parallel formula with the above parameters.

Peak/backoff JM-CCL. However, the analysis above is conducted at the internal current source level, which is based on the assumption that the PA is an ideal current source with a constant output capacitor $C_{\rm ds}$ and the transistor output impedance at the OBO point $Z_{\rm C,bo}$ is designed as $[\beta R_{\rm C,opt} \parallel (\mathrm{j}/\omega C_{\rm ds})]$ which is considered the optimal impedance at the OBO point in the conventional CCL theory. Actually, due to the presence of knee voltage, the nonlinearity of $C_{\rm ds}$, and other nonideal factors, the optimal output impedance (including $C_{\rm ds}$) at the OBO point deviates from $[\beta R_{\rm C,opt} \parallel (\mathrm{j}/\omega C_{\rm ds})]$. Efficiency at the OBO point will be low if this imperfect matching is adopted.

Consequently, a load-pull simulation at the OBO point conducted at the device package instead of the internal current source plane is necessary to accommodate these nonideal factors. As illustrated in Figure 1(b), the simulated fundamental impedance load-pull result of the carrier PA at the OBO point is presented. It can be seen that the $Z_{\rm C,bo}$ realized in Figure 1(a) achieves an efficiency of only 52.6% (green), while the optimal value is 67.3% (red). Therefore, the JM-CCL method is proposed as a solution. The design goal of the JM-CCL DPA is to attain a DPA that can achieve high efficiency and equal power impedances at both the OBO and the peak point. As illustrated in Figure 1(c), the design parameters of JM-CCL

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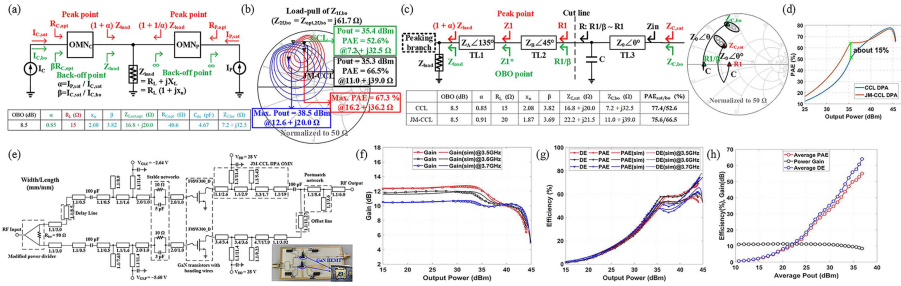

Figure 1 (Color online) (a) Simplified structure of the CCL DPA and design parameters of an 8.5 dB OBO; (b) load-pull of carrier PA at the OBO point at 3.6 GHz; (c) simplified OMN of carrier PA of a JM-CCL DPA with an OBO of 8.5 dB and comparisons between CCL and JM-CCL DPA; (d) simulated PAE comparison between CCL and JM-CCL DPA with ideal passive networks; (e) schematic and photograph of the GaN DPA. Simulated and measured CW results of (f) gain and (g) efficiency; (h) measured modulation results of the 20-MHz 64QAM LTE signal.

DPA reach an efficiency-better and power-same impedance at the OBO point ($Z_{\mathrm{C,bo}} = 11.0 + \mathrm{j}39.0\ \Omega$ with a power added efficiency (PAE) of 66.5%, as shown by the black triangle in Figure 1(b)). Although the impedance at peak point may have a deviation from the optimal impedance ($Z_{\mathrm{C,sat,opt}} = 16.8 + \mathrm{j}20.0\ \Omega$), its PAE has not deteriorated much ($Z_{\mathrm{C,sat}} = 22.2 + \mathrm{j}21.5\ \Omega$ with a PAE of 75.6%). The output matching network (OMN) of the main PA of JM-CCL DPA is also shown in Figure 1(c), which is implemented as an improved version of [2] for a better balance between OBO point and peak point. As analyzed in [2] and Appendix A, TL1 and TL2 can transform Z_{load} and $(1+\alpha)Z_{\mathrm{load}}$ to R_1 and R_1/β, which are purely resistive, and the ratio between them is β. Then, the problem is simplified by simultaneously matching two purely resistive impedances to two complex impedances. The part on the right side of the delineated area in Figure 1(c) demonstrates a structural arrangement for such a comparison. The model incorporates a parallel capacitor, designated as C, and a series transmission line, designated as TL3. The real and imaginary parts of Z_{in} are respectively calculated as follows:

$$\mathrm{Re}(Z_{\mathrm{in}}) = \frac{{Z_0}^2(1+\tan^2\theta)}{\frac{{Z_0}^2}{R} + R(\omega C Z_0 + \tan\theta)^2}, \tag{3}$$

$$\mathrm{Im}(Z_{\mathrm{in}}) = Z_0 \frac{{Z_0}^2\tan\theta + (\omega C Z_0 \tan\theta - 1)(\omega C Z_0 + \tan\theta)R^2}{{Z_0}^2 + (\omega C Z_0 + \tan\theta)^2 R^2}. \tag{4}$$

In our design, the value of R_1 is about 33 Ω and β is 3.69, which means that R ranges from 8.9 Ω at the OBO point to 33 Ω at the peak point. As demonstrated in (3) and (4), it is evident that as the parameter R increases, the real part experiences an increase when R is not substantial and a decrease when $\omega C Z_0 \tan\theta - 1 < \omega C Z_\theta + \tan\theta$. These trends correspond exactly to the trend of $Z_{\mathrm{C,bo}}$ to $Z_{\mathrm{C,sat}}$ changes. Following the prioritization of the OBO point's performance, the Z_{in}s are located in an optimal manner within the designated OBO and peak points (Figure 1(c)). Finally, a comparison is made between the PAEs of CCL and JM-CCL DPAs, both of which are equipped with harmonic controls. As illustrated in Figure 1(d), the PAE of JM-CCL at the OBO point exhibits a 15% increase compared with CCL while maintaining a nearly equivalent efficiency at the peak point and an extended OBO region of 8.5 dB.

Implementation and measurement results. This DPA is implemented by integrating two 13 W GaN HEMTs on a Rogers RO4350B PCB (Figure 1(e)). The quarter-wave TL is inserted in the TL close to the transistor for second harmonic impedance matching, which is known to improve efficiency [4]. The capacitor C in Figure 1(c) is replaced by a terminal open-circuit TL.

Figures 1(f) and (g) show the continuous-wave (CW) measurement performance. The GaN DPA considered delivers 43.3 dBm saturated output power with 69.3% drain efficiency (DE) and 60.1% PAE at 3.6 GHz. For the 8.5-dB OBO point, the system demonstrates 52.9% DE and 48.7% PAE. In addition, it obtains 42.2–44.2 dBm peak power, 64.0%–73.7%/57.0%–61.9% peak DE/PAE, and 43.7%–52.9%/41.3%–48.7% 8.5-dB OBO DE/PAE over 3.5–3.7 GHz.

For modulation tests, the 20-MHz 64QAM long term evolution (LTE) signal with 8.5-dB PAPR is applied. As shown in Figure 1(h), the GaN DPA considered attains an average PAE of 49.8%, an average DE of 55.9%, and a 9.7 dB power gain at an average output power of 34.8 dBm (i.e., an OBO of 8.5 dB) within the 3.6 GHz frequency band, without any calibrations.

Conclusion. This work presents a 3.5–3.7-GHz GaN DPA with high efficiency, which employs JM-CCL techniques. Then, the OMN of the JM-CCL DPA is given and subjected to analysis. The DPA model demonstrates a DE of 52.9% at an 8.5-dB OBO point and a DE of 69.3% at a peak point at 3.6 GHz. In addition, it exhibits superior average efficiency for modulation signals with high PAPR, thereby aligning with the energy-saving demands characteristic of contemporary wireless communication systems.

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Supporting information Appendix A. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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