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Improved synaptic properties of $HfSiO_x$-based ferroelectric memristors by optimizing Ti/N ratio in TiN top electrode for neuromorphic computing

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Abstract Recently, hafnium oxide-based ferroelectric memristors have attracted considerable research interest because they offer several advantages over conventional perovskite-based ferroelectric memristors, including better CMOS compatibility, lower power consumption, and enhanced scalability. HfO_x doped with silicon (Si) shows great potential, as silicon's smaller atomic radius compared with hafnium enhances the induction of ferroelectric properties. This study focuses on $HfSiO_x$-based ferroelectric memristors, examining the electrical characteristics of the devices by varying the DC power during the sputtering of the TiN top electrode while maintaining consistent silicon doping and material composition. Moreover, we emphasize the relationship between DC power and endurance, and assess the electrical characteristics of the devices by evaluating maximum remnant polarization ($2P_r$), interfacial capacitance (C_i), and tunneling electro resistance (TER) under various DC power conditions. Additionally, by investigating synaptic properties of ferroelectric memristors through potentiation and depression (P&D), and paired-pulse facilitation (PPF), the study demonstrates their potential for applications in neuromorphic computing.

Keywords ferroelectric memristors, optimal DC power, synaptic devices, potentiation and depression, hafnium silicon oxide

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1 Introduction

With the continuous advancement of electronic technology, the need for efficient and scalable memory devices has led to significant interest in ferroelectric memristors, which offer key advantages such as low power consumption, non-destructive readout, and simple device structures [1]. Traditional ferroelectric memristors based on perovskite materials like $PbZrO_3$ (PZT), $BaTiO_3$ (BTO), and $BiFeO_3$ (BFO) have shown promising results but are limited in terms of CMOS compatibility, scalability, and thermal stability [2–4]. In contrast, hafnium oxide (HfO_x)-based ferroelectric memristor devices present distinct advantages over these conventional perovskite models. HfO_x-based ferroelectric memristors are highly compatible with existing CMOS processes [5,6], exhibit faster switching speeds, and demonstrate excellent scalability, making them suitable for advanced electronic applications.

The field of ferroelectric memristors is rapidly advancing through diverse approaches. For instance, recent studies include attempts to precisely control the ferroelectric properties of $HfZrO_x$ (HZO) using alloy electrodes [7], achieving significant performance enhancements in $NaBiTiO_x$-based memory through innovative device structure design [8], and utilizing $LiNbO_3$-based nanocomposites in neuromorphic systems to mitigate the effects of device variability [9]. These examples illustrate multifaceted research directions, including material property control, device structure innovation, and system architecture optimization, reflecting the dynamic efforts toward advancing memristor technology. Among these promising materials, HfO_x has garnered particular attention.

The role of the orthorhombic (o-phase) in the ferroelectric properties of HfO_x-based ferroelectric memristors is well-established. The o-phase, which is thermodynamically destabilized under standard conditions, is crucial for enhancing the ferroelectric properties. By inducing tensile stress and using specific

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annealing processes [10,11], the o-phase can be stabilized, significantly improving P_r and tunneling electro resistance (TER), key factors that govern the performance of ferroelectric memristor devices. Research has shown that optimizing the o-phase can lead to superior memory characteristics and higher device stability. In various studies, dopants such as Si, Zr, and Al with HfO_x are being explored [12–14]. Compared with other variants like HZO, $HfSiO_x$(HSO) offers improved operational stability, primarily due to its smaller grain sizes. These smaller grains provide diffusion barriers, reducing the risk of device degradation and enhancing the overall performance of the ferroelectric memristors [15]. This characteristic makes HSO-based devices ideal for reliable, high-performance applications, particularly in neuromorphic computing. HSO has been recognized for its potential, but is still less extensively studied compared with other HfO_x-based materials like HZO [16]. In particular, further research is needed to explore the full capabilities of HSO and its applications in ferroelectric memristors, especially concerning scalability, robustness, and integration with emerging technologies.

In this study, we fabricated metal-ferroelectric-semiconductor (MFS) devices with a TiN/HSO/n^+ Si structure. To understand the impact of DC power on the deposition of the top electrode (TiN), we compared different DC power levels of 70, 100, and 130 W. The devices were analyzed using the PUND method to obtain P_r, TER, Ti/N ratio to investigate oxygen scavenging effects, electrical thin-film analysis, and X-ray diffraction (GIXRD). The electrical characteristics of the devices were measured using a Keithley 4200-SCS parameter analyzer. As a result, the device with the top electrode deposited at 130 W exhibited superior performance. Based on these analysis results, we performed paired-pulse facilitation (PPF) and potentiation and depression (P&D) measurements, and MNIST simulations were conducted through an online learning mechanism. This demonstrates the high potential of HSO-based ferroelectric memristor memory devices for applications in artificial intelligence neural networks.

2 Experiments

The fabrication process of the TiN/HSO/n^+ Si ferroelectric memristor device with an MFS structure is detailed in Figure S1. Initially, a heavily doped n^+ Si substrate (resistivity $> 0.005\ \Omega$·cm) was prepared as the starting material. To remove organic contaminants from the wafer surface, the sulfuric acid peroxide mixture (SPM) process was performed using a 4:1 dilution of H_2SO_4 and H_2O_2. To eliminate particles and organic impurities, the standard cleaning 1 (SC-1) process was conducted by diluting ammonia, hydrogen peroxide, and deionized (DI) water. Since this step can cause surface metal contamination due to the low redox potential, the SC-2 process was also performed by diluting hydrochloric acid, hydrogen peroxide, and DI water to remove any transition metal contaminants. Finally, to remove the native oxide layer, the dilute HF (DHF) cleaning was conducted using a 1:100 dilution of HF and H_2O. After completing the cleaning process, an HSO film was deposited via atomic layer deposition at a stage temperature of 350°C. In this process, O_2 plasma served as the reactant, while diisopropylamino silane and tetrakis(ethylmethylamino)hafnium were used as the precursors for Si and Hf, respectively. The Hf and Si were deposited in a 26:1 ratio over three cycles, resulting in a film thickness of 10 nm, with the Si content in the HSO film maintained at 5%. Subsequently, a TiN capping layer with a thickness of 100 nm was deposited as the top electrode via sputtering (physical vapor deposition method) at DC powers of 70, 100, and 130 W. To induce the orthorhombic phase of the HSO, rapid thermal annealing (RTA) was performed at 750°C for 20 s in a nitrogen (N_2) atmosphere. Finally, lithography was conducted using an appropriate mask to form a 100 μm × 100 μm pattern for the top electrode. The electrical characterization of the device was carried out using a Keithley 4200-SCS system, while pulse characteristics were analyzed with the 4225-PMU ultrafast current-voltage module.

3 Results and discussion

Figure 1(a) presents a schematic illustration of the fabricated TiN/HSO/n^+ Si device, while the overall manufacturing process of the device is shown in Figure S1. Figure 1(b) displays a cross-sectional transmission electron microscopy (TEM) image. The magnified TEM image in Figure 1(b) shows the boundaries between each layer indicated by dashed lines. During the high-temperature annealing process, it is observed that a TiON interfacial layer forms at the TiN/HSO interface. This formation is attributed either to the diffusion of oxygen from the HSO layer toward the highly reactive TiN electrode or to the oxygen scavenging effect by the TiN layer [17]. In addition, the presence of a SiO_2 layer at the HSO/n^+

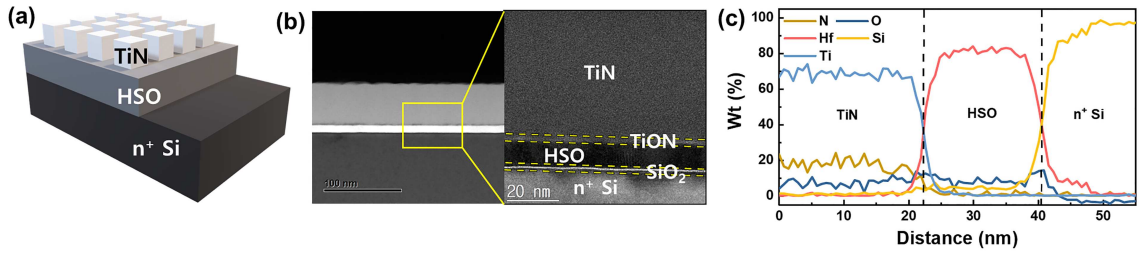

Figure 1 (Color online) (a) Three-dimensional schematic illustration of the TiN/HSO/n$^+$ Si structure; (b) cross-sectional TEM image; (c) EDS line scan of the device deposited TiN top electrode at 130 W.

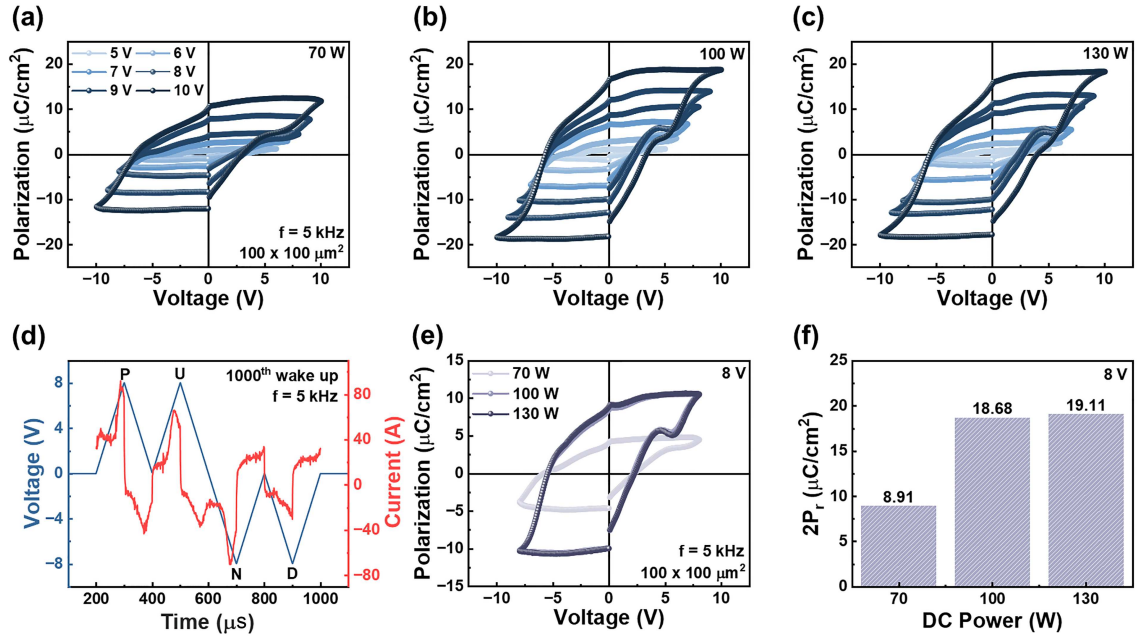

Figure 2 (Color online) P-V curves depending on different DC power of (a) 70 W, (b) 100 W, and (c) 130 W; (d) pulse scheme of PUND and current response; (e) PV curves of 70, 100, and 130 W at 8 V; (f) comparison of extracted $2P_r$ values according to DC power.

Si interface suggests that the native oxide initially present on the n$^+$ Si substrate surface was not completely removed prior to HSO deposition, or that reoxidation of the Si surface occurred during subsequent thermal processing [18]. Both of these interfacial layers are typically non-ferroelectric and act as 'dead layers' in series with the HSO film, which can significantly impact the device's overall capacitance and measured ferroelectric properties [19]. The energy-dispersive X-ray spectroscopy (EDS) line scan data shown in Figure 1(c) provided the atomic percentages of each element within the MFS device.

Figures 2(a)–(c) display the polarization-voltage (P-V) curves of devices with top electrodes deposited at 70, 100, and 130 W. The P-V curves were evaluated using the PUND method, which applies four triangular pulses at a frequency of 5 kHz, as illustrated in Figure 2(d), and represent the outcome of 1000 wake-up cycles at 6 V [20]. In Figure 2(e), a representative comparison of the $2P_r$ values was made from the P-V curves of devices with TiN top electrodes deposited at 70, 100, and 130 W, using an arbitrarily chosen voltage of 8 V. A graph providing the quantitative evaluation of these values is presented in Figure 2(f). The results show $2P_r$ values of 8.91, 18.68, and 19.11 μC/cm$_2$ for devices deposited at 70, 100, and 130 W, respectively. These findings suggest that TiN deposition at 130 W is the optimal DC power for forming the top electrode.

To examine the impact of different DC power levels (70, 100, and 130 W) on the crystalline structure of the HSO thin films, GIXRD analysis was performed in the 2θ range of 27°–39°. As shown in Figure 3(a), peaks corresponding to the m- (-111), o- (111)/t- (011), m- (111), and o- (200) phases were observed in all devices. Diffraction peaks associated with the non-centrosymmetric o- (111) phase were present in all three devices, indicating the ferroelectric properties of the HSO film. The peak observed near 31° consists of a mixture of t- and o-phases, with its intensity varying depending on the DC power applied.

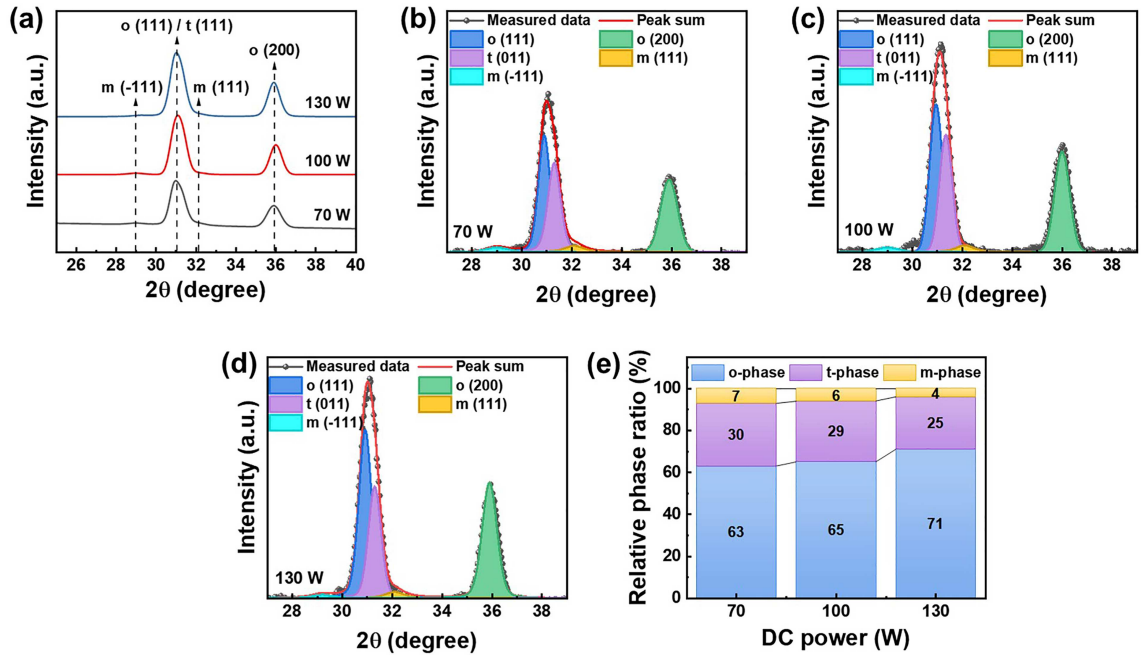

Figure 3 (Color online) (a) GIXRD spectra of devices deposited at 70, 100, 130 W; GIXRD peak spectra representing (b) 70 W, (c) 100 W, (d) 130 W; (e) the proportion of o-, t-, and m-phases in the devices according to DC power.

To distinguish between the o- and t-phases, Gaussian peak fitting was performed to separate the peaks in the vicinity of 31° for each sample, as shown in Figures 3(b)–(d). For a thorough comparison of the phase ratios, the m-, t-, and o- (200) phases were also analyzed using the same separation method. The ratios of each phase were determined from the integrated peak intensities corresponding to the o-, t-, and m-phases in the GIXRD pattern, as depicted in Figure 3(e). The analysis revealed that, consistent with the previously analyzed $2P_r$ results, the o-phase ratio at 130 W was 8% higher than that at 70 W and 6% higher than that at 100 W. In contrast, the t-phase ratio was the lowest under the 130 W condition, which coincided with an increase in the o-phase ratio. This shift in phase distribution suggests that relatively higher tensile stress was induced in the HSO film grown under the 130 W condition. It has been reported in several studies that tensile stress promotes the formation or stabilization of the ferroelectric o-phase in HfO_2-based thin films [11, 21]. It is generally known that an increase in DC sputtering power alters the deposition environment, such as substrate temperature and plasma ion energy, which in turn can affect the film's microstructure and the residual stress (including both intrinsic and thermal components) within the film stack [22, 23]. Therefore, the enhanced crystallization of the o-phase observed under the 130 W condition is interpreted as being primarily due to the increased tensile stress induced by the higher deposition power used during TiN layer formation.

To analyze the non-ferroelectric characteristics of HSO-based devices under various DC power conditions, we employed a short pulse switching technique based on polarization reversal theory [24, 25]. Assuming that the C_i holds a fixed, time-independent value, the capacitive charging current operates under a constant R_LC_i condition. Figures 4(a)–(c) illustrate the time-dependent switching current (I_{sw}) for different DC powers. For initial state setup, each device received a 10 μs negative square pulse to align all dipoles in a uniform direction. Subsequently, we applied a positive pulse with gradually increasing amplitude from 7 to 8.2 V in 0.2 V increments to measure the I_{sw}. At the start of the pulse, all devices exhibited a sharp rise in current similar to the capacitive charging process, followed by an exponential decrease in current after charging, indicating a discharge phenomenon. The time dependence of I_{sw} can be described by the following equation, as derived from polarization reversal theory [26, 27]:

$$I_{sw}(t) = I_{sw}^0 \mathrm{e}^{-(t-t_0)/(R_LC_i)}, \quad t_0 \leqslant t \leqslant t_{sw}, \tag{1}$$

where the parameter I_{sw}^0 represents the current at the initiation of the ferroelectric switching process, while t_0 and t_{sw} correspond to the times marking the start and end of ferroelectric switching, respectively. In this context, R_L denotes the total possible resistance and C_i represents the non-ferroelectric interfacial capacitance. For all fabricated devices under the tested conditions, the switching process was observed to

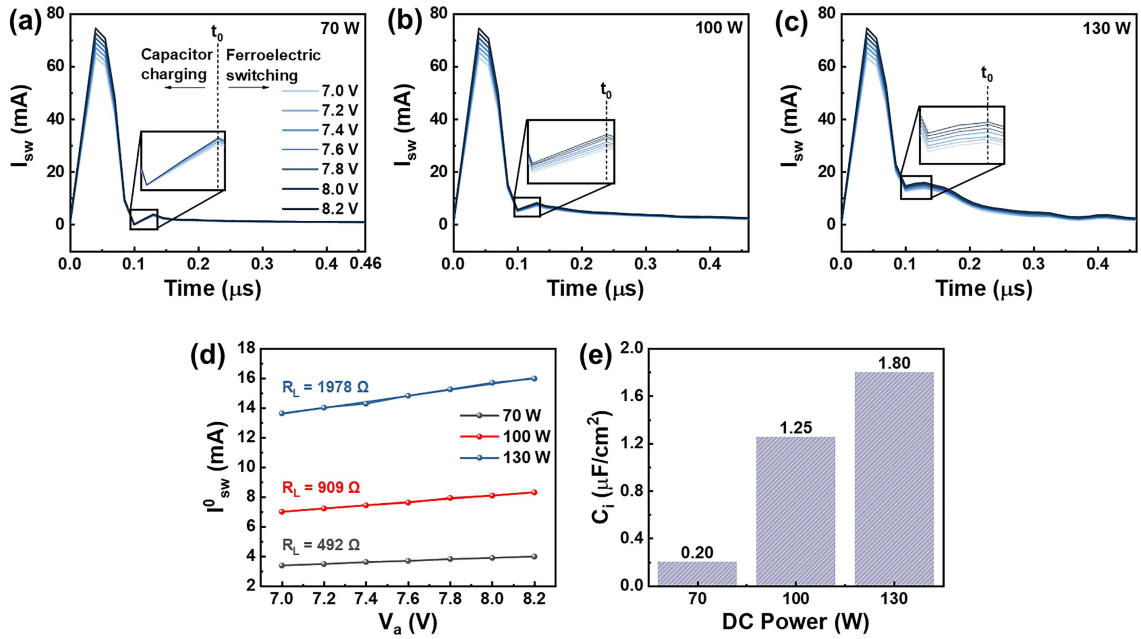

Figure 4 (Color online) Transient switching currents measured with a 7–8.2 V write pulse from devices with top electrode TiN deposited at different DC powers: (a) 70 W, (b) 100 W, (c) 130 W; (d) extracted initial switching current (I_{sw}^0) as a function of the applied voltage for each DC power condition; (e) calculated C_i values for different DC power levels under various process conditions.

complete at approximately $t_{sw} = 0.46$ μs. This theoretical model is particularly applicable from the onset of the ferroelectric switching event, as illustrated by the decay trend of the switching current through the ferroelectric layer in Figure S2.

The initial switching current, I_{sw}^0, can be determined as follows:

$$I_{sw}^0(t) = \frac{V_a - V_c}{R_L}, \tag{2}$$

where V_a and V_c represent the applied and coercive voltages, respectively. Figure 4(d) displays the I_{sw}^0-V_a curves for each device, from which the value of R_L was determined based on the slope. Specifically, the extracted R_L values were found to be 1978, 909, and 492 Ω for the devices fabricated with 70, 100, and 130 W DC power, respectively. Finally, C_i was calculated by dividing the time constant obtained from Figure S2 by R_L. Figure 4(e) illustrates the C_i values calculated for all devices, ordered in magnitude as follows: 130, 100, and 70 W. The quantitative C_i results for devices deposited at various DC power levels align with the findings from the P-V curves. The device with the top electrode deposited at 130 W exhibits the highest C_i value, indicating the presence of the thinnest dead layer and enhanced crystallinity and phase formation of ferroelectric HfO_2.

Consequently, as inferred from the C_i comparisons in this study, an optimal DC power of 130 W for the HSO layer deposition is effectively emphasized. To investigate the influence of deposition power on atomic composition and distribution in the TiN/HSO/n^+ Si device stack, X-ray photoelectron spectroscopy (XPS) depth profiling was conducted, focusing particularly on the TiN top electrode (TE) layer with deposition powers set at 70, 100, and 130 W.

Figures 5(a)–(c) show the XPS depth profiles of TiN electrodes deposited at 70, 100, and 130 W, highlighting compositional changes with power levels. Figure 5(d) summarizes the Ti and N atomic concentrations, where the Ti/N ratio was observed to be the lowest at 130 W (1.50) compared with 1.94 and 1.74 at 70 and 100 W, respectively. Figures 5(e) and (f) show the atomic distributions of O and N within the depth profiles, respectively. The electrode deposited at a DC power of 130 W, with a low Ti/N ratio, alleviated the oxygen scavenging behavior of Ti, which is a common issue in TiN electrodes, thereby limiting oxygen absorption [28–30]. This reduction in oxygen incorporation is beneficial because it decreases the formation of oxygen vacancy defects in the HSO layer, which are known to contribute to leakage current and reduced reliability in ferroelectric devices [31, 32]. Although some oxygen incorporation and residual oxygen vacancies remained, these were reduced compared with the

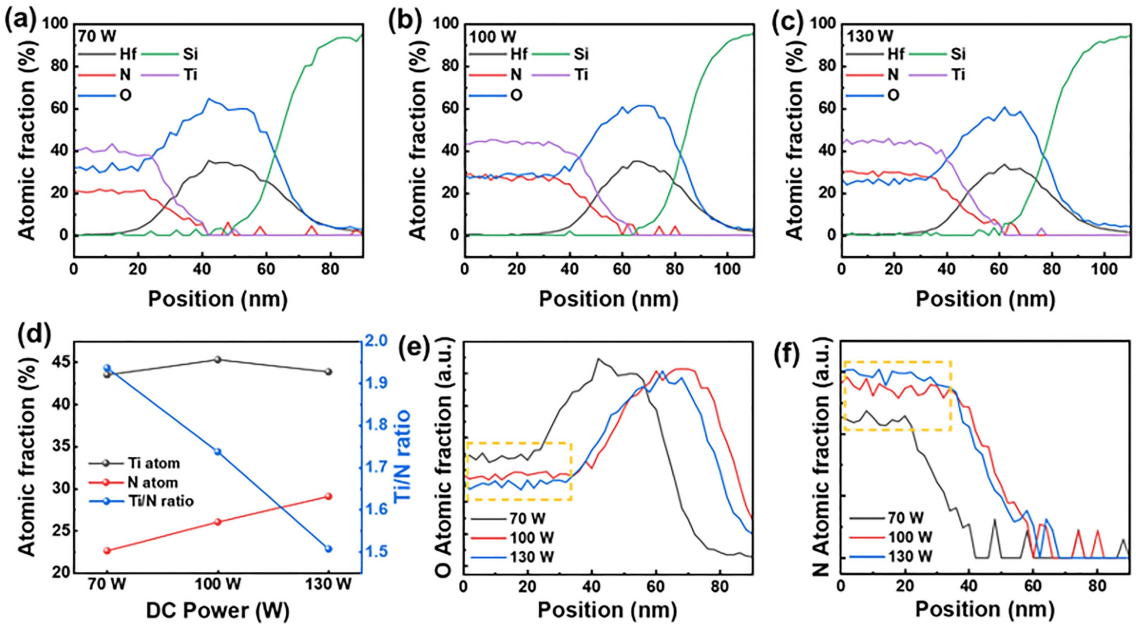

Figure 5 (Color online) Elemental composition of the XPS depth profile of the device with deposited top electrode TiN at (a) 70 W, (b) 100 W, (c) 130 W; (d) Ti and N atomic concentrations and Ti/N ratio as a function of DC power; depth profile of (e) O atomic fraction and (f) N atomic fraction at different DC powers.

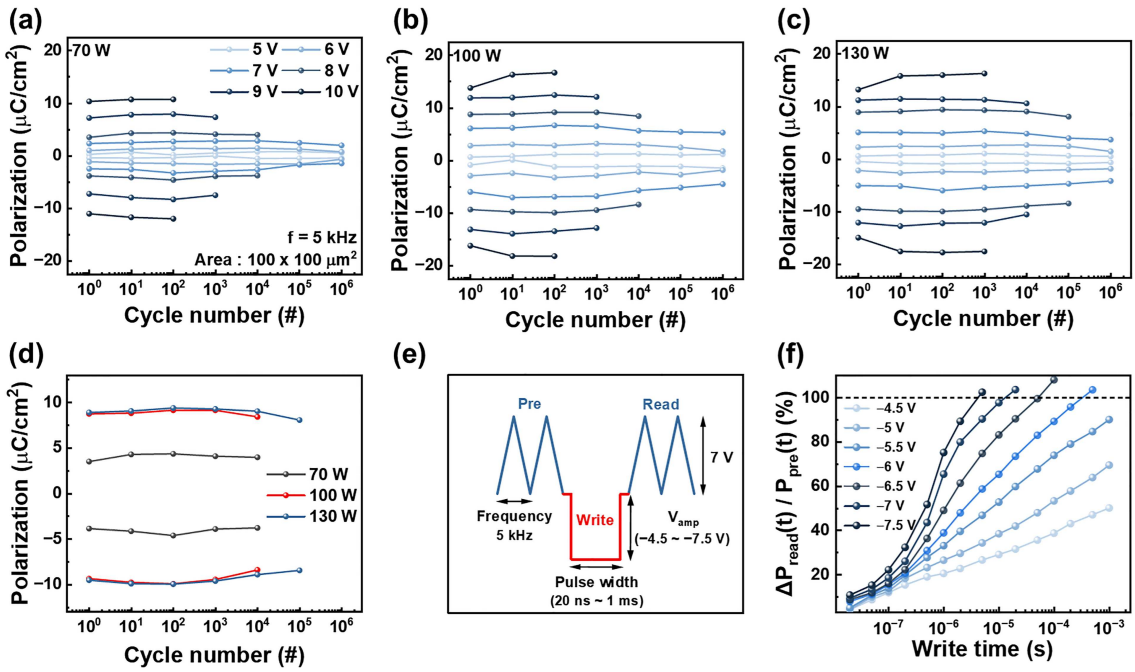

Figure 6 (Color online) Endurance characteristics at various voltages (5–10 V) at (a) 70 W, (b) 100 W, (c) 130 W, (d) comparison of endurance characteristics at 8 V; (e) pulse scheme of switching speed; (f) time-dependent switched polarization responses following the application of various switching pulse widths and heights.

lower DC power samples. As a result, devices with 130 W electrodes exhibited lower leakage current and improved stability compared with devices fabricated at 70 and 100 W, showing the potential for optimizing TiN electrode configurations despite some remaining challenges. Therefore, 130 W deposition appears to be the most favorable condition for reliable device operation.

The endurance performance of the TiN/HSO/n^+ Si device stack with varying TiN deposition powers is presented in Figures 6(a)–(c). Figures 6(a)–(c) display endurance measurements recorded at 1 V intervals from 5 to 10 V for devices with TiN top electrodes deposited at 70, 100, and 130 W, respectively. Across

all power settings, the endurance profiles demonstrate three distinct phases: the wake-up, stable, and fatigue stages [32, 33]. This phase progression is evidenced by an initial increase in P_r in the wake-up stage, driven by the redistribution of oxygen vacancies and the shift toward the orthorhombic (o-) phase, followed by a stabilization of P_r in the stable stage, and ultimately, a decline in P_r values during the fatigue stage due to defect accumulation and charge trapping effects within the material [34–36].

In Figure 6(d), endurance comparisons at a fixed 8 V across the three deposition DC powers (70, 100, and 130 W) highlight that the 130 W deposition power achieved the best endurance performance. As discussed in the XPS depth profiles in Figures 5(a)–(c), the TiN electrode deposited at 130 W exhibits a lower Ti/N ratio (1.50) than those deposited at 70 and 100 W, correlating with a higher nitrogen atomic content and lower oxygen atomic content. This increased nitrogen content effectively limits oxygen scavenging from the ferroelectric HSO layer by reducing the oxygen-scavenging behavior of Ti. As a result, the device deposited at 130 W shows reduced oxygen vacancy defects and enhanced stability during cycling, ultimately improving endurance by mitigating the degradation mechanisms that lead to fatigue. These findings indicate that optimizing the TiN deposition power, specifically to 130 W, enhances the endurance of the device by fostering a stable electrode composition that limits defect formation and maintains polarization over extended cycling [37]. This optimization could be essential for achieving reliable, nonvolatile performance in ferroelectric-based devices. One of the advantages of ferroelectricity is its fast switching speed. The switching speed characteristics of the device were evaluated using a specific pulse scheme illustrated in Figure 6(e). The switching procedure started by applying two consecutive positive triangular pulses to establish the initial polarization state within the ferroelectric layer. This pre-conditioning step is critical for aligning the ferroelectric regions and preparing the device for subsequent switching operations. A negative square pulse was then applied to induce polarization inversion, which is essential for evaluating ferroelectric switching dynamics. Subsequently, a continuous positive triangular pulse was subsequently applied to accurately capture the switching response. Similar to the PUND method used in polarization studies, the ferroelectric switching current can be measured while minimizing the effect of leakage current [20,38,39]. This combination of pulse sequences effectively demonstrates the capacity of the device for fast switching and the dynamics of the polarization changes within the HSO layer. Figure 6(f) shows the degree of polarization reversal normalized, with the HSO device starting to switch at an astonishing rate of 100 ns. In addition, this curve shows the effect of pulse voltage and width on ferroelectric switching. The normalized polarization is plotted against the switching time, showing a clear increase in polarization as the pulse width and amplitude increase [40–42]. This behavior not only confirms the fast switching rate of the device but also highlights the efficacy of the pulse regime in achieving significant polarization inversion within the ferroelectric layer.

The MFS-based ferroelectric memristors exhibit unique resistance-switching characteristics, transitioning between high-resistance (HRS) and low-resistance (LRS) states depending on the applied voltage. These characteristics, influenced by the device's band structure and polarization alignment, give rise to various conduction mechanisms under specific voltages and temperatures, which are crucial for achieving high TER for non-volatile memory applications. According to quantum mechanics, in MFS-based ferroelectric memristors, the band alignment and orientation of the polarization vector determine the barrier height and width at the metal/ferroelectric and ferroelectric/semiconductor interfaces, thereby regulating electron tunneling behavior [43].

As shown in Figures 7(a)–(c), low V_{read} values in HRS (Figure 7(a)) align the ferroelectric polarization from the n^+ Si substrate toward the TiN electrode, creating a depletion region that increases the barrier height and width, thus suppressing tunneling. At higher V_{read} values in HRS (Figure 7(b)), the electric field is enhanced, narrowing the tunneling width and allowing Fowler-Nordheim (F-N) tunneling through a triangular barrier. In LRS, applying a positive voltage to the top electrode reverses the polarization, lowering the barrier height and enhancing current flow, as shown in Figure 7(c). This polarization alignment effectively modulates the conduction path, allowing precise control of resistance states via the applied voltage.

Figures 7(d)–(f) analyze the tunneling mechanisms based on current-voltage (I-V) characteristics at different temperatures, focusing on the transition between resistance states and the relationship with polarization alignment. In HRS, conduction mechanisms were measured from 300 to 360 K in 20 K intervals. The current equations for F-N and direct tunneling (DT), expressed as

$$I_{\text{F-N}} = \frac{q^2}{8\pi h\phi_B} V^2 \exp\left(\frac{-8\pi\sqrt{2qm^*}}{3hV}\phi^{3/2}\right), \tag{3}$$

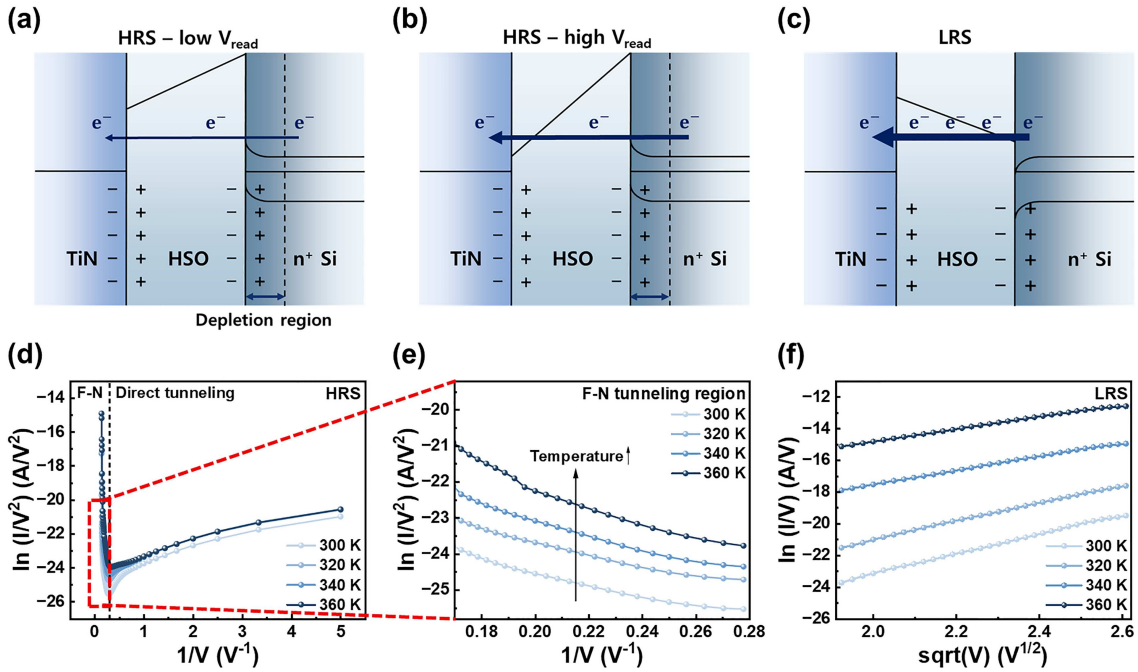

Figure 7 (Color online) Band diagram and polarization vector of the (a) HRS at low V_{read} values, (b) HRS at high V_{read} values, (c) LRS; (d) F-N tunneling and direct tunneling curve fitting of the HRS; (e) enlarged region of F-N tunneling; (f) P-F emission curve fitting of the LRS.

$$I_{\text{DT}} \propto V \exp\left(\frac{-2d\sqrt{2m^*\phi}}{h}\right) \tag{4}$$

were used to fit $\ln(I/V^2)$ versus $1/V$ [44], where q is the elementary electronic charge, h is Planck's constant, ϕ_B is the constant band offset, V is the applied voltage, m^* is the effective mass of an electron, d is the ferroelectric layer thickness, and ϕ is the barrier height.

The fitting results show that at low V_{read} values, DT is dominant because electrons find it difficult to directly traverse the relatively thick ferroelectric layer (10 nm) and depletion layer, as illustrated in the band diagram in Figure 7(a). Figure 7(d) displays an increase in $\ln(I/V^2)$ with temperature, which suggests that although DT and F-N mechanisms are generally temperature-independent, the observed temperature dependence in HRS implies the possible involvement of trap-assisted tunneling (TAT). Trap states in the ferroelectric layer may create intermediate energy states that facilitate tunneling, introducing a temperature-dependent current component [43, 45]. As V_{read} increases, the effective barrier narrows, and the mechanism transitions to F-N tunneling. At higher bias, the reduced tunneling width leads to increased electron tunneling, as confirmed by the band diagram in Figure 7(b) [46]. Figure 7(e) exhibits a linear relationship characteristic of F-N tunneling. However, the temperature dependence suggests the involvement of traps, distinguishing it from purely quantum-mechanical mechanisms.

Finally, in LRS, the significant increase in current with temperature indicates that Poole-Frenkel (P-F) emission is the primary conduction mechanism rather than tunneling [47]. P-F emission, a process wherein electrons are thermally excited from traps and the electric field reduces the trap energy barrier, is depicted in Figure 7(c). Figure 7(f) demonstrates the thermal and field effects on P-F emission, with

$$J_{\text{P-F}} = q\mu N_C \exp\left(\frac{-q(\phi_T - \sqrt{qE/\pi\varepsilon})}{kT}\right) \tag{5}$$

used to fit $\ln(I/V)$ versus $\sqrt{V}$, illustrating both linearity and temperature dependence, where q is the elementary electronic charge, μ is the electron drift mobility, N_C is the density of states in the conduction band, E is the applied electric field, ϕ_T is the trap depth, k is Boltzmann's constant, and T is the absolute temperature. This fitting reveals a linear relationship and temperature dependence, affirming P-F emission's role in LRS.

Figures S3(a)–(c) respectively display the hysteretic tunneling currents for devices with top electrodes deposited at 70, 100, and 130 W. The TiN top electrode underwent continuous double-sweep voltage

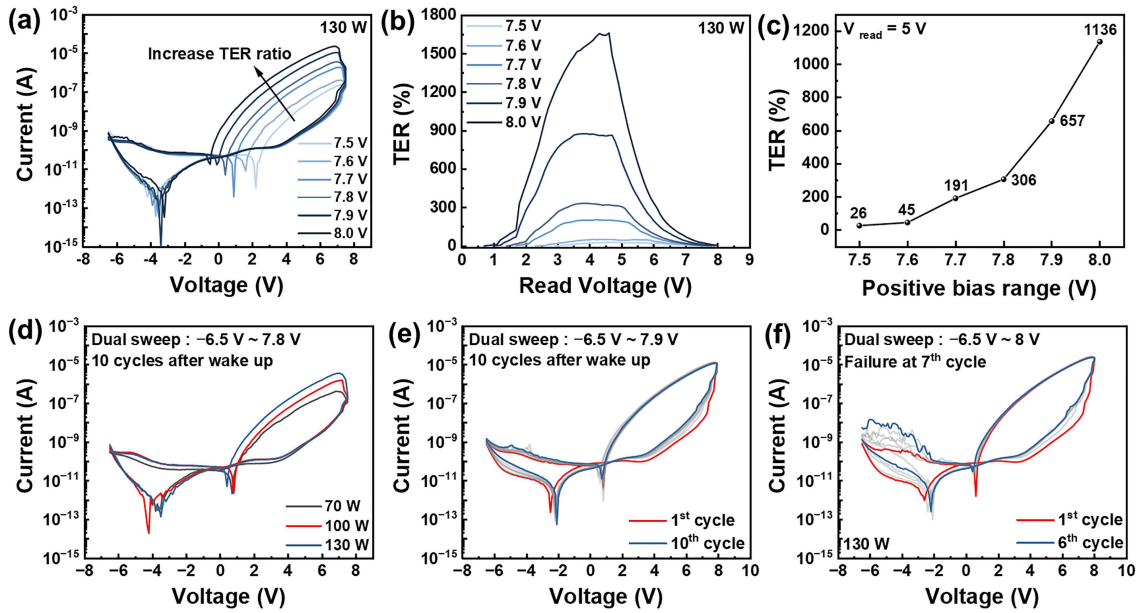

Figure 8 (Color online) (a) I-V curves with dual sweep after wake-up in the multi-level bias (ranging from 7.5 to 8 V in 0.1 V step), of the device deposited with top electrode at 130 W; (b) tunneling electro-resistance (TER) variation of the device deposited at 130 W; (c) quantitative TER ratio value based on the positive bias range; (d) hysteretic tunneling I-V responses comparison of the devices deposited with top electrode at 70, 100, and 130 W; (e) hysteretic tunneling I-V responses of the device deposited with top electrode at 130 W: ten cycles after wake-up at 7.9 V; (f) different cycles indicating a breakdown at the 7th cycle when sweeping at 8 V.

application, ranging from −6.5 to 7.5 V, followed by a reverse sweep from 7.5 V back to −6.5 V. These I-V results demonstrate rectifying characteristics, with suppressed currents under negative bias, attributed to an additional depletion layer formed at the n^+ Si interface due to the MFS structural properties [45,48,49]. Furthermore, to observe tunneling efficiency, a series of 10 continuous cycles was conducted. As shown in Figure S3, the device fabricated under 130 W conditions exhibited a larger memory window in the I-V curve and a higher TER value than other devices. A detailed comparison of TER values across the three devices fabricated under varying process conditions can be seen in Figures S3(g)–(i).

Figure 8(a) illustrates the hysteretic tunneling current behavior for the device with a top electrode deposited at 130 W, under sweeping voltages that increase incrementally by 0.1 V [50]. The applied voltage progresses from negative to positive, then returns from positive to negative. As the HfO_x-based ferroelectric layer has a polycrystalline structure and operates through a domain-switching mechanism, the on-current tends to increase as the voltage rises. With higher applied voltages, more domains undergo switching [51].

Figure 8(b) presents the TER values of this device as the positive voltage increases from 7.5 to 8 V. The TER values were calculated using

$$\mathrm{TER} = \frac{I_{\mathrm{LRS}} - I_{\mathrm{HRS}}}{I_{\mathrm{HRS}}}. \tag{6}$$

In Figure 8(c), the increase in TER values for the device with a 130 W top electrode deposition is shown in response to an increased positive bias (7.5–8 V). This indicates that the TER increases linearly with the difference between the on-state and off-state currents. As the applied voltage increases, the TER rises from 26 to 1136. However, at 8 V, a non-ideal TER was observed. To verify repeatability, continuous cycling tests were performed at both 7.9 and 8 V, with results shown in Figures 8(e) and (f). After six cycles at 8 V, the device experienced breakdown due to the high bias field, likely caused by random defects within the ferroelectric film forming unintended current pathways [52]. These findings suggest that 7.9 V is the optimal operating voltage to achieve reliably high TER.

Figure 9 presents the synaptic characteristic results obtained from the device fabricated with the top electrode deposited at 130 W, which demonstrated optimal performance in the prior analyses. Figure 9(b) highlights the PPF effect, a type of short-term plasticity that influences synaptic strength by varying the interval between two identical set pulses (10 V amplitude, 1 ms duration). PPF serves as an essential

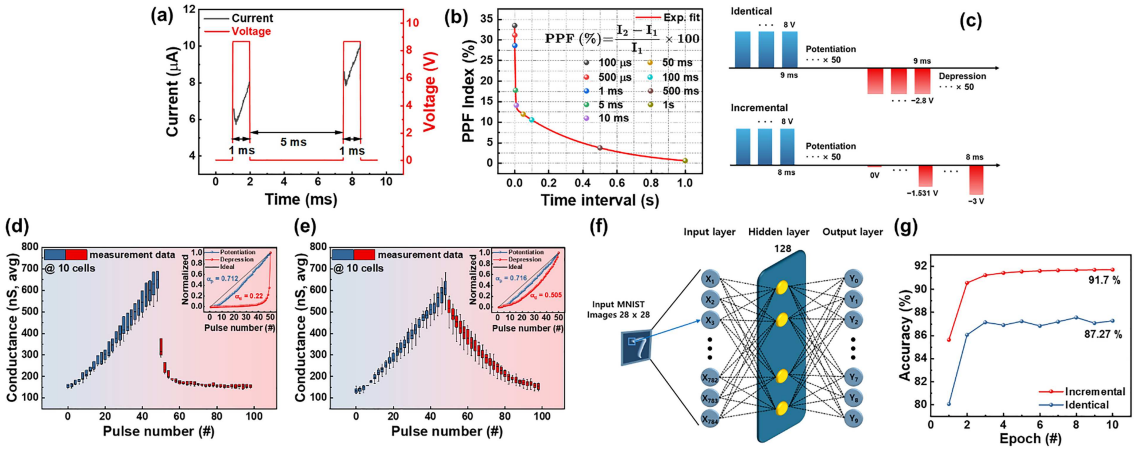

Figure 9 (Color online) (a) Pulse scheme of PPF; (b) PPF behavior as a function of the interval time; (c) identical and incremental pulse scheme of P&D; merged data of P&D of ten cells using (d) identical pulse and (e) incremental pulse; (f) schematics of a simulation framework for MNIST pattern recognition using a neural network; (g) pattern recognition accuracy of the identical and incremental models.

learning mechanism for processing and transmitting information, mimicking neurotransmitter diffusion at biological synapses and producing changes in synaptic plasticity. In this phenomenon, neural facilitation occurs as successive presynaptic stimulation gradually raises the excitatory postsynaptic potential.

To quantitatively analyze the PPF effect, intervals between pre- and post-pulses were adjusted from 100 μs to 1 s, with results expressed as the PPF index in Figure 9(a) [53,54]. The PPF index, representing the degree of excitatory influence, decreases with increasing intervals and is calculated by the following formula:

$$\text{PPF index} = \frac{I_2 - I_1}{I_1} \times 100\ (\%), \tag{7}$$

where I_1 and I_2 denote the average current values from the pre- and post-pulse, respectively [55]. The data shows that facilitation peaks at 33.4% when the interval is 100 μs and subsequently decreases exponentially with longer intervals. At the maximum interval of 1 s, the post-pulse current response remains nearly unchanged from the pre-pulse response. This study reflects the excitatory processes of synaptic plasticity in the human brain and demonstrates the role of short-term adaptation in neuronal activity [56].

Neuromorphic computing seeks to replicate the information processing structure of the human brain by incorporating synaptic properties into hardware devices. A central feature of neuromorphic systems is the simulation of synaptic plasticity, where P&D, mechanisms that represent the strengthening and weakening of synaptic weights, are used to imitate the brain's learning processes [57]. The device stack in this study, which utilizes ferroelectric memristor technology with TiN/HSO/n^+ Si, demonstrates this synaptic behavior by reproducing multi-level conductance states that correspond to varying synaptic weights.

Figures 9(c)–(g) present a detailed investigation into the effects of two pulse schemes on synaptic behavior: the identical pulse and the incremental pulse. Figure 9(c) illustrates the pulse schemes for each approach [58]. For the identical pulse scheme, a pulse train is presented consisting of 50 pulses set at 8 V and 50 pulses set at −2.8 V, each with a constant pulse width of 9 ms. In contrast, the incremental pulse scheme displays a sequence of 50 pulses at 8 V, 50 pulses at −2.8 V, and an additional 50 reset pulses decreasing from 0 to −3 V, with each pulse having a consistent width of 8 ms. Figures 9(d) and (e) present the results of applying the identical and incremental pulses across 10 cells consistently, visualized through box plots. Quantitative analysis of P&D linearity was performed using

$$G = \begin{cases} \left[\left(G_{\text{LRS}}^{\alpha} - G_{\text{HRS}}^{\alpha}\right) \cdot w + G_{\text{HRS}}^{\alpha}\right]^{1/\alpha}, & \text{if } \alpha \neq 0, \\ G_{\text{HRS}} \cdot \left(\frac{G_{\text{LRS}}}{G_{\text{HRS}}}\right)^{w}, & \text{if } \alpha = 0 \end{cases} \tag{8}$$

in MATLAB R2024a software, employing conductivity changes as variables [59], where G_{LRS} and G_{HRS} represent the conductance values at the maximum and minimum levels, respectively. The parameter α is a critical fitting factor for evaluating the linearity of weight updates, while w serves as an internal variable

that varies within the model. Ideally, a value of $\alpha = 1$ indicates a perfectly linear change in conductance. In Figure 9(d), the α value for the identical pulse approach is found to be 0.712 during potentiation and 0.22 during depression. In contrast, for the incremental pulse scheme, the α values are 0.716 for potentiation and 0.505 for depression, as shown in Figure 9(e). The application of incremental pulses results in a conductance response with greater linearity and symmetry than that of identical pulses. This outcome suggests that adjusting the reset pulse during depression improves the linearity of the parameter α.

In this study, we propose a neural network model incorporating P&D processes to manipulate the pixel values in a 28×28 MNIST image dataset as shown in Figure 9(f). Conductance normalization is applied using the following equation:

$$\omega = \frac{G - G_{\min}}{G_{\max} - G_{\min}}, \tag{9}$$

where $G_{\max}$ and $G_{\min}$ represent the maximum and minimum conductance values, respectively [60–62]. During each P&D pulse, the respective conductance values are monitored, and the normalized conductance values, denoted as synaptic weights (ω), undergo MNIST simulations. Synaptic weights are aligned across layers to minimize discrepancies between input and output values, enabling progressive weight updates [62]. Normalization of conductance values plays a crucial role, as neural network activation functions depend on specific input ranges. Proper normalization prevents gradient-related issues like vanishing or exploding values during backpropagation, which, when P&D graphs display symmetry and linearity, translates to reduced image modification.

In Figure 9(g), the network is trained over 60000 iterations with an architecture comprising 784 input neurons, followed by a hidden layer with 128 neurons. Results are validated through 10 output neurons. Testing on 10000 ideal images over 10 epochs shows that the identical pulse approach achieves 87.27% pattern accuracy, while the incremental pulse scheme, designed to enhance linearity, achieves 91.7%. In Figure S4, confusion matrices illustrate the increased accuracy with the incremental approach, recording mean accuracy scores of 87.79% for identical pulses and 91.67% for incremental pulses.

4 Conclusion

In this work, we fabricated HSO-based ferroelectric memristor devices utilizing TiN/HSO/n^+ Si stacks to investigate their high ferroelectric properties. Through optimization of the deposition conditions for the TiN top electrode, specifically by using a DC power of 130 W, we achieved the highest P_r and C_i values, which resulted in enhanced device performance, characterized by a high TER, endurance, and fast switching speeds. The reduced Ti/N ratio at this deposition power minimized oxygen scavenging effects, mitigating defect formation in the HSO layer and thereby enhancing the overall performance of the device. Additionally, the device exhibited consistent and dependable synaptic behaviors, including P&D, which had a considerable impact on the cell-to-cell variation and the linearity of the online learning process. The findings from this study validate that the ferroelectric memristor device reliably functions as a memory element in artificial synapse applications. Consequently, this research significantly advances the development of robust and efficient ferroelectric memristor memory components for future neuromorphic systems.

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Supporting information Figures S1–S4. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Goh Y, Hwang J, Jeon S. Excellent reliability and high-speed antiferroelectric $HfZrO_2$ tunnel junction by a high-pressure annealing process and built-in bias engineering. ACS Appl Mater & Interf, 2020, 12: 57539–57546
2 Barrionuevo D, Zhang L, Ortega N, et al. Enhanced tunneling electroresistance in Pt/PZT/LSMO ferroelectric tunnel junctions in presence of magnetic field. Integrated Ferroelectrics, 2016, 174: 174–185
3 Imam M, Stojić N, Binggeli N. Ferroelectric switching of band alignments in LSMO/PZT/Co multiferroic tunnel junctions: an ab initio study. Nanotechnology, 2017, 28: 315202
4 Wang Z H, Zhao W S, Kang W, et al. Write operation study of Co/BTO/LSMO ferroelectric tunnel junction. J Appl Phys, 2013, 114: 044108
5 Mittermeier B, Dörfler A, Horoschenkoff A, et al. CMOS compatible $Hf_{0.5}Zr_{0.5}O_2$ ferroelectric tunnel junctions for neuromorphic devices. Adv Intell Syst, 2019, 1: 1900034
6 Luo Q, Cheng Y, Yang J, et al. A highly CMOS compatible hafnia-based ferroelectric diode. Nat Commun, 2020, 11: 1391

7 Liu K Q, Dang B J, Yang Z Y, et al. Tuning the ferroelectricity of $Hf_{0.5}Zr_{0.5}O_2$ with alloy electrodes. Sci China Inf Sci, 2024, 67: 182402
8 Xiao M, Hellenbrand M, Strkalj N, et al. Ultra-fast non-volatile resistive switching devices with over 512 distinct and stable levels for memory and neuromorphic computing. Adv Funct Mater, 2025: 2418980
9 Iliasov A I, Matsukatova A N, Emelyanov A V, et al. Adapted MLP-mixer network based on crossbar arrays of fast and multilevel switching $(Co\text{-}Fe\text{-}B)_x(LiNbO_3)_{100-x}$ nanocomposite memristors. Nanoscale Horiz, 2024, 9: 238–247
10 Goh Y, Hwang J, Kim M, et al. Selector-less ferroelectric tunnel junctions by stress engineering and an imprinting effect for high-density cross-point synapse arrays. ACS Appl Mater Interf, 2021, 13: 59422–59430
11 Joh H, Jung T, Jeon S. Stress engineering as a strategy to achieve high ferroelectricity in thick hafnia using interlayer. IEEE Trans Electron Devices, 2021, 68: 2538–2542
12 Lee Y, Song S, Ham W, et al. Si-doped HfO_2-based ferroelectric tunnel junctions with a composite energy barrier for non-volatile memory applications. Materials, 2022, 15: 2251
13 Cao R, Liu Q, Liu M, et al. Improvement of endurance in HZO-based ferroelectric capacitor using Ru electrode. IEEE Electron Device Lett, 2019, 40: 1744–1747
14 Zhou J, Zhou Z, Wang X, et al. Demonstration of ferroelectricity in Al-doped HfO_2 with a low thermal budget of 500°C. IEEE Electron Device Letters, 2020, 41: 1130–1133
15 Hong S, Lee Y, Ahn D, et al. Comparison of the evolution of internal bias field of doped hafnia ferroelectric capacitors for the field-cycling reliability. Appl Phys Lett, 2021, 118: 013504
16 Böscke T S, Müller J, Bräuhaus D, et al. Ferroelectricity in hafnium oxide thin films. Appl Phys Lett, 2011, 99: 102903
17 Yang K, Kim G Y, Ryu J J, et al. Wake-up-mitigated giant ferroelectricity in $Hf_{0.5}Zr_{0.5}O_2$ thin films through oxygen-providing, surface-oxidized W electrode. Mater Sci Semicon Proc, 2023, 164: 107565
18 Morita M, Ohmi T, Hasegawa E, et al. Growth of native oxide on a silicon surface. J Appl Phys, 1990, 68: 1272–1281
19 Stengel M, Spaldin N A. Origin of the dielectric dead layer in nanoscale capacitors. Nature, 2006, 443: 679–682
20 Ryu H, Xu K, Kim J, et al. Exploring new metal electrodes for ferroelectric aluminum-doped hafnium oxide. IEEE Trans Electron Devices, 2019, 66: 2359–2364
21 Shin S Y, Jang Y, Park J, et al. P-20: memory window and endurance improvement of In-Ga-Zn-O-based ferroelectric thin film transistors by inserting In-Ga-Zn-O floating gate. Symp Digest Tech Papers, 2024, 55: 1434–1437
22 Petrov I, Barna P B, Hultman L, et al. Microstructural evolution during film growth. J Vacuum Sci Tech A-Vacuum Surfs Films, 2003, 21: S117–S128
23 Abadias G, Chason E, Keckes J, et al. Stress in thin films and coatings: current status, challenges, and prospects. J Vacuum Sci Tech A-Vacuum Surfs Films, 2018, 36: 020801
24 Gaddam V, Das D, Jeon S. Insertion of HfO_2 seed/dielectric layer to the ferroelectric HZO films for heightened remanent polarization in MFM capacitors. IEEE Trans Electron Devices, 2020, 67: 745–750
25 Zhukov S, Genenko Y A, Hirsch O, et al. Dynamics of polarization reversal in virgin and fatigued ferroelectric ceramics by inhomogeneous field mechanism. Phys Rev B, 2010, 82: 014109
26 Lee Y, Goh Y, Hwang J, et al. The influence of top and bottom metal electrodes on ferroelectricity of hafnia. IEEE Trans Electron Devices, 2021, 68: 523–528
27 Kim H J, Park M H, Kim Y J, et al. A study on the wake-up effect of ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ films by pulse-switching measurement. Nanoscale, 2016, 8: 1383–1389
28 Chen H Y, Lu F H. Oxidation behavior of titanium nitride films. J Vacuum Sci Tech A-Vacuum Surfs Films, 2005, 23: 1006–1009
29 Lin Y J, Teng C Y, Chang S J, et al. Role of electrode-induced oxygen vacancies in regulating polarization wake-up in ferroelectric capacitors. Appl Surf Sci, 2020, 528: 147014
30 Filatova E O, Sakhonenkov S S, Konashuk A S, et al. Inhibition of oxygen scavenging by TiN at the TiN/SiO_2 interface by atomic-layer-deposited Al_2O_3 protective interlayer. J Phys Chem C, 2019, 123: 22335–22344
31 Dang Z, Lv S, Gao Z, et al. Improved endurance of $Hf_{0.5}Zr_{0.5}O_2$-based ferroelectric capacitor through optimizing the Ti-N ratio in TiN electrode. IEEE Electron Device Lett, 2022, 43: 561–564
32 Pešić M, Fengler F P G, Larcher L, et al. Physical mechanisms behind the field-cycling behavior of HfO_2-based ferroelectric capacitors. Adv Funct Mater, 2016, 26: 4601–4612
33 Chouprik A, Negrov D, Tsymbal E Y, et al. Defects in ferroelectric HfO_2. Nanoscale, 2021, 13: 11635–11678
34 Max B, Hoffmann M, Slesazeck S, et al. Direct correlation of ferroelectric properties and memory characteristics in ferroelectric tunnel junctions. IEEE J Electron Devices Soc, 2019, 7: 1175–1181
35 Shin W, Min K K, Bae J H, et al. $1/f$ noise in synaptic ferroelectric tunnel junction: impact on convolutional neural network. Adv Intell Syst, 2023, 5: 2200377
36 Shin W, Min K K, Bae J H, et al. Comprehensive and accurate analysis of the working principle in ferroelectric tunnel junctions using low-frequency noise spectroscopy. Nanoscale, 2022, 14: 2177–2185
37 Lee J, Yang K, Kwon J Y, et al. Role of oxygen vacancies in ferroelectric or resistive switching hafnium oxide. Nano Convergence, 2023, 10: 55
38 Anderson J D, Merkel J, Macmahon D, et al. Evaluation of $Si:HfO_2$ ferroelectric properties in MFM and MFIS structures. IEEE J Electron Devices Soc, 2018, 6: 525–534
39 Mueller S, Muller J, Hoffmann R, et al. From MFM capacitors toward ferroelectric transistors: endurance and disturb characteristics of HfO_2-based FeFET devices. IEEE Trans Electron Devices, 2013, 60: 4199–4205
40 Lee T, Lee K, Lim H, et al. Ferroelectric polarization-switching dynamics and wake-up effect in Si-doped HfO_2. ACS Appl Mater Interf, 2019, 11: 3142–3149
41 Li Y, Li J, Liang R, et al. Switching dynamics of ferroelectric HfO_2-ZrO_2 with various ZrO_2 contents. Appl Phys Lett, 2019, 114: 142902
42 Materano M, Lomenzo P D, Mulaosmanovic H, et al. Polarization switching in thin doped HfO_2 ferroelectric layers. Appl Phys Lett, 2020, 117: 262904
43 Hwang J, Goh Y, Jeon S. Physics, structures, and applications of fluorite-structured ferroelectric tunnel junctions. Small, 2024, 20: 2305271
44 Ryu H, Wu H, Rao F, et al. Ferroelectric tunneling junctions based on aluminum oxide/zirconium-doped hafnium oxide for neuromorphic computing. Sci Rep, 2024, 9: 20383
45 Lim E, Ju D, Lee J, et al. Artificial neural network classification using Al-doped HfO_x-based ferroelectric tunneling junction with self-rectifying behaviors. ACS Mater Lett, 2024, 6: 2320–2328
46 Liu Y, Cao Y, Zhu H, et al. $HfZrO_x$-based ferroelectric tunnel junction with crested symmetric band structure engineering. IEEE Electron Device Lett, 2021, 42: 1311–1314
47 Koo R H, Shin W, Jung G, et al. Stochasticity in ferroelectric memory devices with different bottom electrode crystallinity. Chaos Solitons Fractals, 2024, 183: 114861
48 Wen Z, Li C, Wu D, et al. Ferroelectric-field-effect-enhanced electroresistance in metal/ferroelectric/semiconductor tunnel junctions. Nat Mater, 2013, 12: 617–621
49 Goh Y, Jeon S. The effect of the bottom electrode on ferroelectric tunnel junctions based on CMOS-compatible HfO_2.

Nanotechnology, 2018, 29: 335201
50 Yu J, Min K K, Kim Y, et al. A novel physical unclonable function (PUF) using 16×16 pure-HfO_x ferroelectric tunnel junction array for security applications. Nanotechnology, 2021, 32: 485202
51 Li J, Ge C, Du J, et al. Reproducible ultrathin ferroelectric domain switching for high-performance neuromorphic computing. Adv Mater, 2020, 32: 1905764
52 Guo R, Lin W, Yan X, et al. Ferroic tunnel junctions and their application in neuromorphic networks. Appl Phys Rev, 2020, 7: 011304
53 Lai Q, Zhang L, Li Z, et al. Ionic/electronic hybrid materials integrated in a synaptic transistor with signal processing and learning functions. Adv Mater, 2010, 22: 2448–2453
54 John R A, Ko J, Kulkarni M R, et al. Flexible ionic-electronic hybrid oxide synaptic TFTs with programmable dynamic plasticity for brain-inspired neuromorphic computing. Small, 2017, 13: 1701193
55 Kim D, Kim J, Yun S, et al. Ferroelectric synaptic devices based on CMOS-compatible $HfAlO_x$ for neuromorphic and reservoir computing applications. Nanoscale, 2023, 15: 8366–8376
56 Yu T F, Chen H Y, Liao M Y, et al. Solution-processable anion-doped conjugated polymer for nonvolatile organic transistor memory with synaptic behaviors. ACS Appl Mater Interfaces, 2020, 12: 33968–33978
57 Lee G H, Kim T H, Song M S, et al. Effect of weight overlap region on neuromorphic system with memristive synaptic devices. Chaos Solitons Fractals, 2022, 157: 111999
58 Park Y, Lee J S. Artificial synapses with short- and long-term memory for spiking neural networks based on renewable materials. ACS Nano, 2017, 11: 8962–8969
59 Lin Y, Wang Z, Zhang X, et al. Photoreduced nanocomposites of graphene oxide/N-doped carbon dots toward all-carbon memristive synapses. NPG Asia Mater, 2020, 12: 64
60 Covi E, Brivio S, Fanciulli M, et al. Synaptic potentiation and depression in Al:HfO_2-based memristor. Microelectron Eng, 2015, 147: 41–44
61 Park J, Kim T H, Kwon O, et al. Implementation of convolutional neural network and 8-bit reservoir computing in CMOS compatible VRRAM. Nano Energy, 2022, 104: 107886
62 Jang J W, Park S, Burr G W, et al. Optimization of conductance change in $Pr_{1-x}Ca_xMnO_3$-based synaptic devices for neuromorphic systems. IEEE Electron Device Lett, 2015, 36: 457–459