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• Supplementary File •

Improved synaptic properties of $HfSiO_x$-based ferroelectric memristors by optimizing Ti/N ratio in TiN top electrode for neuromorphic computing

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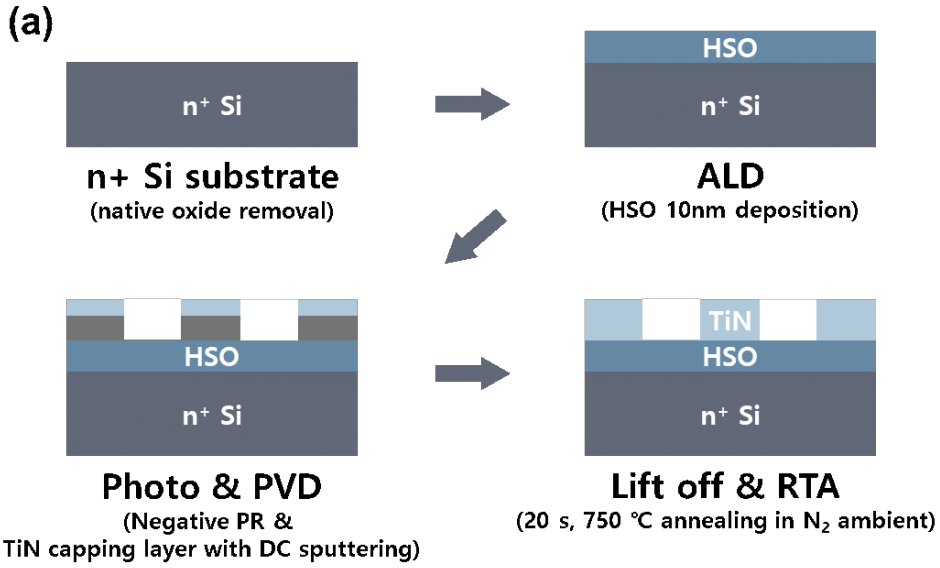

Figure S1 TiN/HSO/n+ Si device fabrication process flow.

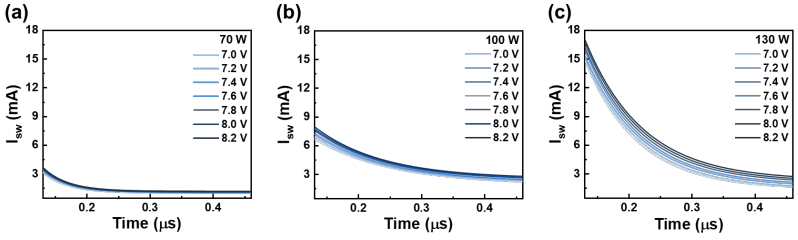

Figure S2 Exponentially fitted curves for devices with top electrode TiN deposited at (a) 70 W, (b) 100 W, and (c) 130 W.

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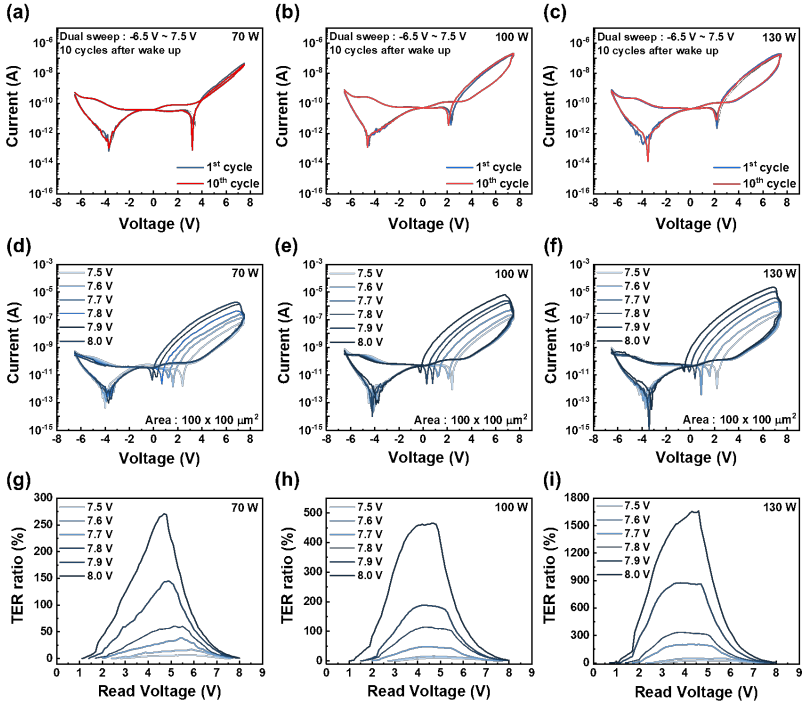

Figure S3 Hysteretic tunneling I-V responses of the device deposited with top electrode at (a) 70W, (b) 100 W, and (c) 130 W. I-V curve with dual sweep after wake-up in the multi-level bias at (d) 70 W, (e) 100 W, and (f) 130 W. TER variation depending on the bias range in the I-V curve at (g) 70 W, (h) 100 W, and (i) 130 W.

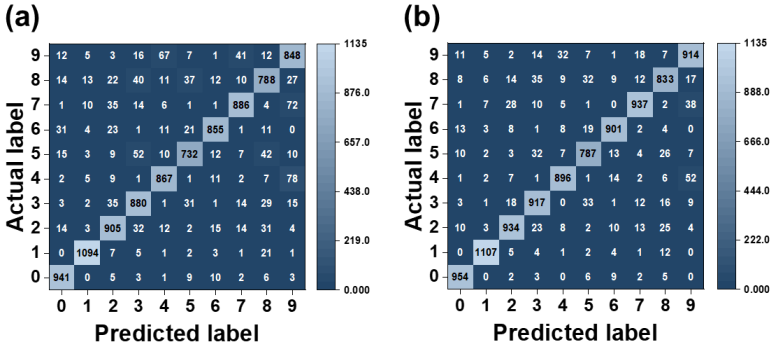

Figure S4 Confusion matrix after training for the (a) identical and (b) incremental models.