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3-bit memory operation of capacitor-less one-transistor one-diode DRAM cell

Seungho RYU[1], Kyoungah CHO[2*] & Sangsig KIM[1,2*]

[1]*Department of Semiconductor System Engineering, Korea University, Seoul 02841, Republic of Korea*
[2]*Department of Electrical Engineering, Korea University, Seoul 02841, Republic of Korea*

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Recently, capacitor-less two-transistor (2T0C) dynamic random-access memory (DRAM) cells have emerged as building blocks for next-generation DRAM applications due to their multibit operation, low power consumption, and the elimination of highly complex capacitor formation processes [1, 2]. Their multibit memory states can be read by sensing the magnitude of the output current (I_{OUT}), which is determined by the amount of charge stored in the storage node (SN). For 2T0C DRAM cells comprising oxide thin-film transistors (TFTs), the I_{OUT} magnitude has a nonlinear relationship with the SN charge. The nonlinear relationship is a hindrance on multibit memory operation; therefore, the different sensing margins between memory states result in unreliable memory operation. In 2T0C DRAM cells, the write devices require a low leakage current (I_{Leakage}) for retention characteristics, and the read devices require high on-current (I_{ON}) and on/off current ratios for multibit memory operation. Write and read devices should operate with different mechanisms to meet these requirements. Nevertheless, write and read devices in 2T0C DRAM cells were fabricated using the same channel material and operated by the same mechanism. Hence, we design a novel capacitor-less one-transistor one-diode (1T1D0C) DRAM cell that comprises an oxide TFT acting as a write device and a gated silicon diode acting as a read device. In this study, we fabricate a 1T1D0C DRAM cell with an integrated structure and evaluate its feasibility for 3-bit memory operation as a foundation for multibit memory operations.

Experiment. The key fabrication process of the 1T1D0C DRAM cell involves two primary parts: the first for fabricating the gated silicon diode and the second for fabricating the amorphous indium-tin-gallium-zinc oxide (a-ITGZO) TFT. The details of the fabrication process are described in Appendix A. All electrical measurements and characterizations were performed using a semiconductor parameter analyzer (HP4155C, Agilent), an LCR meter (HP4285A, Agilent), and a source meter (2636B, Keithley) at room temperature in a dark box. A cross-sectional image of the gated silicon diode was obtained using transmission electron microscopy (TEM, JEOL JEM-2100F, FEG) to validate the structural characteristics.

Results and discussion. Figure 1(a) shows a schematic of the 1T1D0C DRAM cell structure. As shown in the circuit diagram and optical image in Figure 1(b), the 1T1D0C DRAM cell consists of an a-ITGZO TFT and a double-gated silicon diode, the double gates of which are named gate1 (G1) and gate2 (G2). G1, connected to the source of the a-ITGZO TFT, serves as an SN for data storage, and G2 acts as a gate to induce the latch-up phenomenon, a unique feature of the gated silicon diode [3]. The write bit line (WBL) and write word line (WWL) are connected to the drain and gate of the a-ITGZO TFT, respectively, and the read bit line (RBL) is connected to the anode of the gated silicon diode. The optical image and channel cross-section transmission electron microscopy (TEM) image of the fabricated gated silicon diode are shown in Figure 1(c). The Ω-shaped polysilicon gate and SiO_2 gate dielectric structure surrounds the silicon channel region to enhance gate controllability. Figure 1(d) shows the drain-source current (I_{DS}) versus gate-source voltage (V_{GS}) characteristics of the a-ITGZO TFT at a drain-source voltage (V_{DS}) of 0.1 V. The linear mobility, subthreshold swing, and threshold voltage (V_{TH}) are estimated to be 1.49 $\mathrm{cm^2{\cdot}V^{-1}{\cdot}s^{-1}}$, 216 $\mathrm{mV{\cdot}dec^{-1}}$, and 0.81 V, respectively. Since the a-ITGZO TFT operates in enhancement mode, it turns completely off when a V_{GS} below 0 V is applied. Figure 1(e) represents the anode current (I_{Anode}) versus anode voltage (V_{Anode}) curves of the gated silicon diode in which the latch-up phenomena occur owing to the energy band modulation when gate1 voltage (V_{G1}) is at 1.2 V or higher. The energy band modulation mechanism does not impose a burden on the gate oxide, which allows for nearly unlimited endurance. The potential barrier height determines the latch-up voltage ($V_{\mathrm{Latch\text{-}up}}$), which is defined as the V_{Anode} value when the I_{Anode} increases abruptly. Thus, an increase in V_{G1} results in an increase in $V_{\mathrm{Latch\text{-}up}}$, as shown in the eight distinct I_{Anode} versus V_{Anode} curves, including the initial state at $V_{\mathrm{G1}} = 0.0$ V (Appendix B). Figure 1(f) demonstrates the 3-bit memory operation of a 1T1D0C DRAM cell. For the write operation, the write word line voltage (V_{WWL}) higher than V_{TH} is set

* Corresponding author (email: chochem@korea.ac.kr, sangsig@korea.ac.kr)

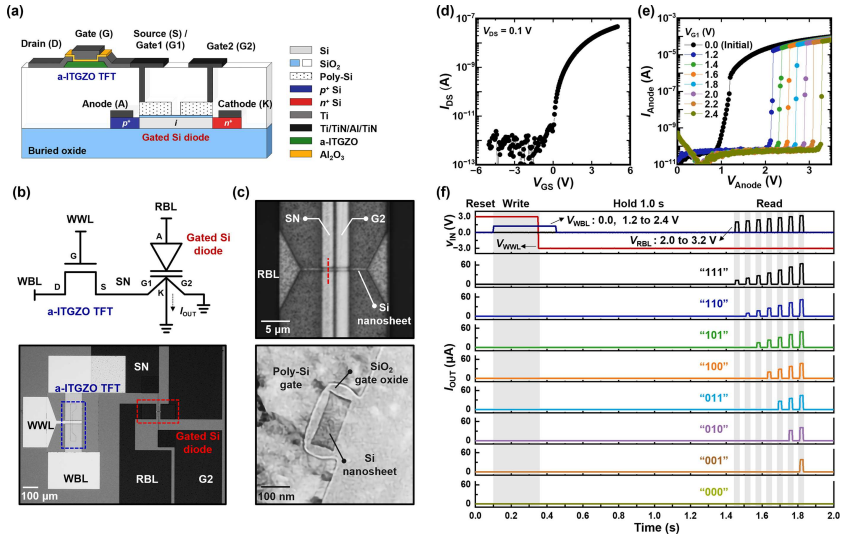

Figure 1 (Color online) (a) Schematic illustration of 1T1D0C DRAM cell; (b) circuit diagram and optical image of 1T1D0C DRAM cell, respectively; (c) optical image and channel cross-section TEM image of the gated silicon diode; (d) transfer characteristics (I_{DS}-V_{GS}) of an a-ITGZO TFT; (e) electrical characteristics (I_{Anode}-V_{Anode}) of the gated silicon diode at various V_{G1} values; (f) the 3-bit memory operation of the 1T1D0C DRAM cell. Eight memory states are distinguished when the V_{RBL} pulse activates the gated silicon diode.

to 3.0 V for 250 ms. The write bit line voltage (V_{WBL}) is in a range from 0.0 to 2.4 V as a function of the memory states.

V_{WBL} is applied at intervals of 100 ms after supplying V_{WWL} to prevent charge loss from the SN to the WBL. From the perspective of the gated silicon diode, the storage node voltage (V_{SN}) corresponds to V_{G1}. Thus, V_{WBL} controls the amount of charge stored in the SN, resulting in a $V_{\mathrm{Latch\text{-}up}}$ shift. For the hold operation, the a-ITGZO TFT is turned off by applying a negative V_{WWL} (−3.0 V), while V_{WBL} is set to 0.0 V. Owing to the low I_{Leakage} of the a-ITGZO TFT, the V_{SN} remains stable during the hold operation [4]. The gate leakage from the diode is under 100 fA, which is low enough to maintain the stability of V_{SN}. An incremental step pulse from 2.0 to 3.2 V in steps of 0.2 V is applied to the RBL with a pulse width of 25 ms for the read operation. Eight memory states are clearly distinguished when the read bit line voltage (V_{RBL}) pulse activates the gated silicon diode because $V_{\mathrm{Latch\text{-}up}}$ is adjusted by the amount of charge stored in the SN. For example, in a memory state "100", the I_{OUT} is sensed at a V_{RBL} of 2.6 V because the $V_{\mathrm{Latch\text{-}up}}$ is in the range of 2.4–2.6 V. For the 1T1D0C DRAM cell, the sensing margin between two adjacent memory states exceeds 10^5. The 1T1D0C DRAM cell distinguishes memory states based on the switching behavior of the gated silicon diode. Thus, the read operation method of the 1T1D0C DRAM cell can be an effective way to reduce read errors caused by noises resulting from low current levels. However, for conventional 2T0C DRAM cells, the sensing margin is defined as the I_{OUT} ratio between two adjacent memory states, and the sensing margin ranges from 1.4 to 2.1 [2]. This relatively low margin makes the read operation vulnerable to noise-induced errors. Moreover, the 1T1D0C DRAM cell offers significant advantages in high-density integration and is expected to achieve scaling down to $2\mathrm{F}^2$/bit through a monolithic 3D structure [5]. Furthermore, the 1T1D0C DRAM cell can have storage capacity more than 3-bit by subdividing V_{WBL} into more than eight levels when the gated silicon diode has more than eight distinct $V_{\mathrm{Latch\text{-}up}}$. In terms of the increase in storage capacity without altering the cell structure, 1T1D0C DRAM shows the potential for next-generation multibit memory applications.

Conclusion. This study designed a 1T1D0C DRAM cell comprising an a-ITGZO TFT and a double-gated silicon diode to achieve a 3-bit memory operation. The DRAM cell exhibited a linear relationship between the amount of charge stored in the SN and the magnitude of I_{OUT} owing to the latch-up phenomenon of the diode. Consequently, the 1T1D0C DRAM cell demonstrated a reliable 3-bit memory operation, with eight distinct memory states. This study demonstrates the 1T1D0C DRAM cell as a promising candidate for next-generation multibit memory applications.

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Supporting information Appendixes A and B. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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