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• Supplementary File •

3-bit memory operation of capacitor-less one-transistor one-diode DRAM cell

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Appendix A Fabrication process of 1T1D0C DRAM cell

The key fabrication process of the 1T1D0C DRAM cell involves two primary parts: the first for fabricating the gated silicon diode and the second for fabricating the a-ITGZO TFT. The starting wafer was a p-type (100)-oriented silicon-on-insulator wafer with a 100 nm-thick silicon active layer (doping concentration of approximately 10^{16} cm^{-3}). An active layer with a width of 200 nm was patterned by photolithography and dry etching. A 25 nm-thick SiO_2 gate dielectric layer was grown by the thermal oxidation of the active layer. The 400 nm-thick polysilicon layer was deposited using low-pressure chemical vapor deposition (LPCVD). The polysilicon layer was patterned with a length of 2.5 μm and a gap of 1.0 μm via photolithography and dry etching processes to form double gate structures. The cathode and the G1 regions were heavily doped with P^+ ions at 3×10^{15} cm^{-2} at 50 keV. Subsequently, the anode and G2 regions were heavily doped with B^+ ions at 3×10^{15} cm^{-2} at 30 keV, followed by rapid thermal annealing at 1050 °C for 30 s to activate the implanted dopant. The resulting gated silicon diode had a channel width of approximately 180 nm and a thickness of 70 nm. A 700 nm-thick SiO_2 interlayer dielectric layer was deposited via LPCVD using tetraethyl orthosilicate and patterned to form contacts and vias for the anode, cathode, and gate. Finally, the first part of fabricating the gated silicon diode was completed by depositing a Ti/TiN/Al/TiN metal stack as the anode, cathode, and gate electrodes, followed by an alloying process at 400 °C for 30 min. To fabricate the a-ITGZO TFT, a 50 nm-thick a-ITGZO channel layer was deposited from an ITGZO target via radiofrequency sputtering in a gas mixture of Ar and O_2. The width and length of the channel layer were 10 and 20 μm, respectively. The source and drain electrodes made of Ti were deposited by thermal evaporation at 25 °C. The source of the a-ITGZO TFT was connected to G2 of the gated silicon diode. A 32 nm-thick Al_2O_3 gate dielectric layer was then deposited by atomic layer deposition at 130 °C. Finally, the gate electrode made of Ti was deposited by thermal evaporation, followed by an activation process at 200 °C for 20 min.

All electrical measurements and characterizations were performed using a semiconductor parameter analyzer (HP4155C, Agilent), an LCR meter (HP4285A, Agilent), and a source meter (2636B, Keithley) at room temperature in a dark box. A cross-sectional image of the gated silicon diode was obtained using transmission electron microscopy (TEM, JEOL JEM-2100F, FEG) to validate the structural characteristics.

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Appendix B Latch-up phenomenon of gated silicon diode

The unique characteristic of the gated silicon diode, the latch-up phenomenon, operates through the modulation of the energy band in the p-n-p-n structure [1]. As indicated in Figure B1(a), the diode has a p^+–n^*–p^*–n^+ structure, even without applying an external voltage, by doping G1 with P^+ ions and G2 with B^+ ions. Here, the $n^*(p^*)$ region represents an electrostatically $n(p)$-doped region, and the potential barrier height is determined by the G1 voltage (V_{G1}). I_{Anode} versus V_{Anode} measurements were repeated 32 times for the gated silicon devices to verify the $V_{Latch\text{-}up}$ variance in seven states, except for the initial state, as shown in Figure B1(b). Figure B1(c) shows the cumulative distribution function of the $V_{Latch\text{-}up}$ extracted from Figure B1(b), indicating that the seven states are separated without overlapping regions. Herein, each of the seven states corresponds to "110" to "000," and the initial state is "111." Figure B1(d) shows that the diode has an extremely low cycle-to-cycle variance and exhibits a linear relationship between V_{G1} and $V_{Latch\text{-}up}$; these are essential factors for multibit memory device data accuracy and reliability [2, 3]. Moreover, the gated silicon diode is not only robust against bias/thermal stress but also exhibits negligible process variance since they are fabricated through a wafer-scale CMOS process [4, 5].

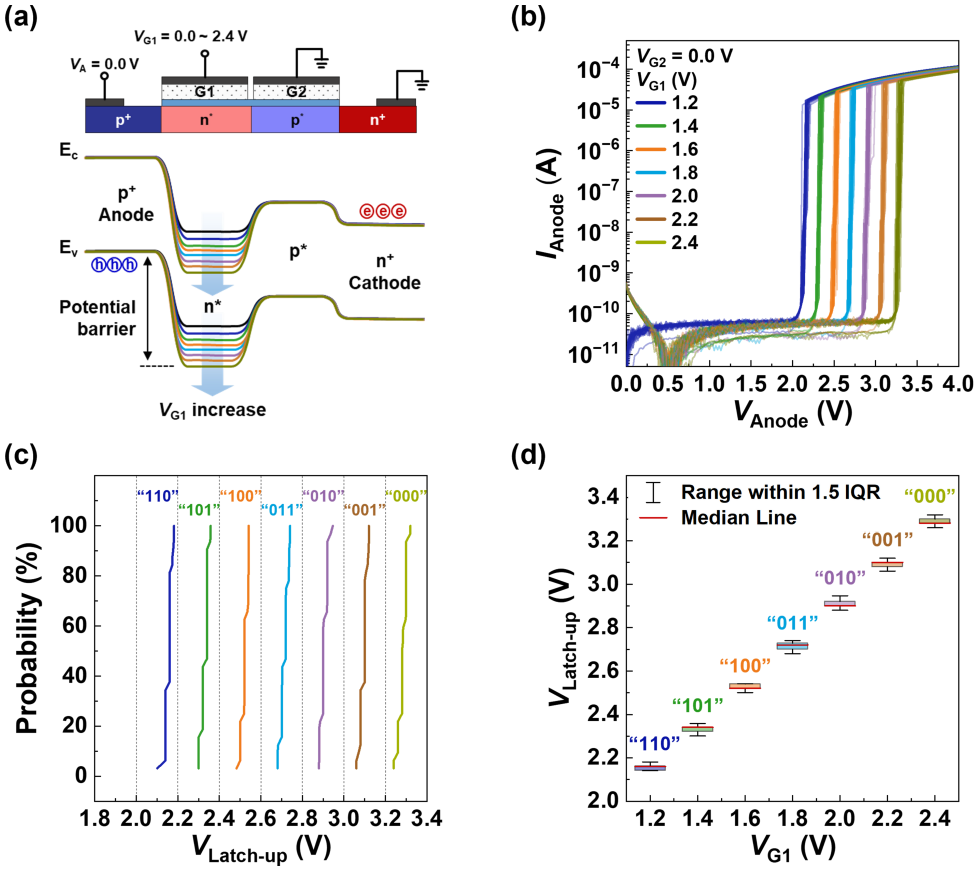

Figure B1 (a) Energy band diagram of a gated silicon diode. (b) The overlaid single plot of the 32 I_{Anode}–V_{Anode} curves, as V_{G1} varies from 1.2 to 2.4 V. (c) Cumulative distribution function of $V_{Latch\text{-}up}$ indicating that the seven states are separated without overlapping region. Each of the seven states corresponds to "110" to "000". (d) The linear relationship between V_{G1} and $V_{Latch\text{-}up}$.

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