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A reference-free and derivative-insensitive all-digital calibration technique for timing-skew in TI-ADCs

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Due to the input-dependent property, timing mismatch error is the most difficult to calibrate and significantly degrades the performance of time-interleaved analog-to-digital converters (TI-ADCs). Many state-of-the-art studies employ various calibration algorithms to mitigate this mismatch [1–4]. However, the speed, accuracy, effective bandwidth, and hardware overhead of these calibrations are restricted by multiple aspects of traditional techniques, including the timing reference channels, search methods, differential filters, and singularity. This study proposes a new calibration technique for the 2^i channels TI-ADCs to overcome these limitations and improve their performances.

Calibration process. As illustrated in Figure 1(a), the presented timing-skew calibration technique for a four-channel TI-ADC consists of the following two components. One is a novel two-step estimation, aiming to reduce singularity and quickly obtain estimation values without relying on a timing reference; the other is the optimized compensation, which enhances its accuracy and range by minimizing the root mean square (RMS) value of detection results.

During the first step of estimation, only the sampling instant of even channels is adjusted through an iterative process. For example, the mismatch error of channel 2 caused by its skew t_2 is calculated by the autocorrelation difference

$$\text{error} = E\left|y_{1,k} - \hat{y}_{2,k}\right| - E\left|\hat{y}_{2,k} - y_{3,k}\right| \propto t_2 \cdot R'(\tau), \quad (1)$$

where $y_{i,k}$ is the k-th sample of channel i. Depending on the error polarity, the detection based on an improved binary search successively approaches the timing skews of even channels until their sampling instants equally divide the sampling intervals (T_{13} and T_{31}) between odd channels. Hence, the adjacent sampling intervals can be updated as

$$T_{12} = T_{23} = T_s + \frac{\Delta T_1 + \Delta T_2}{2}, \quad (2)$$

where ΔT_i is the mismatch relative to sampling interval T_s.

Based on the results of the previous adjustments, the timing skews of the odd channels are estimated in the second step using the same iterative process, resulting in all adjacent sampling intervals being equal to T_s.

In the above process, another different set of detection results could be generated under the reversing detection order of odd and even channels, and theoretically be used to correct the relative sampling mismatch. However, the increased RMS values of detection results that are dependent on the artificial detection order seriously degrade the accuracy and range of mismatch compensation. Therefore, the optimal timing-skews ($\boldsymbol{t}_{\text{opt}}$) with the minimum RMS value are determined by removing the common-mode quantity ($\boldsymbol{t}_{\text{com}}$) related to the detection sequence from the detected results ($\boldsymbol{t}_{\text{detect}}$), then instituted into the first-order approximation to achieve high-precision compensation of samples $y_{i,k}$ as

$$\hat{y}_{i,k} = y_{i,k} - t_i \times \frac{\mathrm{d}y_{i,k}}{\mathrm{d}t}, \quad (3)$$

where the derivative is obtained by a 5-tap differential FIR filter with three adders and two shifters. Compared to the filters in [2,4], this filter eliminates the need for multipliers, thereby significantly reducing hardware cost and latency.

Reducing singularity. In those autocorrelation-based calibration techniques in [1–4], the singularity is closely tied to the characteristics of the autocorrelation function and the detection strategy. If the autocorrelation of a sinusoidal input is a cosine wave, the derivative of the autocorrelation function, $R'(\tau)$, proportional to the errors in (1), can be expressed as

$$R'(\tau) = -f_{\text{in}} \cdot \pi \cdot \sin(2\pi f_{\text{in}}\tau), \quad (4)$$

where the factor τ, dependent on the detection strategy, can lead to non-convergence in calibration by making $R'(\tau)$ equal to zero at singularities. As verified by the dotted lines in Figure 1(e), the calibrations in [2] determine the coefficient τ to be $2T_s$ and T_s during the detection process, resulting in singularities at the input frequency f_{in} of $0.25f_s$ and $0.5f_s$.

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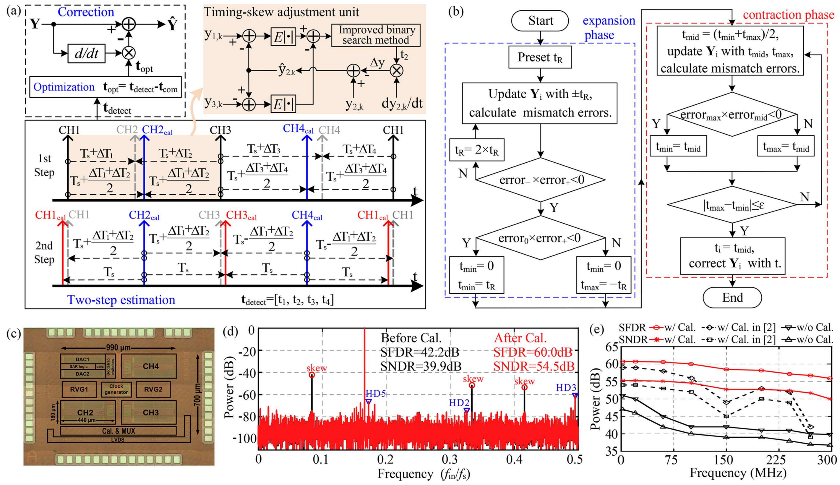

Figure 1 (Color online) (a) Overall structure of the proposed four-channel timing-skew calibration; (b) improved binary search with expandable detection range; (c) TI-ADC die micrograph; (d) measured TI-ADC output spectrum before and after calibration; (e) measured SFDR and SNDR versus input frequency with/without different calibrations.

To reduce singularities, the proposed calibration employs a new strategy to uniformly redistribute the sampling intervals and reduce the range of factor τ in (4). During the two-step estimation, the τ value can be rewritten as $T_s \pm (\Delta T_1 + \Delta T_2)/2$ in the first step, and equal to T_s in the second step. Compared to T_s, the sampling mismatches ΔT_i are too small to determine the singularity calculation. Hence, the proposed calibration is only affected by $R'(T_s)$, resulting in a singularity at $0.5f_s$.

Compensation for derivatives. According to the error term at the right side of (3), although the derivative is attenuated at high frequencies due to the filter's limited bandwidth [4], calibration will still converge if the detected value t_i adequately compensates for this attenuation. Therefore, an improved binary search with a variable range, instead of the least mean square (LMS) search in [2], is introduced to ensure the calibration is insensitive to derivative attenuation.

As shown in Figure 1(b), the improved binary search driven by mismatch error polarity employs a two-phase iteration to quickly determine an appropriate timing skew t_i. The expansion phase flexibly widens the search range to compensate for the derivative. Following this, the contraction phase halves the updated range and the search step size at every iteration, allowing for quick and high-accuracy detection.

Verification results. To verify the effectiveness of the proposed calibration technique, a calibration model incorporating two timing-skew adjustment units was implemented on the VC7203 board equipped with a Virtex-7 XC7VX485T-3 FFG1761E FPGA. The model operates on the FPGA at a clock frequency of 200 MHz. The hardware consumption for this implementation is 3451 LUTs, 30 DSPs, and 6 Block RAMs, corresponding to resource occupancy rates of 1.14%, 1.07%, and 0.58%, respectively. Disregarding the differences in FPGA types or algorithm implementations, the above calibration model reduces resource consumption by 2936 LUTs, 400 LUTRAMs, and 8040 FFs compared to the model with one DCSD module reported in [4]. The silicon-proven 600 MS/s 4-channel 10-bit TI-SAR ADC depicted in Figure 1(c) provides the original output data for calibration. Following the calibration of offset and gain mismatches using the equalization method in [2], 4K samples were stored in the Block RAMs for subsequent calibration processing.

Figure 1(d) shows the measured spectrum with a 100 MHz input signal before and after calibration. The calibration significantly attenuates all interleaving spurs to the noise floor, resulting in improvements of 17.8 dB in SFDR and 14.6 dB in SNDR. Figure 1(e) displays the measured spurious free dynamic ratio (SFDR) and signal-to-noise and distortion ratio (SNDR) at a 600 MS/s sampling rate across various input frequencies. Compared to the results in [2], the improvement in dynamic performance, particularly near 150 and 300 MHz, demonstrates that the proposed technique can effectively achieve high-precision calibration and reduce singularities, as well as expand the effective bandwidth to $0.49f_s$.

Conclusion. This study proposes a reference-free and derivative-insensitive digital timing-skew calibration technique for the 2^i channels TI-ADCs. The technique employs two-step estimation and optimized compensation processes, which significantly enhance calibration precision and reduce singularities by half. An improved binary search with an expandable range is utilized in the estimation process to compensate for the attenuation of derivatives, thus enhancing both convergence speed and accuracy. Verification results from a TI-ADC prototype and an FPGA calibration model demonstrate the proposed technique can achieve excellent calibration performance with low hardware cost, maintaining an effective bandwidth up to $0.49f_s$.

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