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A D-band CMOS eight-channel I/Q transmitter with enhanced LO feed-through suppression

Ning JIANG[1,2], Pingyang HE[3], Huiqi LIU[3], Guohua ZHAO[3], Ming ZHAO[4,5], Dalong ZHU[4] & Dixian ZHAO[1,2*]

[1]*National Mobile Communications Research Laboratory, Southeast University, Nanjing 210096, China*
[2]*Purple Mountain Laboratories, Nanjing 211111, China*
[3]*Chengdu Xphased Technology Company Ltd., Chengdu 610041, China*
[4]*Beijing Research Institute of Telemetry, Beijing 100094, China*
[5]*School of Electronics and Information, Northwestern Polytechnical University, Xi'an 710072, China*

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The D-band (110–170 GHz) falls within the sub-terahertz (sub-THz) range and has gained considerable attention in recent years. With its abundant spectrum resource, ultra-high-speed data transmissions can be realized, making it ideal for 6G backhaul and point-to-point communication [1]. A broadband high-performance transmitter (TX) is required to realize the full potential of this band. The advanced standard CMOS technologies are credible candidates due to their advantages of low cost and high integration [2].

The realization of a D-band TX faces three challenging issues due to severe parasitic effects. First, the local oscillator feed-through (LOFT) is closely related to the parasitic capacitance from the mixing transistors and layout overlapping. Moreover, the LOFT from the mixer is inevitably amplified by the power amplifier (PA), which will corrupt the transmitted signal. Second, I/Q modulation is a popular solution to realize image suppression [3,4]. However, the I/Q balance is more sensitive to the parasitic mismatch at D-band. The third issue is the increasing design complexity. For example, the single-stage amplifier gain is less than 5 dB at 120 GHz due to the limited maximum available power gain of the transistor. To compensate for the high insertion loss of the mixer, the PA has to cascade multiple stages.

In this study, a CMOS D-band eight-channel direct-conversion I/Q TX is presented. The LOFT suppression technique is proposed by modifying the layout routings in I/Q paths. Through the phase-inverted layout floor-plan, the TX achieves an improved LOFT with negligible effect on the desired signal. The measured LOFT is less than −34 dBc across 111–123 GHz with the peak gain of 30.94 dB.

Architecture. The system diagram of the proposed TX is depicted in Figure 1(a). The TX consists of eight identical channels, LO networks, serial peripheral interface (SPI), temperature sensors and power management modules. The LO input signal is quadrupled and subsequently divided to feed eight channels by the distribution network. In each channel, the I/Q generator with variable gain amplifiers (VGAs) provides quadrature LO signals of equal magnitude. The active balun in the baseband chain performs single-ended-to-differential (S2D) from a standard 50-Ω input interface. Following a pair of up-conversion mixers, a differential Wilkinson power combiner (WPC) and a 4-stage PA are adopted to enhance the driving capability. Considering the performance uniformity across temperature variations, a global biasing network and proportional-to-absolute-temperature (PTAT) compensation technique are included. The reference current (I_{TC}) is generated from the on-chip bandgap and delivered to all active building blocks.

Circuit implementation. Figure 1(b) illustrates the in-channel building blocks. Sufficient D-band LO power is accomplished by the quadrupler and driver amplifiers, and fed to the LO input port of the channel. Detailed circuit design techniques on LOFT suppression and I/Q calibration are addressed in the following.

A phase-inverted layout floor-plan is proposed to suppress LOFT based on the analysis of LO signals in I/Q paths. The quadrature LO signals are generated by the 3-dB 90° coupler with the simulated amplitude and phase imbalance below ±0.5 dB and ±1.8° across 105–130 GHz. An issue revealed by simulations is that the coupling between the identical matching networks in I/Q paths (i.e., T_1&T_2, T_3&T_4) introduces an extra phase imbalance. This I/Q imbalance will further affect the combination of the outputs of I/Q mixers (i.e., two sidebands and LOFT) by the WPC. The detailed operation principle of introducing additional phase error and synthesizing I/Q LOFT is presented in Appendix A. It is shown that the layout floor-plan of inverting the interconnections between mixers and WPC in the Q-path is superior to the same-polarity combining

* Corresponding author (email: dixian.zhao@seu.edu.cn)

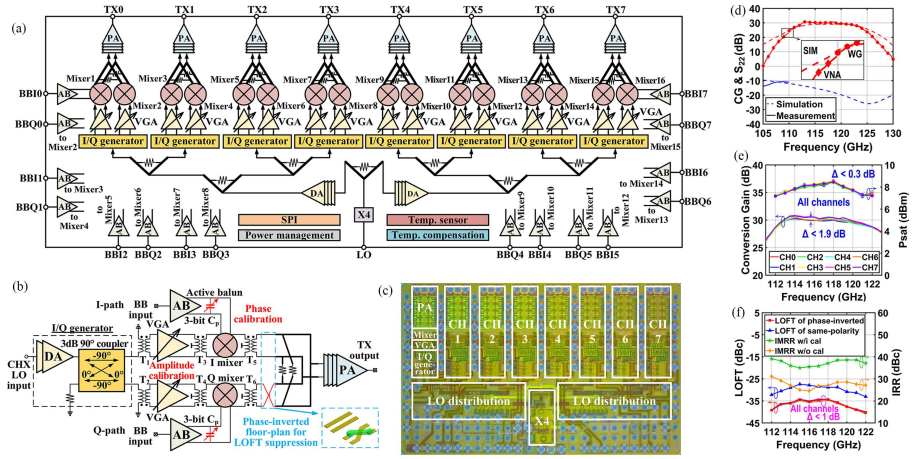

Figure 1 (Color online) (a) Architecture of the proposed TX; (b) channel diagram; (c) die photograph; (d) measured conversion gain and S_{22} of single channel versus simulation; (e) measured conversion gain and $P_{\rm sat}$ across eight channels; (f) measured LOFT and IRR.

scheme. Compared with the calibration method in [5, 6], this method is easy to implement without adding additional devices. According to the simulation of overall TX, this proposed suppression technique enables an 8-dB improvement of LOFT across the whole frequency band. The desired signals are negligibly affected, thanks to the careful implementation of differential cross-lines to mitigate the amplitude imbalance. To verify this LOFT suppression technique, an individual single-channel design with all identical modules but the same-polarity combining scheme is also taped out for comparison.

Two I/Q single-stage VGAs are adopted to ensure the equal amplitude of I/Q LO signals, while increasing driving capability. The gain tuning is achieved by controlling the 5-bit current digital-to-analog converter (IDAC). Combined with 3-bit switched capacitors (C_p) as shown in Figure 1(b), the imbalance of I/Q paths can be calibrated to improve the image rejection ratio (IRR). Because a small capacitance (e.g., 5 fF) can cause considerable phase variation at D-band, C_p is added at the baseband port of the mixer instead of LO port considering the tuning accuracy. The 3-bit C_p of 150/300/600 fF are designed to achieve ±5° fine-turning with 0.22 dB insertion loss and negligible effect on bandwidth.

Measurement results. The proposed D-band I/Q TX is fabricated in 65-nm CMOS. Die photograph is shown in Figure 1(c), with an area of 2.6 mm × 4.2 mm. The total power consumption is 1399 mW, including 8 × 161 mW for the eight channels and 106 mW for the common LO circuits. All measurements are done on a high-frequency probe station. Tests below 110 GHz are performed by the vector network analyzer (VNA). Above 110 GHz, the spectrum analyzer and a D-band frequency extender are employed with the waveguide probe. Detailed test setup is shown in Appendix B.

The measured 3-dB bandwidth of more than 12 GHz (111–123 GHz) is shown in Figure 1(d), with a maximum conversion gain of 30.94 dB. The measured gains near 110 GHz using two testing methods are close. The output return loss S_{22} below 110 GHz is below −10 dB, which is consistent with the simulation. The measured conversion gain and $P_{\rm sat}$ across eight channels are depicted in Figure 1(e). The gain variations are lower than 1.9 dB and $P_{\rm sat}$ is more than 7 dBm over broad bandwidth, which shows good channel consistency. The measured output 1-dB compression point at 118 GHz is 5.18 dBm. The measured LOFT and IRR are summarized in Figure 1(f). Compared to the aforementioned single-channel chip with a same-polarity combining scheme, the LOFT of this work is reduced to less than −34 dBc from 111 to 123 GHz. It proves that the proposed LOFT suppression technique is effective without specific calibration in measurement. The calibrated IRR is optimized from 29 to 38 dBc at 119 GHz and over 35 dBc among 3-dB bandwidth by adjusting C_p and VGAs in I/Q paths. The performance comparison is also summarized in Appendix C.

Conclusion. This study presents a D-band eight-channel I/Q TX in 65-nm CMOS technology. The enhanced LOFT suppression technique is proposed and the measured LOFT is less than −34 dBc across 111–123 GHz. Detailed circuit implementation and compact layout floor-plan are performed to optimize the overall performance. The measured peak conversion gain is 30.94 dB with good channel consistency.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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