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• **Supplementary File** •

A D-band CMOS Eight-Channel I/Q Transmitter with Enhanced LO Feed-Through Suppression

Ning JIANG[1,2], Pingyang HE[3], Huiqi LIU[3], Guohua ZHAO[3], Ming ZHAO[4,5], Dalong ZHU[4] & Dixian ZHAO[1,2*]

[1]*National Mobile Communications Research Laboratory, Southeast University, Nanjing 210096, China;*
[2]*Purple Mountain Laboratories, Nanjing 211111, China;*
[3]*Chengdu Xphased Technology Company Ltd., Chengdu 610041, China;*
[4]*Beijing Research Institute of Telemetry, Beijing 100094, China;*
[5]*Northwestern Polytechnical University, Xi'an 710072, China*

Appendix A LOFT suppression technique analysis

In each channel of the proposed transmitter (TX), the outputs of I/Q up-mixers is combined through the differential Wilkinson power combiner (WPC). The desired signals are superimposed while the image signals are cancelled out. The LO leakages are also combined, which will be analyzed in the following.

Appendix A.1 Phase Imbalance of LO I/Q paths

The I/Q imbalance caused by the coupling between the identical passive matching networks in I/Q paths is discussed. The quadrature LO signals are generated by the 3-dB 90° coupler and then pass through I/Q VGAs with two sets of inter-stage matching transformers. Two-transformer network with ideal orthogonal input excitation signals (i.e., $i_2 = ji_1$) is depicted in Figure A1(a). The output voltage V_3 is affected by both i_1 and i_2. The phase difference between V_3 and V_4 matters, as it may deviate from 90 degrees. Considering the characteristics of transformers and the coupling of adjacent coils, V_3 and V_4 can be represented as

$$V_3 = M_{13}\frac{di_1}{dt} + M_{23}\frac{di_2}{dt} + L_3\frac{di_3}{dt} \tag{A1}$$

$$V_4 = M_{24}\frac{di_2}{dt} + M_{14}\frac{di_1}{dt} + L_4\frac{di_4}{dt}. \tag{A2}$$

Assume that transformers XF_1 and XF_2 are completely identical, hence $L_1 = L_2,\ L_3 = L_4,\ k_{13} = k_{24},\ k_{23} = k_{14}$. By substituting $M_{ij} = \frac{k_{ij}}{\sqrt{L_iL_j}}$ and $n_{ij} = \frac{\sqrt{L_i}}{\sqrt{L_j}} = \frac{i_j}{i_i}$, (A1) and (A2) can be simplified to

$$V_3 = \frac{k_{13} + L_1L_3}{\sqrt{L_1L_3}}\frac{di_1}{dt} + j\frac{k_{23}}{\sqrt{L_1L_3}}\frac{di_1}{dt} = A\frac{di_1}{dt} + jB\frac{di_1}{dt} \tag{A3}$$

$$V_4 = j\frac{k_{13} + L_1L_3}{\sqrt{L_1L_3}}\frac{di_1}{dt} + \frac{k_{23}}{\sqrt{L_1L_3}}\frac{di_1}{dt} = jA\frac{di_1}{dt} + B\frac{di_1}{dt}. \tag{A4}$$

When $k_{23} = k_{14} = 0$,

$$V_3 = jV_4. \tag{A5}$$

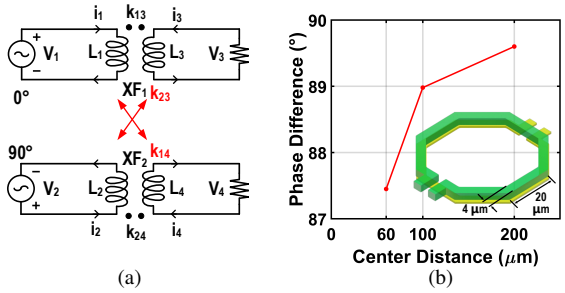
When $k_{23} = k_{14} \neq 0$ and the phase of V_i is represented as α_i, thus

$$\begin{aligned} \cos\alpha_3 &= \sin\alpha_4 = \frac{A}{\sqrt{A^2+B^2}} \\ \sin\alpha_3 &= \cos\alpha_4 = \frac{B}{\sqrt{A^2+B^2}}. \end{aligned} \tag{A6}$$

Considering the practical coupling and the homonymous ends, all k_{ij} are positive and $k_{13} > k_{23}$, which means $A > B$. With (A6) and the product-to-sum formula of trigonometric function, we have

$$\begin{aligned} \cos(\alpha_4 - \alpha_3) &= \frac{2AB}{A^2+B^2} > 0 \\ 0 < \sin(\alpha_4 - \alpha_3) &= \frac{A^2-B^2}{A^2+B^2} < 1. \end{aligned} \tag{A7}$$

* Corresponding author (email: dixian.zhao@seu.edu.cn)



(a) (b)

Figure A1 (a) Diagram of two-transformer network with orthogonal input signals. (b) Simulated phase difference of two-transformer network with different center distance at 120 GHz.

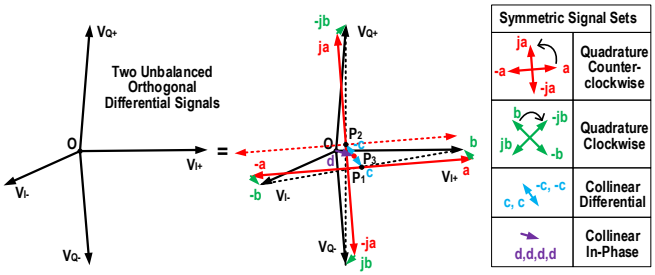


Figure A2 Unbalanced I/Q differential signals decomposed by four symmetric signal sets.

As revealed by (A7), the phase difference of output signals satisfies $0°<\alpha_4-\alpha_3<90°$ under the condition of $\alpha_2-\alpha_1=90°$.

The simulated phase difference of a two-transformer example with the ideal orthogonal 120 GHz input signals is shown in Figure A1(b). The length of side of the instanced square octagonal transformer is 20 μm, with the line width of 4 μm. It can be seen that the quadrature of the output signals deteriorates as two transformers become closer. In the proposed TX, the coupler and the subsequent transformers are simulated together with center distance of 100 μm. According to the EM simulation, the worst phase difference of I/Q LO signals from 110 to 130 GHz is deteriorated to 85.8° after passing through two sets of transformers.

Appendix A.2 Phase-inverted Floor-plan for LOFT Optimization

In practice, the LOFT signals in I/Q paths inevitably have I/Q imbalance and differential imbalance due to parasitic effect. These two unbalanced differential signals can be expressed as four related signals V_{I+}, V_{Q+}, V_{I-}, V_{Q-}. According to [1–3], arbitrary unbalanced signals can be represented as the sum of symmetric vectors to simplify the circuit analysis. As shown in Figure A2, I/Q LOFT can be decomposed in the complex plane, we have

$$\begin{aligned} V_{I+} &= \vec{a}+\vec{b}+\vec{c}+\vec{d} \\ V_{Q+} &= j\vec{a}-j\vec{b}-\vec{c}+\vec{d} \\ V_{I-} &= -\vec{a}-\vec{b}+\vec{c}+\vec{d} \\ V_{Q-} &= -j\vec{a}+j\vec{b}-\vec{c}+\vec{d} \end{aligned} \tag{A8}$$

where includes four symmetric signal sets, quadrature counterclockwise $\vec{a}$, quadrature clockwise $\vec{b}$, collinear differential $\vec{c}$, and collinear in-phase $\vec{d}$.

Due to the symmetry in I/Q paths, the conventional combining scheme is to synthesize the signals of the same polarity, as shown in Figure A3(a). The output voltages are given by

$$V_{I+}+V_{Q+} = \vec{a}(1+j)+\vec{b}(1-j)+2\vec{d} \tag{A9}$$

$$V_{I-}+V_{Q-} = -\vec{a}(1+j)-\vec{b}(1-j)+2\vec{d} \tag{A10}$$

where $\vec{c}$ is cancelled out through the isolation resistors in WPC. The common-mode (CM) component of the combined signal is clearly $2\vec{d}$. It can be seen that the LOFT will be optimized by reducing amplitude imbalance. The differential-mode (DM) can be calculated by equation (A9) and (A10). Therefore, we have

$$V_{DM\_same-polarity} = \vec{a}+\vec{b}+j(\vec{a}-\vec{b}). \tag{A11}$$

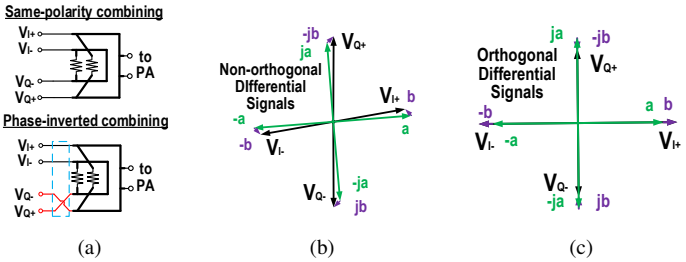


Figure A3 (a) Two combining schemes. (b) Non-orthogonal differential signals only decomposed of $\vec{a}$ and $\vec{b}$. (c) Orthogonal differential signals only with I/Q amplitude imbalance.

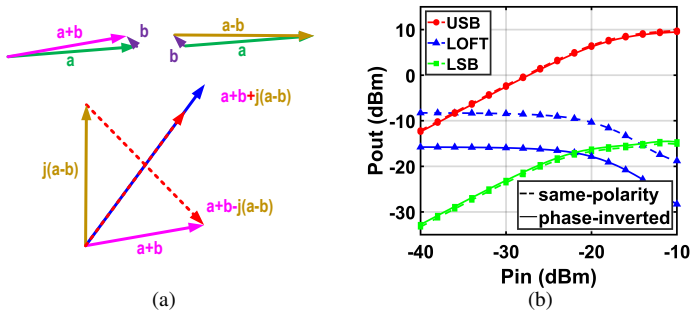


Figure A4 Comparison of two combining schemes. (a) Diagram of the length of DM components. (b) Simulated output signals and LOFT versus input power.

The phase-inverted combining scheme is accomplished by swapping the interconnections between the mixer and WPC, as depicted in Figure A3(a). Therefore, the combined signals and DM component can be calculated as

$$V_{I+} + V_{Q-} = \vec{a}(1-j) + \vec{b}(1+j) + 2\vec{d} \tag{A12}$$

$$V_{I-} + V_{Q+} = -\vec{a}(1-j) - \vec{b}(1+j) + 2\vec{d} \tag{A13}$$

$$V_{DM\_phase-inverted} = \vec{a} + \vec{b} - j(\vec{a} - \vec{b}). \tag{A14}$$

Comparing (A11)-(A14), the CM outputs of two combining schemes are the same and the DM outputs are only related to $\vec{a}+\vec{b}$ and $\vec{a}-\vec{b}$. Further analysis are focused on the relationship of $|V_{DM\_same-polarity}| - |V_{DM\_phase-inverted}|$ to figure out the effect of the proposed combining scheme.

As indicated by (A8), $\vec{a}$ is the desired differential I/Q signals while $\vec{b}$ is introduced by both the gain and phase imbalances. To simplify the analysis and expression, assume that the CM distortions are neglected (i.e., $\vec{c}\,\&\vec{d}=0$), equation (A8) can be simplified to

$$\begin{aligned} V_{I+} &= -V_{I-} = \vec{a} + \vec{b} \\ V_{Q+} &= -V_{Q-} = j(\vec{a} - \vec{b}). \end{aligned} \tag{A15}$$

According to the analysis in Appendix A.1, the phase difference of I/Q LO signals (i.e., the phase of V_{I+} and V_{Q+}) satisfies the condition of $0^\circ < \alpha = \alpha_4 - \alpha_3 < 90^\circ$ and an example is shown in Figure A3(b). Assume that $V_{Q+} = XV_{I+}e^{j\alpha}(X>0)$ and substitute it into (A11) and (A14), we have

$$V_{DM\_same-polarity} = V_{I+} + V_{Q+} = V_{I+} + XV_{I+}e^{j\alpha} \tag{A16}$$

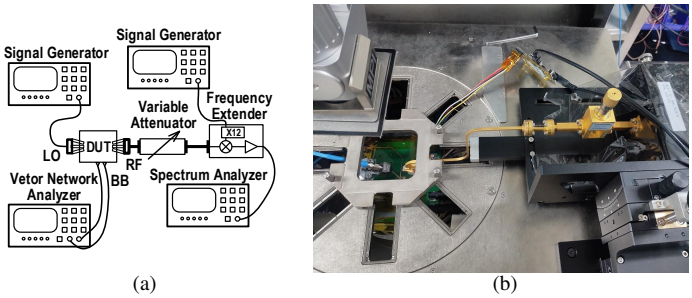
$$V_{DM\_phase-inverted} = V_{I+} - V_{Q+} = V_{I+} - XV_{I+}e^{j\alpha} \tag{A17}$$

$$|V_{DM\_same-polarity}| - |V_{DM\_phase-inverted}| = |V_{I+}||1 + Xe^{j\alpha}|(1 - \frac{|1 - Xe^{j\alpha}|}{|1 + Xe^{j\alpha}|}). \tag{A18}$$

Considering $0^\circ < \alpha < 90^\circ$, we have

$$1 - \frac{|1 - Xe^{j\alpha}|}{|1 + Xe^{j\alpha}|} = 1 - \frac{\sqrt{1 + X^2\cos^2\alpha - 2X\cos\alpha + \sin^2\alpha}}{\sqrt{1 + X^2\cos^2\alpha + 2X\cos\alpha + \sin^2\alpha}} > 0. \tag{A19}$$

Therefore, $|V_{DM\_same-polarity}| - |V_{DM\_phase-inverted}| > 0$. In other words, the proposed combining scheme can achieve LOFT suppression. If the differential signals are orthogonal as depicted in Figure A3(c), the combined LOFT will be not affected by using this phase-inverted combining scheme.



(a) (b)

Figure B1 (a) Measurement setup for output power and conversion gain above 110 GHz. (b) Photograph of the testing scene.

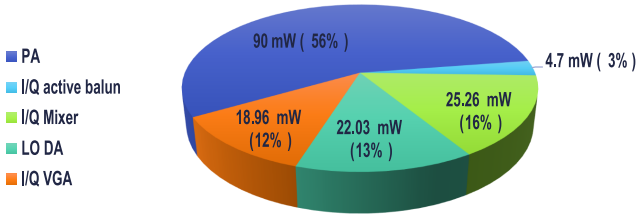


Figure C1 Power consumption breakdown of the modules in a single channel.

The diagram of DM-component synthesis based on Figure A3(b) is illustrated in Figure A4(a). It is clearly found that the length of $\vec{a}+\vec{b}-j(\vec{a}-\vec{b})$ is shorter than that of $\vec{a}+\vec{b}+j(\vec{a}-\vec{b})$. In practice, according to the performance simulation of overall TX, this proposed LOFT suppression technique enables an 8-dB improvement of LOFT, as shown in Figure A4(b). The layout implementation of the connections between I/Q mixers and PA is carefully designed to ensure the differential balance and I/Q balance. Thanks to this, the conversion gain and IRR of the proposed TX are negligibly affected.

Appendix B Measurement setup

All measurements of the proposed TX are done on a high-frequency probe station. Two test schemes are adopted considering the comprehensiveness and credibility. The vector network analyzer (VNA) is used for test below 110 GHz due to the limited maximum operating frequency. Although this frequency is at the edge of the designed operating band, this measurement can provide decent support for the other test scenario. The measurement setup above 110 GHz is illustrated in Figure B1(a) and the photograph of the testing scene on the probe station is shown in Figure B1(b). Two mutually orthogonal IF signals are generated through the Differential I/Q mode of the VNA, which are fed into the chip through the PCB board. In order to process the D-band transmitting signal with the waveguide-probe interface, a WR-06 (110-170 GHz) frequency extension module for the spectrum analyzer (SA) is used. The frequency extender can down-convert the D-band signals to enable the analysis of the signal spectrum by the SA. The waveguide power meters (e.g., PM5B) are not used because they cannot distinguish the main signal from the LO leakage and the image signal. The function of the variable waveguide attenuator is to protect the waveguide frequency extender by keeping the input signal within an appropriate range. Two signal generators provide LO signals for the chip and the frequency extender respectively. The detailed measurement results are calculated by multiple calibration parameters, including the conversion loss of the frequency extender, the attenuation of the variable attenuator and the insertion loss of the connector and waveguide probe. In particular, the attenuation of the variable attenuator is achieved by mechanically adjusting the scale, which inevitably has the accidental errors of 1-2 dB. To avoid ambiguity, the attenuation has been measured for several times and relatively large values have been taken. Note that this work focuses on the improvement of the LOFT, which is a relative value and almost unaffected in the case of high losses.

Appendix C Performance discussion and comparison

The performance of the proposed TX is summarized in Table C1. The channel area is obtained by dividing the total chip area by the number of channels for easy comparison with other works. The DC power consumption of a single channel is calculated as 174.25 mW, comprising 161 mW for each module and an additional 13.25 mW derived from dividing 106 mW equally across eight channels. The detailed breakdown of each module is illustrated in C1, including a PA, two I/Q active baluns, two I/Q mixers, an LO driver amplifier and two I/Q VGAs. The 3-dB 90° coupler is passive and the PA consumes 85 mW at static while increasing to 90 mW at the saturated state. The high and flat gain response gain relieves the requirement of baseband input power. The measured LOFT among eight channels is less than -34 dBc with only 1 dB variation, which shows good channel consistency. The proposed LOFT suppression technique also has the advantage of not requiring complex adjustments in measurement. In the optimal combinations of C_p and VGAs in I/Q paths, the calibrated

Table C1 Performance Comparison of CMOS TXs.

Reference	This work	[6]	[7]	[8]	[9]	[10]
Process	65nm CMOS	65nm CMOS	40nm CMOS	22nm FinFET	22nm FDSOI	45nm CMOS SOI
Architecture	8-CH I/Q modulation with quadrupler	full-duplex I/Q modulation TRX	I/Q modulation with tripler	RF-DAC with PLL and tripler	I/Q modulation with 9× multiplier	8-CH with 6× multiplier and LO leakage cancellation
Frequency (GHz)	117	112	119	140	135	140
Peak Gain (dB)	30.94	7[a]	10.8	7.3(sim)	18	21
LO Power (dBm)	0(@30GHz)	–(@28GHz)	–(@40GHz)	built-in PLL	0(@15GHz)	–(21.5–23GHz)
OP1dB (dBm)	5.18@118GHz	–	7.5	2.6(sim)	–	9.5@148GHz
Psat (dBm)	>7	0	10	7.5(sim)	2.8	11.2–12.2(PA)
LOFT (dBc)	<-34	<-20(mixer)	-33.7	-28	-23.3	-29/-38[d]
IRR (dBc)	>35	35[a]	43.1	22	–	28
Power (mW)	174.25[b]	199	220	173.5	196	231[b]
Channel Area (mm^2)	1.365[c]	0.93	1.19	4/0.75(core)	1.444	3.44[c]

IRR is optimized from 29 to 38 dBc at 119 GHz and over 35 dBc among 3-dB bandwidth.

In conclusion, compared with the prior-arts, the proposed TX achieves the highest conversion gain with eight-channel integration while achieving decent LOFT without calibration in measurement.

References

1 Frounchi M, Alizadeh A, Coen C T, et al. A low-loss broadband quadrature signal generation network for high image rejection at millimeter-wave frequencies. IEEE Trans Microw Theor Tech, 2018, 66: 5336-5346
2 Behbahani F, Kishigami Y, Leete J, et al. CMOS mixers and polyphase filters for large image rejection. IEEE J. Solid-State Circ, 2001, 36: 873-887
3 Gu P, Zhao D X, You X H. A wideband vector-modulated variable gain phase shifter for 5G NR FR2 in 40-nm CMOS. IEEE Trans Microw Theor Tech, 2024, 72: 5274-5284
4 Lee C J, Kang J, Park C S. A D-Band low-power gain-boosted up-conversion mixer with low LO power in 40-nm CMOS technology. IEEE Microw Wireless Compon Lett, 2017, 27: 1113-1115
5 Zhao D X, Reynaert P. A 40 nm CMOS E-Band transmitter with compact and symmetrical layout floor-plans. IEEE J. Solid-State Circ, 2015, 50: 2560-2571
6 Wang C, Abdo I, Liu C X, et al. A sub-THz full-duplex phased-array transceiver with self-interference cancellation and LO feedthrough suppression. IEEE J. Solid-State Circ, 2024, 59: 978-992
7 Kim S H, Jang T H, Kang D M, et al. Wideband 120-GHz CMOS I/Q transmitter with suppressed IMRR and LOFT for wireless short-range high-speed 6G IoT applications. IEEE Internet Things J., 2023, 10: 11739-11748
8 Callender S, Agrawal A, Whitcombe A, et al. A fully integrated 160-Gb/s D-Band transmitter achieving 1.1-pJ/b efficiency in 22-nm FinFET. IEEE J. Solid-State Circ, 2022, 57: 3582-3598
9 Farid A A, Ahmed A S H, Dhananjay A, et al. A fully packaged 135-GHz multiuser MIMO transmitter array tile for wireless communications. IEEE J. Solid-State Circ, 2022, 70: 3396-3405
10 Li S W, Zhang Z, Rebeiz G M. An eight-element 136-147 GHz wafer-scale phased-array transmitter with 32 dBm peak EIRP and >16 Gbps 16QAM and 64QAM operation. IEEE J. Solid-State Circ, 2022, 57: 1635-1648
11 Chien J S, Buckwalter J F. A 110-120-GHz, 12.2% efficiency, 16.2-dBm output power multiplying outphasing transmitter in 22-nm FDSOI. In: Proceedings of IEEE Asian Solid-State Circuits Conference (A-SSCC), Taipei, 2022, 1-3
12 Farid A A, Simsek A, Ahmed A S H, et al. A broadband direct conversion transmitter/receiver at D-band using CMOS 22nm FDSOI. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Boston, 2019, 135-138
13 Lee C J, Kim S H, Son H S, et al. A 120 GHz I/Q transmitter front-end in a 40 nm CMOS for wireless chip to chip communication. In: Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Philadelphia, 2018, 192-195
14 Kananizadeh R, Momeni O. High-power and high-efficiency millimeter-wave harmonic oscillator design, exploiting harmonic positive feedback in CMOS. IEEE Trans Microw Theor Tech, 2017, 65: 3922-3936
15 Li S W, Rebeiz G M. High efficiency D-Band multiway power combined amplifiers with 17.5-19-dBm Psat and 14.2-12.1% peak PAE in 45-nm CMOS RFSOI. IEEE J. Solid-State Circ, 2022, 57: 31332-1343

1) [a] Graphically estimated.
2) [b] After adjustment in measurement.
2) [c] The equivalent power consumption of single channel
2) [d] Total area divided by the number of channels.