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Special Topic: Novel Memory Materials and Devices: Ferroelectrics and Oxide Semiconductors

Scaled 3D-stacked 2T0C DRAM based on indium-tin-oxide transistors with long data retention and fast write speed of 10 ns

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DRAM is a critical component in many digital systems, providing temporary storage for data frequently accessed by the processor due to its high density and high reliability [1]. However, the development of traditional silicon-based 1T1C DRAM is currently facing significant bottlenecks. As DRAM dimensions continue to shrink and approach the 10 nm range, not only does the short-channel effect lead to an increasing leakage current in the off-state of the access transistors, but the reduction in capacitance also results in a decrease in stored charge. Both factors contribute to the degradation of data retention time, thereby limiting improvements in power consumption [2]. Amorphous oxide semiconductors (AOS), represented by IGZO, ITO, and IWO, etc., are considered the most promising candidates for next-generation DRAM due to their significant advantages, including high mobility, low off-state leakage current, and low thermal budget [3].

Recent research on AOS-based 2T0C DRAM has demonstrated excellent data retention time through the optimization of transistor performance, primarily by adopting a planar structure [4]. Although 2T0C DRAM significantly reduces power consumption associated with data write-back by separating read and write operations, it incurs a greater area overhead compared to the 1T1C structure. Therefore, 3D-stacked 2T0C DRAM provides an effective method for shrinking the cell area to enhance integration density. However, currently reported 3D-stacked DRAM exhibits inferior data write speed and retention time compared to planar structures due to the limitations in dimension scaling, contact resistance, and threshold voltage shifts during the fabrication process [5].

In this work, the scaled 3D-stacked 2T0C DRAM has been successfully fabricated using two layers of ITO transistors with identical electrical performance, serving as the write and read transistors, respectively. Notably, both layers of 60 nm ITO transistors exhibit a high current on/off ratio of 10^{11} and an outstanding on-state current, the 3D-stacked 2T0C DRAM demonstrates a high write speed of 10 ns and an impressive data retention time exceeding 1000 s. These findings underscore the significant potential of ITO transistors for high-density 3D-stacked DRAM applications.

Results and discussion. Figure 1(a) shows the zoom-in scanning electron microscope (SEM) image of the 3D-stacked 2T0C DRAM cell based on two layers of ITO transistors. The device fabrication process, optical image, and transmission electron microscopy (TEM) image are described in Appendix A. Figure 1(b) compares the transfer characteristics of the 1st layer and 2nd layer ITO transistors with a scaled channel length of 60 nm at $V_{\rm ds}$ = 0.5 V. Both layers of ITO transistors demonstrate remarkable electrical properties. They exhibit a high current on/off ratio of 10^{11} and a low subthreshold swing of 90 mV/dec. The corresponding output characteristics of the 1st layer and 2nd layer ITO transistors at $V_{\rm ds}$ = 0.5 V are shown in Figure 1(c). The maximum on-state current ($I_{\rm d}$) of the 1st layer and 2nd layer ITO transistors is 750 and 810 μA/μm, respectively. Further, the mobility, contact resistance, and reliability of ITO transistors are shown in Appendix B. These results suggest that ITO transistors are compatible with 3D stacking while exhibiting excellent electrical performance.

The circuit schematic view and the measurement setup for the write and read operation of 3D-stacked 2T0C DRAM are illustrated in Figure 1(d). For the write operation of 2T0C DRAM, the storage node capacitance ($C_{\rm s}$), which corresponds to the gate capacitance of the 2nd layer read transistor, is charged using positively biased write word line

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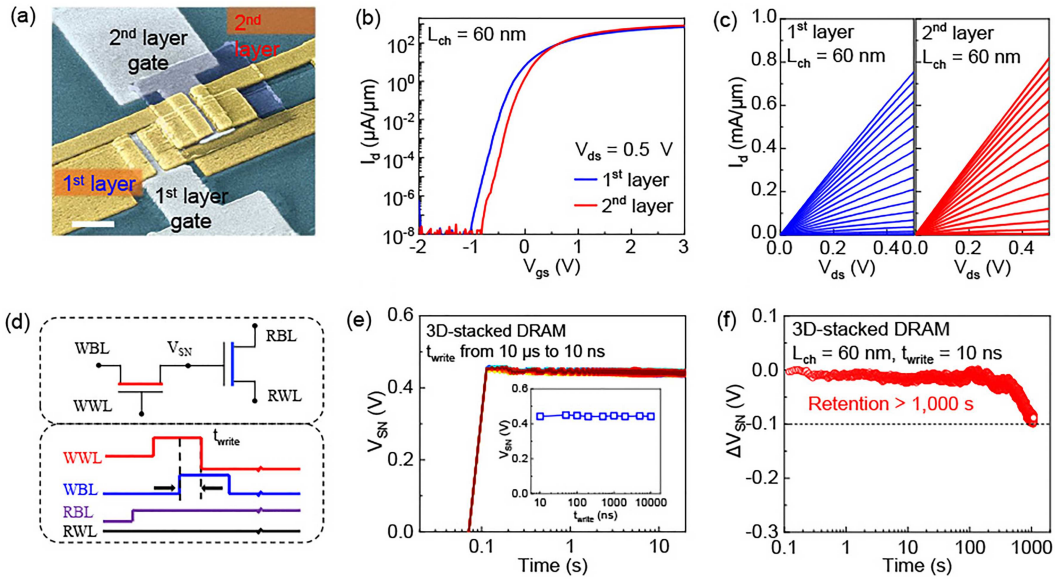

Figure 1 (Color online) (a) SEM image of the 3D-stacked 2T0C DRAM cell (scale bar, 200 nm); (b) transfer characteristics of the 1st layer and 2nd layer ITO transistors with $L_{\rm ch}$ = 60 nm at $V_{\rm ds}$ = 0.5 V; (c) output characteristics of the 1st layer and 2nd layer ITO transistors with $L_{\rm ch}$ = 60 nm at $V_{\rm ds}$ = 0.5 V and $V_{\rm gs}$ varies from −1 to 3 V in 0.2 V step; (d) circuit schematic view and measurement setup of write and read operation for 2T0C DRAM cell; (e) storage node retention characteristics of the 3D-stacked DRAM cell with different write times (the insert shows the storage node voltage versus write time varying from 10 μs to 10 ns); (f) the change in storage node voltage versus time for 3D-stacked DRAM cell with $L_{\rm ch}$ = 60 nm.

(WWL) and write bit line (WBL) voltages. The write time ($t_{\rm write}$) is defined by the overlap of WWL and WBL voltage pulses, which determines the duration for charging the storage node and writing data to the DRAM cell. The hold voltage ($V_{\rm hold}$) of the WWL (−3 V) is applied to fully turn off the write transistor after write operation, preventing charge leakage from the storage node capacitance and ensuring a long retention time, while the WBL voltage is set to 0 V. For the read operation of 2T0C DRAM, the voltages of read bit line (RBL) and read word line (RWL) are set to 0.5 and 0 V, respectively, to monitor the output current of the read transistor and estimate the data storage state. The storage node voltage ($V_{\rm SN}$) of the 2T0C DRAM is obtained from $I_{\rm d}$-$V_{\rm gs}$ fitting. The retention time is defined as the duration it takes for the storage node voltage to drop by 0.1 V from its initial value. It is worth noting that the non-destructive read operation and excellent data retention time of the 2T0C DRAM are beneficial for lowering power consumption by reducing the write-back and refresh frequency. Figure 1(e) shows the storage node voltage of the 3D-stacked DRAM cell at different write times. The inset shows the extracted storage node voltage after writing data "1" as a function of write time. The storage node voltage shows no variation as the write time changes from 10 μs to 10 ns, confirming that the write speed is faster than 10 ns, which is limited by the measurement equipment. This excellent performance can be attributed to the high on-state current of the write transistor, which enables rapid and efficient charging of the storage node during the write operation. Figure 1(f) shows the change in $V_{\rm SN}$ of the 3D-stacked 2T0C DRAM after the write operation as a function of measurement time. The short-channel DRAM demonstrates a remarkable retention time of over 1000 s, along with a high write speed of 10 ns. The performance benchmark of 2T0C DRAM with sub-100 nm channel length based on AOS transistors is displayed in Appendix C. The scaled 3D-stacked 2T0C DRAM presented in this work, with its fast write speed and long retention time, indicates the tremendous potential of AOS transistors in high-density memory applications.

Conclusion. We have successfully demonstrated high-performance 3D-stacked 2T0C DRAM based on sequentially fabricated layers of scaled ITO transistors. The fabricated layers of ITO transistors exhibit high carrier mobility and high on-state current. Consequently, the 60 nm 3D-stacked 2T0C DRAM achieves an outstanding data retention time exceeding 1000 s, along with a high write speed of 10 ns, indicating the significant potential of ITO transistors toward high-speed and high-density 3D-integrated DRAM applications.

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Supporting information Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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