SCIENCE CHINA
Information Sciences

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Gate conduction mechanisms and high V_{th} stability of Cu-Gated p-GaN HEMT

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Appendix A Growth epitaxy and device fabrication

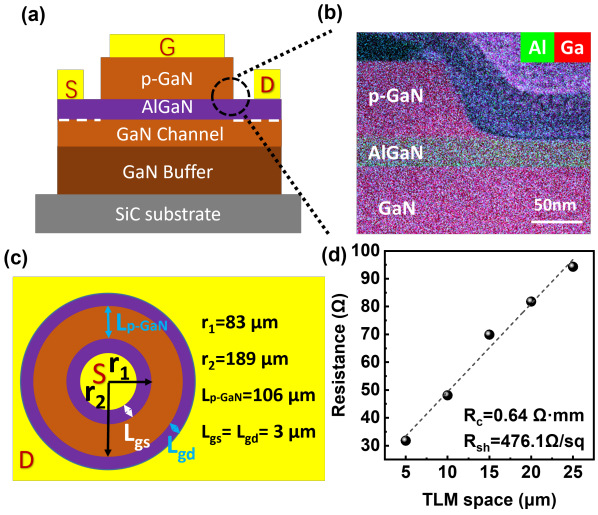

Figure A1 (a) Schematic diagram, (b) Energy Dispersive Spectrometer test in TEM photography, (c) top view and (d) TLM plot of p-GaN HEMT.

Epitaxial structure in this work based on a SiC substrate consists of a 1.3 μm high resistance GaN buffer layer, a 300 nm un-doped GaN channel layer, a 25 nm $Al_{0.2}Ga_{0.8}N$ barrier layer, and an 80 nm p-GaN cap layer grown by metal-organic chemical vapor deposition (MOCVD) with $3 \times 10^{19} cm^{-3}$ Mg doping used to achieve enhancement-mode and high gate breakdown voltage, shown in Figure A1(a). Fabrication of the device starts with a Cl-based dry etch of the active region of p-GaN with a low rate of 2 nm/min to guarantee accurate depth. The complete retention of the AlGaN layer in the EDS test of Figure A1 (b) shows the precision of the etching process. Subsequently, Ti (20 nm)/Al (160 nm)/Ni (55 nm)/Au (45 nm) metal stack is deposited and annealed in the N_2 atmosphere for 1 min at 860 °C to form ohmic contacts and Oxford Instrument's inductively coupled-plasma reactive-ion etching (ICP-RIE) system using BCl_3/Cl_2 gas mixture is carried out to isolate the device. The contact resistance (R_C) and sheet resistance (R_{SH}) of these devices are approximately 0.64 $\Omega \cdot mm$ dand 476.1 Ω/sq, according to a transmission line model measurement (TLM), as shown in Figure A1(d). Then, Ni/Au, Cu/Au, and W/Au (45/200 nm) are deposited by magnetron sputtering as a gate stack. A 250 nm Si_3N_4 passivation layer was prepared on the whole wafer by the PECVD method. Finally, source/drain contact windows are formed by a fluorine-based etching. To avoid the influence of additional leakage and amplify the influence of the gate stack on the device, this paper investigates ring-shaped p-GaN/AlGaN/GaN HEMTs with different gate metals. Structural parameters of the p-GaN HEMTs are labeled in Figure A1(c). All the devices under test (DUTs) are characterized by a Keithley 4200 semiconductor parameter analyzer.

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