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Performance limit prediction of atomically thin In_2O_3 transistors

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Moore's law requires the downscaling of metal oxide semiconductor field effect transistors (MOSFETs) for future integrated circuits (ICs) development. The performance of Si-based MOSFETs becomes insufficient to meet the standards outlined in the international technology roadmap for semiconductors (ITRS) due to short-channel effects as the channel length shrinks below 10 nm [1]. Ultrathin thin In_2O_3 films with atomically smooth surfaces have recently been fabricated using atomic layer deposition (ALD) [2]. Compared to Si, In_2O_3 demonstrates higher mobility (over 100 $cm^2{\cdot}V^{-1}{\cdot}s^{-1}$) [3], superior gate controllability, and reduced leakage current due to its wider bandgap (1.92–2.43 eV) [4]. Furthermore, unlike other 2D van der Waals (vdW) materials, In_2O_3 offers better chemical stability in air, compatibility with dielectric layer due to the existence of surface dangling bonds, and a low thermal growing budget (225°C) during growth [5]. However, to the best of our knowledge, the performance limit of the In_2O_3 transistors with gate lengths below 5 nm remains to be elucidated.

Device performance. The double gate (DG) two-probe In_2O_3 thin film transistor (TFT) model, as shown in Figure 1(a), is used in the quantum transport simulation. The scaling behavior of hydrogenated 0.7-nm-thick In_2O_3 TFTs is investigated for gate lengths (L_g) below 5 nm. The detailed IV-characteristics are shown in Appendix C. The on-state current ($I_{\rm on}$) of In_2O_3 TFT satisfies the ITRS standards for high-performance (HP) and low-power (LP) applications at gate lengths of 3 and 4 nm, respectively. Under the underlap (UL) optimized technique, the short-channel effect is effectively surpassed by reducing the tunneling current (Appendix D). In_2O_3 TFTs exhibit higher on-state current ($I_{\rm on}$) than InSe, silicene, and MoS_2 FETs for HP applications at a gate length of 5 nm and show comparable performance to Bi_2O_2Se FETs at 3 nm, as shown in Figure 1(b). However, their LP performance remains competitive, meeting the ITRS standards only at 5 nm (Figure 1(c)). The subthreshold swing (SS) of In_2O_3 TFTs is observed to range from 78 to 160 mV/dec, significantly outperforming competing 2D materials such as MoS_2 and InSe in electrostatic control as shown in Figure 1(d).

Strain engineering. Strain engineering is applied to further optimize the performance of ultrathin In_2O_3 TFTs (Appendix E). A 1% tensile strain reduces the bandgap, increasing the carrier concentration and boosting $I_{\rm on}$ by 97% for a 4-nm-L_g device. However, excessive strain induces lattice distortions, leading to performance degradation.

In_2O_3 TFT-based inverter. Most oxide semiconductor TFTs only have either n- or p-type devices and inverters are usually based on both n-type and p-type MOSFETs. A pseudo-CMOS design has been proposed in the experiment to realize an inversion function using only unipolar TFTs. Four types of pseudo-CMOS design inverters, i.e., pseudo

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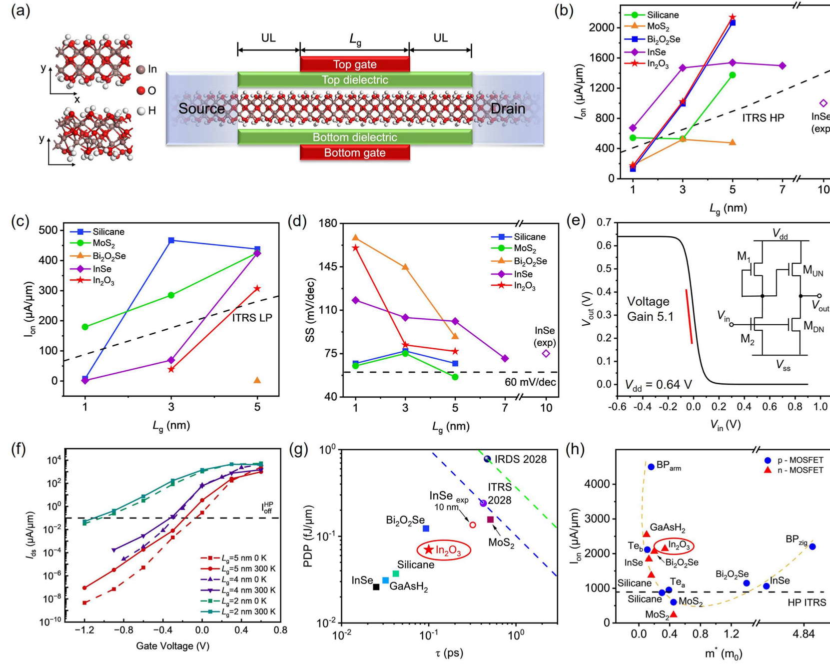

Figure 1 (Color online) (a) Atomic configuration of 0.7-nm thickness hydrogenated In_2O_3 structure (left) and schematic view of the double gate (DG) In_2O_3 TFT (right); comparison of (b) I_{on} (HP standard), (c) I_{on} (LP standard), (d) SS; (e) voltage transfer curves (VTCs) and circuit diagram of the In_2O_3-based pseudo depletion load inverter (PDL); (f) transfer characteristic curves of In_2O_3 TFTs with gate lengths of 5, 4, and 2 nm at temperatures of 0 and 300 K; (g) PDP vs. τ of the n-type 5-nm-L_g MOSFET with different channel materials for HP applications (the blue and green dashed lines are ITRS 2013 and IRDS 2022 version requirements of EDP, respectively; the 2028 technical nodes are denoted by purple and blue balls.); (h) I_{on} vs. m^* map of MOSFETs at $L_g = 5$ nm.

enhancement load inverter (PEL), pseudo depletion load inverter (PDL), linear enhancement load inverter (LEL), and conventional depletion load inverter (DL), are characterized to evaluate the performance of In_2O_3 TFTs on circuit level (Appendix F). Among four configurations, the PDL inverter achieves the highest voltage gain of 5 while maintaining rail-to-rail operation as shown in Figure 1(e).

Electron-phonon coupling (EPC) effect. The EPC effect is a critical factor affecting device performance in the nanoscale regime. Phonon-assisted tunneling increases off-state currents, particularly at elevated temperatures. Simulations using the special thermal displacement (STD) method are shown in Figure 1(f). The off-state current for a 5 nm L_g device increases by four orders of magnitude compared to 0 K. The I_{on} of the 4-nm-L_g device is reduced by approximately 36% due to the EPC effect, yet it still meets ITRS standards. Further analysis highlights the impact of EPC on the local device density of states (LDDOS) (Appendix G). The broadening and shifting of energy states under EPC modify the tunneling barrier, increasing the tunneling probability.

Conclusion. In_2O_3 TFTs demonstrate superior energy-delay product (EDP) compared to MoS_2 MOSFETs and achieve similar switching speeds with lower energy consumption than Bi_2O_2Se MOSFETs, ensuring excellent device performance. However, silicene, $GaAsH_2$, and InSe MOSFETs exhibit smaller EDPs. The U-shaped relationship between I_{on} and effective mass (m^*) in 5-nm-L_g MOSFETs highlights the trade-off between thermal velocity (v_{th}) and density of states (DOS) as shown in Figure 1(g). When $m^* < 0.4m_0$, v_t dominates I_{on}, whereas DOS becomes significant for $m^* > 0.4m_0$.

Discussion. In summary, we investigate 0.7-nm-thick In_2O_3 TFTs at sub-5 nm gate lengths. UL-optimized ultra-thin In_2O_3 TFTs meet ITRS HP and LP standards down to gate lengths of 3 and 4 nm, respectively. Compared to typical 2D FETs, they offer higher I_{on}, lower EDP, and reduced power consumption, outperforming Bi_2O_2Se MOSFETs. Pseudo-CMOS designs show rail-to-rail operation with voltage gains of 5 in PDL and DL inverters. At 4-nm gate length, they meet ITRS standards even at 300 K despite the modest EPC effect. Their high performance, energy efficiency, and transparency make them ideal for low-power logic circuits and transparent, flexible electronics.

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Supporting information Appendixes A–H. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

References

1 Quhe R, Xu L, Liu S, et al. Sub-10 nm two-dimensional transistors: theory and experiment. Phys Rep, 2021, 938: 1–72
2 Si M, Lin Z, Chen Z, et al. Scaled indium oxide transistors fabricated using atomic layer deposition. Nat Electron, 2022, 5: 164–170
3 Charnas A, Lin Z, Zhang Z, et al. Atomically thin In_2O_3 field-effect transistors with 1017 current on/off ratio. Appl Phys Lett, 2021, 119: 263503
4 Si M, Hu Y, Lin Z, et al. Why In_2O_3 can make 0.7 nm atomic layer thin transistors. Nano Lett, 2021, 21: 500–506
5 Si M, Lin Z, Chen Z, et al. High-performance atomic-layer-deposited indium oxide 3-D transistors and integrated circuits for monolithic 3-D integration. IEEE Trans Electron Devices, 2021, 68: 6605–6609