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An 85 mm×89 mm 64M pixel high-speed CMOS image sensor with a negative capacitance circuit

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CMOS image sensors (CIS) have supplanted charge-coupled devices as the dominant technology for consumer imaging applications because of their high integration, low power consumption, and affordability. As CMOS image sensor technology continues to advance, the demand for higher resolutions and faster frame rates increases. To achieve faster frame rates, large array CIS must be capable of reading image signals at high speeds. The current dominant architecture for CIS is column-parallel. As the array size expands, the column bus may extend to tens or even hundreds of millimeters, leading to a significant increase in parasitic effects. As a result, the frame rate is limited by the establishment time of the column bus signal.

Both domestic and international researchers have investigated this issue in depth. In [1], the parasitic capacitance between multilayer metal wires is reduced by optimizing the layout. However, the effectiveness of this approach is constrained. In [2], a two-sided readout architecture is utilized to increase the frame rate of large array image sensors. This design approach reduces the parasitic effects of the column bus. However, when compared with single-sided readout architecture, it doubles power consumption and significantly increases the chip area. The challenge of slow column bus signal establishment time in large array CIS should be the focus of further research. This study presents a high-speed column bus signal readout circuit designed for large array CIS. Without compromising the design of the pixel array or significantly increasing power consumption, the circuit integrates a negative capacitance circuit at the readout node of the column bus. This integration effectively reduces the establishment time of the column bus signal.

High speed column bus signal readout circuit. The readout speed of the column bus signal is influenced by the parasitic capacitance of the metal transmission line. To address this issue, a high-speed column bus readout circuit that features negative capacitance is employed. This circuit is designed to mitigate the effects of parasitic capacitance on the column bus, thereby enhancing the readout speed of the column bus signal. The high-speed column bus signal readout circuit, based on the principle of negative capacitance and its operational sequence, is illustrated in Figure 1(a). It comprises three CMOS transistors, two switches, a capacitance C_2, and a distributable capacitance C_3. During Φ_2, the linear model of the high-speed column bus signal readout circuit proposed in this study is depicted in Figure 1(b). The impedance variation of the linear model with the load is

$$Z = \frac{V_1}{i_1} = -\frac{1}{g_{m2}}\frac{1}{g_{m1}R}\frac{1+s\frac{C_2}{g_{m2}}(1+g_{m2}R)}{s\frac{C_2}{g_{m2}}}. \quad (1)$$

When $|s| \ll \frac{g_{m2}}{C_2(1+g_{m2}R)}$,

$$Z \approx -\frac{1}{g_{m1}R}\frac{1}{sC_2}; \quad (2)$$

when $|s| \gg \frac{g_{m2}}{C_2(1+g_{m2}R)}$,

$$Z \approx -\frac{1}{g_{m2}}\frac{1+g_{m2}R}{g_{m1}R}. \quad (3)$$

From (2) and (3), the linear model has a negative capacitance of $-g_{m1}RC_2$ when the frequency is lower than $g_{m2}/[C_2(1+g_{m2}R)]$.

At frequencies that exceed $g_{m2}/[C_2(1+g_{m2}R)]$, the linear model transitions into negative resistance. Linear models with non-ideal negative capacitance characteristics pose a risk of instability for the column bus signal. Hence, it is crucial to maximize the negative capacitance while also enlarging the zero frequency as much as possible. Greater negative capacitance values result in faster establishment speeds for large signals. However, heightened negative capacitance exacerbates loop instability, slows down small signal establishment, and prolongs the total signal establishment time. To address this design dilemma, capacitance C_3 is introduced in this study. During Φ_1, capacitances C_2 and C_3 are concurrently connected to the loop to achieve

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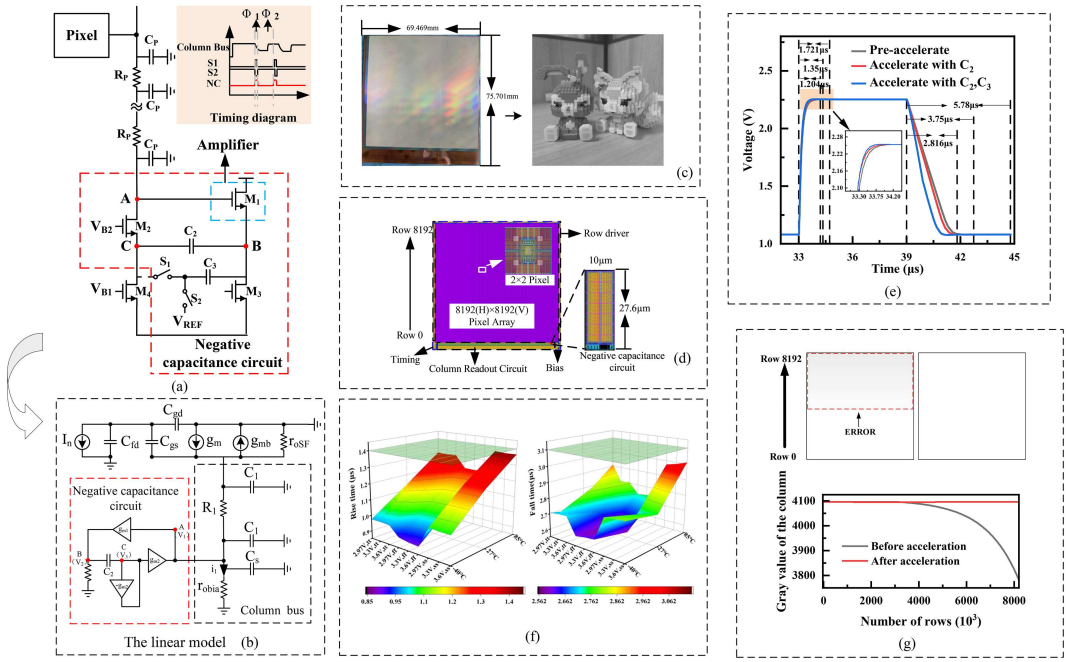

Figure 1 (Color online) (a) Proposed high-speed column bus signal readout circuit; (b) linear model of the high-speed column bus signal readout circuit; (c) large array CMOS image sensor chip on the design platform; (d) proposed layout design of a large array CMOS image sensor; (e) PVT simulation results for the rise time and the fall time; (f) output voltage waveforms of the column bus before and after acceleration; (g) output image and gray values: pre- and post-acceleration under high-intensity exposure.

a large negative capacitance and expedite large signal establishment. Subsequently, during Φ_2, capacitance C_3 is disengaged from the loop, reducing negative capacitance, enhancing loop stability, and accelerating small signal establishment. The dynamic loop adjustment technique enables the negative capacitance circuit to achieve a greater bandwidth and a quality factor closer to 5.

Simulation results. The high-speed column bus signal readout circuit proposed in this study completed the circuit design and layout design in an 8192 (H) by 8192 (V) CMOS image sensor based on the 55 nm 1P4M process. All parasitic parameters were extracted according to the actual layout. Figure 1(c) illustrates the successfully taped out CMOS image sensor. The simulation results obtained by the design platform are basically consistent with the chip test results. In this study, the proposed circuit is also fully verified based on this design platform. The overall layout design of the large array CMOS image sensor is shown in Figure 1(d). The height of the column readout circuit for the large array CMOS image sensor is 6.2 mm, with the negative capacitance circuit occupying only 27.6 μm. In the experiment environment built in this study, the output voltage swing of the column bus signal is 1.2 V, with a pixel pitch of 10 μm × 10 μm and a pixel bias current of 5 μA. The static and dynamic power consumptions of the proposed negative capacitor circuit are 3.3 and 20.7 μW, respectively. Figure 1(e) shows the output waveforms of the column bus before acceleration and when accelerated with C_2 and C_2, C_3. Based on the analysis presented in Figure 1(e), prior to acceleration, the rise time and the fall time of the column bus signal are 1.721 and 5.78 μs, respectively. The rise and fall times of the column bus signal are reduced to 1.204 and 2.816 μs, respectively, when capacitances C_2 and C_3 are used for acceleration. This accounts for a reduction of 30.04% in the rise time and 51.28% in the fall time of the column bus signal. As anticipated, the inclusion of capacitance C_3 enhances both stability and speed. Compared with using only capacitance C_2, the rise time and the fall time are reduced by 10.8% and 24.9%, respectively. In order to achieve the design goal of 27 fps, the rise and fall times of the column bus signal are designed to be 1.4 and 3.1 μs, respectively. Figure 1(f) shows the PVT simulation results for the rise and fall times of the column bus signal after acceleration. The experiment results show that the rise and fall times of the column bus signal meet the design requirements in all cases. Figure 1(g) depicts the output images before and after acceleration under strong exposure, with a row time of 4.5 μs. Before acceleration, because of the long establishment time of the column bus signal, the image exhibits graded horizontal stripes, leading to a row fixed pattern noise (RFPN) of 1.33%. After acceleration, image quality improves considerably, with the RFPN reduced to 0.01%. The additional noise introduced by the negative capacitance circuit is $0.27e^-$.

Conclusion. In this study, a high-speed column bus readout circuit is introduced and verified by experiment in an 8192 (H) × 8192 (V) CMOS image sensor. A negative capacitance circuit is used to offset the effect of column bus parasitic capacitance on the rise and fall times of column bus signals. The experiment results show that the rise and fall times of the column bus signal are reduced by 30.04% and 51.28%, respectively.

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