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Al_2O_3/AlN/GaN MOS-HEMTs on 6-inch silicon substrate with high transconductance and state-of-the-art $f_{max} \times L_G$

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Owing to their low cost, large wafer size, and easy heterogeneous integration, GaN-based high-electron-mobility transistors (HEMTs) on silicon substrates have been utilized as superior devices in high-frequency applications such as 5G communication and satellite radar [1–3]. Scaled-down GaN technology has gradually achieved high performance in the sub-6 GHz and millimeter-wave bands. However, the device structure and processes need to be optimized to mitigate the short-channel effect caused by the thick barrier layer and small gate length, gate leakage caused by the poor interface state, low breakdown voltage caused by the strong vertical electric field near the gate electrode, and low cut-off frequency caused by large parasitic resistances. Here we propose methods for improving the characteristics of HEMT devices.

To reduce the device geometry, we adopted an AlN/GaN heterojunction epitaxial structure with an electron sheet concentration of 1.7×10^{13} cm^{-2} and an AlN layer thickness within 5 nm. The breakdown voltage was increased using a gate dielectric of high-quality Al_2O_3 fabricated by atomic layer deposition. The gate leakage was suppressed with a low-damage remote plasma oxidation pre-treatment (PRO), which repairs the etching damage of the gate foot and hence improves the interface. Meanwhile, the ohmic contact resistance was decreased using regrown ohmic technology, which both increases the peak transconductance and decreases the knee voltage. Applying these materials and processes along with deep ultra-violet lithography to eliminate the short-channel effect and simplify the lithography process, we fabricated metal-oxide-semiconductor HEMTs (MOS-HEMTs) on a 6-inch silicon (Si) substrate with a gate length of 0.2 μm.

Experiment. To demonstrate the effects of regrown ohmic technology and low-damage PRO treatment on the device performance, we measured the direct current (DC) characteristics of three kinds of devices. We also verified the reliability of the surface interface from C-V hysteresis curves, pulsed I-V measurements, and finally performed a small-signal measurement. Figures 1(a) and (b) show a schematic of the Al_2O_3/AlN/GaN MOS-HEMTs with regrown ohmic contacts and an SEM image of the T-shape, respectively. All devices in this study have double-gate fingers with a total gate width of 100 μ m, a source/drain spacing (L_{SD}) of 2 μm, and a gate length (L_G) of 0.2 μm.

Results and discussion. Figures S2(a) and (b) show the ohmic contact resistances and sheet resistances of the MOS-HEMTs with alloyed and regrown ohmic contacts. Both MOS-HEMTs possess the same epi-structure and were fabricated using the same processes, differing only in their ohmic contact processing. In the MOS-HEMTs with alloyed ohmic contacts, the ohmic contact resistance, sheet resistance, and special contact resistivity were 0.67 Ω·mm, 338 $\Omega\cdot sq^{-1}$, and 1.3×10^{-5} $\Omega\cdot cm^{-2}$, respectively. In the MOS-HMETs with regrown ohmic contacts, the ohmic contact resistance was 0.1 Ω·mm and the special contact resistance was reduced by two orders of magnitude from that of its counterpart, suggesting that the regrown ohmic method effectively decreases the parasitic resistance.

Figures 1(c) and (d) compare the transfer and output characteristics, respectively, of the MOS-HEMTs with regrown and alloyed ohmic contacts. The transconductance was more than 200 $mS\cdot mm^{-1}$ larger in the MOS-HEMTs with regrown ohmic contacts than in its counterpart with alloyed ohmic contacts, owing to the reduced parasitic resistance in the former. Meanwhile, the on-resistance of the MOS-HEMTs with regrown ohmic contacts was 1.01 Ω·mm, half that of the MOS-HEMTs with alloyed ohmic contacts. Regrown ohmic contacts also reduced the knee voltage of

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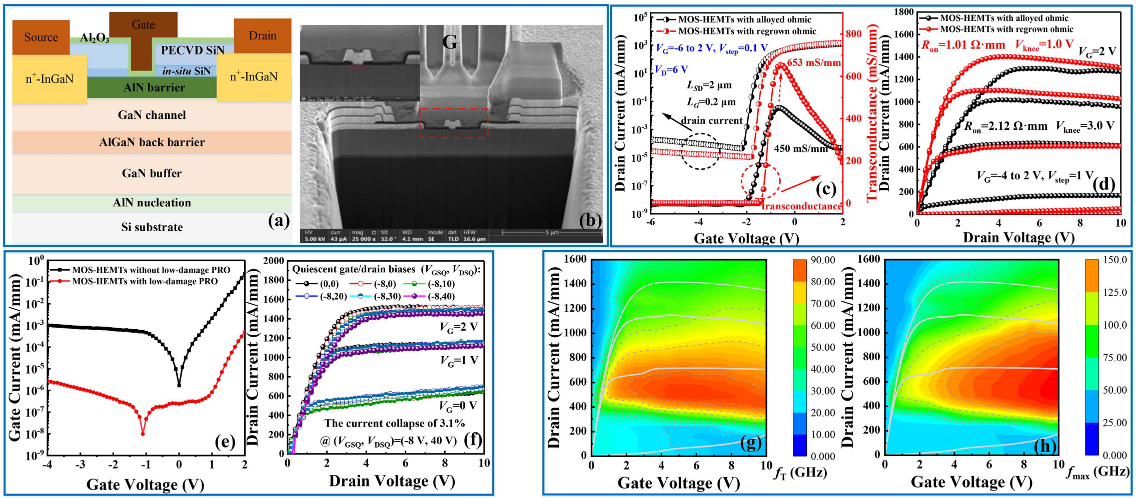

Figure 1 (Color online) (a) Schematic structure and (b) cross-sectional SEM image of Al_2O_3/AlN/GaN MOS-HEMTs on Si substrate with regrown ohmic contacts; (c) transfer and (d) output characteristics curves of the MOS-HEMTs with alloyed (black) and regrown (red) ohmic contacts on Si; (e) Schottky characteristics of the device in (a) without (black) and with (red) low-damage PRO treatment; (f) current collapse characteristics of MOS-HEMTs with regrown ohmic contacts; (g) f_T and (h) f_{max} contour plots of MOS-HEMTs with regrown ohmic contacts on Si.

the MOS-HEMTs to 1.0 V, demonstrating the potential of these MOS-HEMTs in efficient and high-frequency applications. The breakdown voltages of both HEMTs were similar (Figure S3(c)) owing to the epitaxial structure.

Next, the effect of low-damage PRO treatment on the device performance was evaluated. Figure 1(e) shows the Schottky curves of the Al_2O_3/AlN/GaN MOS-HEMTs with and without low-damage PRO treatment. Both devices were structured and processed as shown in Figure 1(a), differing only in their interface treatments. The low-damage PRO treatment reduced the Schottky leakage current of the MOS-HMETs by nearly three orders of magnitude, suggesting that this treatment effectively reduces interface defects and improves the quality of the contact between the gate dielectric and the AlN barrier layer, thereby suppressing the gate leakage.

To evaluate the quality of the Al_2O_3/AlN interface, the *C-V* hysteresis curves were measured at 100 kHz and 1 MHz. The results are shown in Figure S5(a). At the higher test frequency, some electrons lack sufficient time for release or capture, causing a positive drift in the threshold voltage. Moreover, as the trapped electrons cannot be released in time, a small voltage hysteresis appears. The *C-V* hysteresis was approximately 0.4 V at 100 kHz and less than 5 mV at 1 MHz, demonstrating the excellent quality of the fabricated interface. In addition, the interface trap density was 2.84×10^{12} cm^{-2} at 100 kHz and 3.53×10^{10} cm^{-2} at 1 MHz. The pulse *I-V* measurements were obtained at a pulse width of 500 ns and a period of 1 ms. Under different quiescent gate biases V_{GSQ} and quiescent drain biases V_{DSQ}, the MOS-HEMTs with regrown ohmic contacts showed negligible gate and drain delays. At $(V_{GSQ}, V_{DSQ}) = (-8$ V, 40 V), the current collapse was 3.1% (Figure 1(f)), suggesting few interface traps and a large passivation effect.

Figures 1(g) and (h) are contour plots of the cut-off frequency f_T and maximum oscillation frequency f_{max} of the Al_2O_3/AlN/GaN MOS-HEMTs, respectively. The small gate-channel spacing, high quality of the Al_2O_3/AlN interface, and regrown ohmic contact method reduced the parasitic resistance and parasitic capacitance, effectively improving the frequency characteristics of the HEMTs despite its relatively large L_G (0.2 μm). The f_T and f_{max} were obtained as 85 and 150 GHz, respectively. Moreover, the figure of merit $f_{max}\times L_G$ was 30 GHz·μm, surpassing (to our knowledge) those of all reported GaN HEMTs fabricated on Si substrates at low drain voltage [4, 5].

Conclusion. Al_2O_3/AlN/GaN MOS-HEMTs were successfully fabricated on a 6-inch Si substrate. The low-damage RPO treatment, Al_2O_3 dielectric, and regrown ohmic technology optimized the peak transconductance, maximum cut-off frequency, and maximum oscillation frequency of the MOS-HEMTs. Moreover, to our knowledge, the figure of merit $f_{max}\times L_G$ (30 GHz·μm) is state-of-the-art among the reported GaN-on-Si radio-frequency HEMTs and the figure of merit $f_T\times L_G$ (17 GHz·μm) exceeds that of most GaN-on-Si HEMTs. Therefore, the Al_2O_3/AlN/GaN MOS-HEMTs are potentially utilizable as high-performance scaled-down GaN HEMTs in high-frequency and low-voltage applications.

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Supporting information Appendix A and Figures S1–S5. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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