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An AND-type 1T-FeFET array with robust write and read operations

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HfO_2-based ferroelectric field-effect transistor (FeFET) has become a promising solution for next-generation embedded non-volatile memory (NVM) owing to its complementary metal-oxide-semiconductor (CMOS) compatibility, small footprint, high performance, and non-destructive readout [1]. Recent research of HfO_2-based FeFET has focused on the device operation mechanisms as well as reliability issues such as the interplay between polarization switching and charge trapping/detrapping [2], read-after-write latency [3] and endurance degradation [4]. It has been demonstrated that endurance higher than 10^{10} cycles with negligible read-after-write latency is possible if the gate stack of FeFET is well engineered [5]. Although the performance of FeFET has been significantly improved from the device level. Actual memory applications will require FeFET interconnecting in an array, where the write and read operations of the selected memory cell may affect the states of the neighboring un-selected cells. Investigation of array-level operations of FeFET is in desperate need of understanding the potential disturbing issues and optimization of operation schemes.

In this study, we have fabricated and systematically characterized FeFET cells as well as AND-type arrays with comparatively large sizes. The program disturb issue in an AND-type FeFET array is investigated and mitigated by applying suitable program inhibition schemes. In addition, the optimized read gate voltage (V_g) is determined by the trade-off between device-to-device (D2D) variation and the on/off ratio of drain current (I_d) according to both measurement and simulation results. Finally, robust write and read operations of a 1-kbit AND-type FeFET array are experimentally demonstrated with the optimized program and read conditions.

Experiment. Figure 1(a) illustrates the schematic of a FeFET cell as well as the cross-sectional transmission electron microscope (TEM) image of TiN/HZO/SiO_2/Si gate stack. The detailed fabrication process can be found in Appendix A. The gate length (L_g) and width (W) of characterized devices are 0.5 and 8 μm, respectively. Meanwhile, AND-type FeFET arrays are fabricated on the same wafer by the same process. To enable the highest storage density, using a single FeFET (1T) as a unit cell is preferred. Figure 1(b) shows the configuration of an AND-type 1T-FeFET array, where the bit-lines (BLs) and source-lines (SLs) connecting FeFET source/drain (S/D) run in row-wise, while the word-lines (WLs) connecting the gate run in column-wise. Note that all the cells share the same p-well, which enables erase in a block unit, and is suitable for memory arrays of large size. After array fabrication, the 1-kbit (32 × 32) AND-type FeFET array is packaged and mounted on a printed circuit board (PCB) for the electrical characterization (Figure 1(c)). Access to each cell and array-level operations is carried out by a customized switch matrix on a PCB for source selection.

Results and discussions. The basic characteristics of FeFET cells can be found in Appendix B. By implementing the operation schemes illustrated in Figure 1(d), each memory cell in an array can be accessed and written into different states. V_{PRG}, V_{ERS} and V_{RWL}/V_{RBL} represent program voltage, erase voltage and read voltage on WL/BL, respec-

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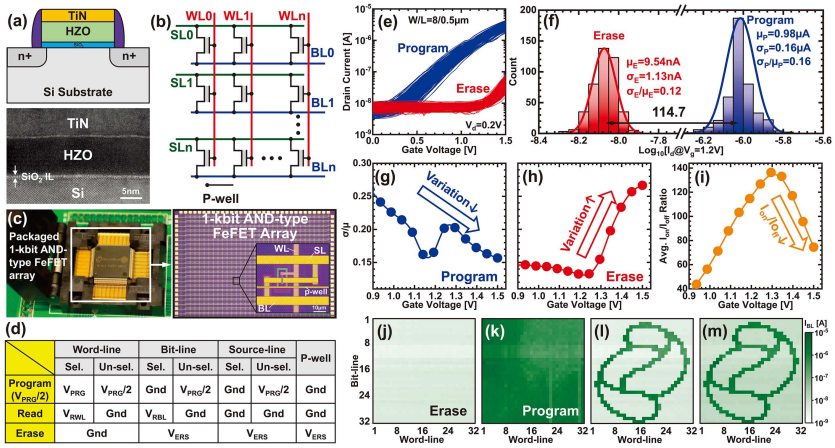

Figure 1 (Color online) (a) The schematic of a FeFET cell and the cross-sectional TEM image of TiN/HZO/SiO_2/Si gate stack in a fabricated device. (b) The configuration of an AND-type 1T-FeFET array in this study. (c) The packaged 1-kbit (32 × 32) AND-type FeFET array for electrical characterization. (d) Operation table of an AND-type FeFET array. (e) Read I_d-V_g of FeFET cells in a 1-kbit AND-type array. (f) Distribution of read I_d at V_g = 1.2 V for program and erase states. The normalized variation (σ/μ) of read I_d as a function of V_g for (g) program and (h) erase states. (i) The average ratio of read I_d in program and erase states (I_{on}/I_{off} ratio) versus V_g. Measured 2D mapping of BL current for (j) erase and (k) program states of each cell in a 1-kbit AND-type FeFET array. Measured 2D mapping of BL current of each cell after selective program for the (l) first and (m) hundredth cycles.

tively. Here, $V_{PRG}/2$ scheme is utilized for the inhibition of program disturb. The detailed disturb analysis, including both $V_{PRG}/2$ and $V_{PRG}/3$ bias schemes, can be found in Appendix C. Figure 1(e) plots read I_d-V_g of FeFET cells in a 1-kbit AND-type array. The statistical distributions of read I_d at V_g = 1.2 V for both program and erase states are summarized in Figure 1(f). The normalized variation (σ/μ) of read I_d at V_g = 1.2 V are 0.12 and 0.16 for program and erase states, respectively. The larger D2D variation in program state can be attributed to channel percolation paths formation around weak inversion by stochastic switching of ferroelectric domains, and random spatial fluctuation of ferroelectric and dielectric phases in polycrystalline HfO_2 thin film. Figures 1(g) and (h) plot σ/μ as a function of V_g for program and erase states, respectively. In the target range of read V_g, σ/μ increases as V_g becomes larger for the erase state while decreasing for the program state. This phenomenon can be explained by the fact that the largest σ/μ should be achieved around weak inversion due to channel percolation path formation. To realize the smallest variation of read I_d in the program state, read V_g should be as high as possible. However, the average on/off ratio of read I_d (I_{on}/I_{off} ratio) decreases significantly when V_g is higher than 1.3 V, as shown in Figure 1(i). As a result, the proper choice of read V_g is essential for the trade-off between D2D variation and I_{on}/I_{off} ratio, and therefore a high sense margin. Suitable read V_g would be even more essential for FeFET cells with smaller size (sub-100 nm), since the larger variation is induced by the limited number of grains in ferroelectric HfO_2. The corresponding analysis is provided in Appendix D.

According to the statistical analysis of measurement results, the optimum V_{RWL} for array-level operations is chosen to be 1.2 V for a high I_{on}/I_{off} ratio with acceptable variations. Figures 1(j) and (k) plot 2D mapping of the BL current for erase and program states of each cell in a 1-kbit AND-type FeFET array, respectively. Next, we selectively program the cells in an array to a target pattern by $V_{PRG}/2$ inhibition scheme. Figures 1(l) and (m) plot measured 2D mapping of the BL current of each cell after the selective program for the first and hundredth write cycles, respectively. Robust operations of 1-kbit AND-type FeFET array are experimentally demonstrated with excellent disturb immunity and decent I_{on}/I_{off} ratio.

Conclusion. We have investigated the feasibility of array-level operations of FeFET in AND configuration. FeFET devices as well as AND-type arrays have been fabricated and systematically characterized. The disturb-free operations are verified by measurement on both a single cell and an AND-type array. Moreover, optimum read V_g is determined according to the trade-off between D2D variation and I_{on}/I_{off} ratio. Such trade-off is even more essential for devices with small size in advanced technology nodes, since the larger variation is induced by a limited number of grains in ferroelectric HfO_2 as indicated by the simulation results. Finally, robust write and read operations of a 1-kbit AND-type FeFET array are experimentally demonstrated.

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Supporting information Appendixes A–D. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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