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• **Supplementary File** •

An AND-type 1T-FeFET array with robust write and read operations

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Appendix A Device Fabrication

The fabrication starts from p-type silicon substrates. After active area patterning, shallow trench isolation (STI) is performed by dry etching of silicon and chemical vapor deposition (CVD) SiO_2. Then, dummy gate is formed by thermal oxidation of silicon and CVD poly-silicon. After spacer formation, arsenic ions are implanted for source/drain (S/D) and activated by spike annealing. After dummy gate removal, ozone oxidation is carried out for better interface property. Next, 10nm $Hf_{0.5}Zr_{0.5}O_2$ (HZO) is deposited by atomic layer deposition (ALD). Subsequently, 20nm TiN and 75nm W are deposited by sputter and CVD, respectively. To crystalize HZO and induce ferroelectricity, rapid thermal annealing (RTA) is carried out in N2 ambient at 550℃ for 1min. Finally, metallization and interconnects are performed for electrical characterization.

Appendix B Basic Characteristics of FeFET Cells

To verify the ferroelectricity of fabricated FeFET cells, direct-current (DC) drain current versus gate voltage (I_d-V_g) of FeFET are characterized by varying maximum V_g from 2 to 4V (Fig. B1(a)-(c)). As maximum V_g increases, I_d-V_g evolve from charge-trapping-dominant clockwise hysteresis to polarization-switching-dominant counter-clockwise hysteresis [1]. The I_d-V_g in Fig. B1(c) exhibits larger counter-clockwise hysteresis than Fig. B1(b) since the more switched polarization at higher applied V_g.

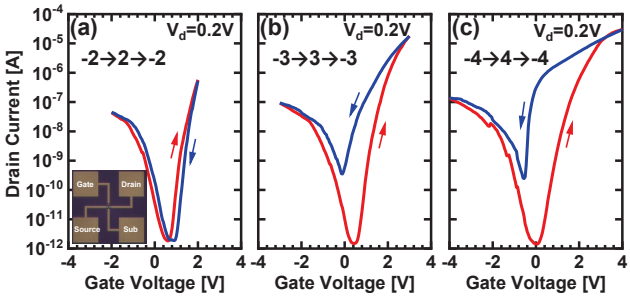

Figure B1 The measured DC I_d-V_g characteristics by varying maximum V_g from 2 to 4V. The microscopic image of a fabricated FeFET cell is shown in inset.

Fig. B2(a) plots the measured read I_d-V_g after write operations at both room temperature (RT) and 85℃. The FeFET cell is in program state (low threshold voltage (V_{th})) after applying a pulse with amplitude/width of 4V/100μs to the gate electrode. On the contrary, erase state (high V_{th}) is realized after applying a pulse with amplitude/width of -3V/100μs. Leakage current increases and V_{th} roll-off happens at elevated temperature for both program and erase states. Principally,

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the directions of $V_{\rm th}$ shift for program and erase states of FeFET should be opposite as temperature increases (i.e. $V_{\rm th}$) shifts toward right side for program state and left side for erase state), which is expected from the reduction of $|+P_{\rm r}|/|\text{-}P_{\rm r}|$ corresponding to program/erase state at higher temperature [2]. However, $V_{\rm th}$ shifts toward left side for both program and erase states at elevated temperature as observed in Fig. B2(a). Such phenomenon can be explained by the additional substrate effect (including electrostatics and carrier transport) and its dependence on temperature results in a shift of basic FET $I_{\rm d}$-$V_{\rm g}$ toward left side [3,4]. In this way, a larger $V_{\rm th}$ shift toward left side happens as temperature increases for erase state, since the superposition of the influence by $|\text{-}P_{\rm r}|$ reduction and substrate effect. On the contrary, the influence of these two factors compensates for program state and smaller $V_{\rm th}$) shift toward left side occurs (Fig. B2(a)).

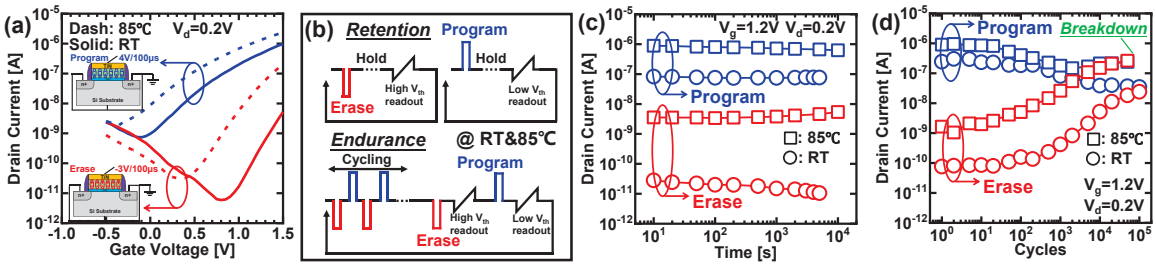

Figure B2 (a) The read $I_{\rm d}$-$V_{\rm g}$ curves after write operations at RT (solid) and 85℃ (dash). (b) Pulse schemes for retention and endurance measurements. (c) Retention and (d) endurance characteristics of fabricated FeFET cells at RT (circle) and 85℃ (square).

Next, retention and endurance characteristics are measured by the schemes illustrated in Fig. B2(b). The amplitudes and widths of $V_{\rm g}$ pulses for endurance cycling are same as the write process depicted in Fig. B2(a). The $I_{\rm d}$ readout is performed at $V_{\rm g}$=1.2V and $V_{\rm d}$=0.2V for both retention and endurance measurements. Fig. B2(c) and (d) plot retention and endurance characteristics of a fabricated FeFET cell at both RT and 85℃, respectively. Negligible $I_{\rm d}$ shift is observed for program and erase states within the maximum retention time of 10^4s at 85℃, which indicates excellent retention of our fabricated FeFET cells. Thanks to the comparatively high coercive field ($E_{\rm c}$) of ferroelectric HfO_2, retention is significantly improved compared to the previous FeFET with perovskite ferroelectric material [5]. However, the on/off ratio of $I_{\rm d}$ at $V_{\rm g}$=1.2V decreases at 85℃ because of $V_{\rm th}$ roll-off as indicated in Fig. B2(a). The read $V_{\rm g}$ at which the highest on/off ratio of $I_{\rm d}$ is achieved shifts to the lower value at higher temperature. Therefore, the optimum read $V_{\rm g}$ should be carefully chosen by considering the fluctuation of read $I_{\rm d}$-$V_{\rm g}$ in the target range of operation temperature [3,4]. For the endurance characteristics, the on/off ratio of $I_{\rm d}$ degrades after cycling due to charge trapping and trap generation [6,7], especially for 85℃ where a hard breakdown happens after 5×10^4 cycles because of the enhanced charge trapping and trap generation at higher temperature.

Appendix C Operations of AND-type FeFET Arrays and Disturb Analysis

	Word-line		Bit-line		Source-line		P-well
	Sel.	Un-sel.	Sel.	Un-sel.	Sel.	Un-sel.	
Program (V_{PRG}/2)	V_{PRG}	V_{PRG}/2	Gnd	V_{PRG}/2	Gnd	V_{PRG}/2	Gnd
Program (V_{PRG}/3)	V_{PRG}	V_{PRG}/3	Gnd	2V_{PRG}/3	Gnd	2V_{PRG}/3	Gnd
Read	V_{RWL}	Gnd	V_{RBL}	Gnd	Gnd	Gnd	Gnd
Erase	Gnd		V_{ERS}		V_{ERS}		V_{ERS}

Figure C1 Operation table of an AND-type FeFET array.

Fig. C1 summarizes the operation bias schemes for AND-type FeFET arrays in this study. Readout is performed by applying read voltages to the WL and BL ($V_{\rm RWL}$ and $V_{\rm RBL}$) of the selected cell with other lines grounded. Erase is performed in a block unit by applying an erase voltage ($V_{\rm ERS}$) pulse to all the BLs, SLs and p-well, while all the WLs are grounded. For program operation, a program voltage ($V_{\rm PRG}$) pulse is applied to the WL of the selected cell with the corresponding SL/BL grounded. Meanwhile, $V_{\rm PRG}/2$ is applied to the rest of WLs/SLs/BLs for the $V_{\rm PRG}/2$ inhibition scheme. Alternatively, $V_{\rm PRG}/3$ and $2V_{\rm PRG}/3$ are applied to the un-selected WLs and the un-selected BLs/SLs for the $V_{\rm PRG}/3$ inhibition scheme, respectively. To investigate the feasibility of program inhibition schemes (Fig. C2(a)), the corresponding voltage bias is applied to a FeFET cell to emulate the bias conditions of WL/BL half-selected cells (sharing the same WL/BL with the selected cell) and un-selected cells in program operations. Negligible shift of $I_{\rm d}$ at $V_{\rm RWL}$=1.2V and $V_{\rm RBL}$=0.2V is observed after 10^4 disturb cycles with 100μs pulse width for both $V_{\rm PRG}/2$ and $V_{\rm PRG}/3$ bias schemes as shown in Fig. C2(b) and (d), respectively. However, $V_{\rm PRG}/3$ bias scheme exhibits a little bit improvement of disturb immunity for WL/BL half-selected cells with the sacrifice of more cells under disturb (Fig. C2(d)). In addition, Fig. C2(c)

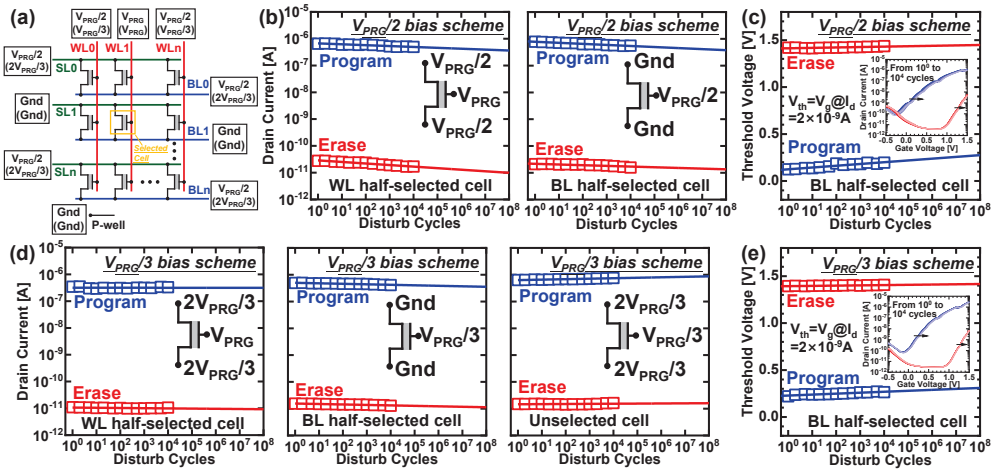

Figure C2 (a) The $V_{\rm PRG}/2$ and $V_{\rm PRG}/3$ bias schemes for the immunity of program disturb. (b) The measured $I_{\rm d}$ versus disturb cycles (100μs) for WL/BL half-selected cells with $V_{\rm PRG}/2$ bias scheme. (c) $V_{\rm th}$ as a function of disturb cycles for the BL half-selected cells with the $V_{\rm PRG}/2$ bias scheme. (d) The measured $I_{\rm d}$ versus disturb cycles for WL/BL half-selected cells and unselected cells with $V_{\rm PRG}/3$ bias scheme. (e) $V_{\rm th}$ as a function of disturb cycles for the BL half-selected cells with the $V_{\rm PRG}/3$ bias scheme.

and (e) plot $V_{\rm th}$ as a function of disturb cycles for the BL half-selected cells with $V_{\rm PRG}/2$ and $V_{\rm PRG}/3$ bias schemes as examples, respectively. The insets show the corresponding read $I_{\rm d}$-$V_{\rm g}$. Here, $V_{\rm th}$ is defined as the $V_{\rm g}$ where $I_{\rm d}$ is 2×10^{-9}A. The evolution of $V_{\rm th}$ shows the same trend as read $I_{\rm d}$, which further confirms the disturb-free program operations. The slight $I_{\rm d}$ or $V_{\rm th}$ shift as the increment of disturb cycles is mainly due to charge trapping in the gate stack, as $I_{\rm d}$ of program and erase states shifts to the same direction. Furthermore, $I_{\rm d}$ shift with $V_{\rm PRG}/3$ bias scheme is smaller than the case with $V_{\rm PRG}/2$ bias scheme because of the weaker charge trapping effect at lower bias.

Appendix D Trade-off between Variation and $I_{\rm on}/I_{\rm off}$ ratio for Devices with Small Size

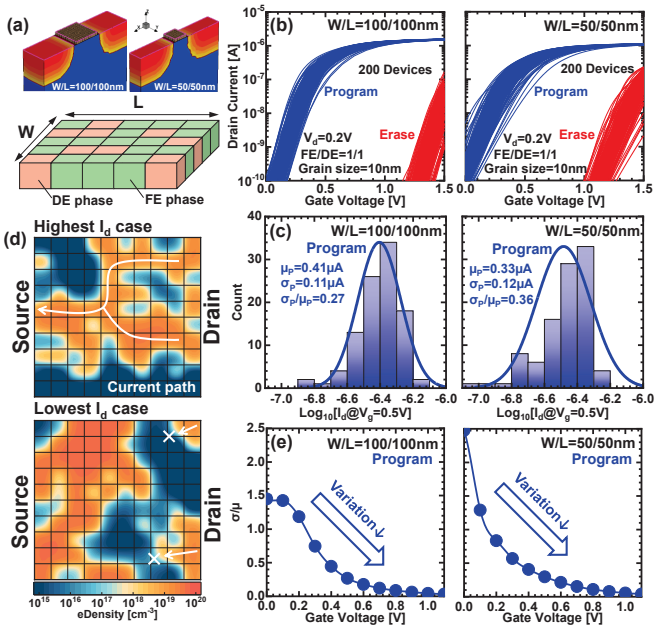

Figure D1 (a) The device structures in simulation and illustration of random spatial fluctuation of FE and DE phases. (b) The simulated read $I_{\rm d}$-$V_{\rm g}$ after write of 200 FeFET cells with size of W/L=100/100nm and 50/50nm. (c) Distribution of read $I_{\rm d}$ at $V_{\rm g}$=0.5V for program states of FeFET cells. (d) Two cases of 2D electron density distribution with highest and lowest $I_{\rm d}$ at $V_{\rm g}$=0.5V for FeFET cells with size of W/L=100/100nm in program state. (e) The calculated σ/μ of read $I_{\rm d}$ as a function of $V_{\rm g}$ for program state.

The trade-off between D2D variation and $I_{\rm on}/I_{\rm off}$ ratio would be more essential for FeFET cells with smaller size (sub-100nm), since the larger variation induced by the limited number of grains in ferroelectric HfO_2. To investigate such trade-off for smaller devices which are the cases for actual FeFET applications in advanced technology nodes, numerical simulation of

memory characteristics of FeFET cells with W/L=100/100nm and 50/50nm are carried out with Sentaurus^{TM} technology computer-aided design (TCAD) by considering random spatial fluctuation of ferroelectric (FE) and dielectric (DE) phases (Fig. D1(a)). The grain size of FE HfO_2 is assumed to be 10nm in the simulation. To describe polarization switching of ferroelectric phases, Preisach model is implemented in the simulation [4, 8]. The remnant polarization (P_r), saturation polarization (P_s), relative dielectric constant (ε_r) and coercive field (E_c) of FE HfO_2 are 20.1μC/cm^2, 23μC/cm^2, 35 and 1.16 MV/cm, respectively, which are same as the calibration values in Ref. [8]. Fig. D1(b) plots simulation results for read I_d-V_g of 200 devices after write operations ($\pm$7V, 100μs). Larger D2D variation is observed for devices with W/L=50/50nm (σ/μ=0.36) than W/L=100/100nm (σ/μ=0.27) as shown in Fig. D1(c). The larger D2D variation of devices with smaller size is attributed to the more severe influence by the assumed random spatial fluctuation of FE and DE phases. To directly visualize the physical origin of D2D variation, Fig. D1(d) plots two cases of 2D electron density distribution with highest and lowest I_d at V_g=0.5V for FeFET cells with size of W/L=100/100nm in program state. For the highest I_d case, a conduction path with high electron density is formed between source and drain. However, for the lowest I_d case, the conduction path is cut off by a region with low electron density. Fig. D1(e) plots the calculated σ/μ of read I_d as a function of V_g for FeFET cells in program state. The trend is consistent with the measurement results in Fig. 1(g), however, with larger values of σ/μ because of smaller grain number. Therefore, the appropriate choice of read V_g would be even more important for devices with small size.

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