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Logic-in-memory cell enabling binary and ternary Boolean logics

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Abstract In computing systems, processing and memory units have been integrated into logic-in-memory (LiM) to enhance the computational efficiency and performance. LiM has been attempted to perform not only binary but also ternary logic functions, which reduces computing complexity. Herein, we demonstrate a binary and ternary LiM (BT-LiM) cell with eight triple-gated (TG) feedback field-effect transistors (FBFETs) reconfigured into *n*- or *p*-channel modes. The TG FBFETs exhibit symmetrical latch-up voltages and an on-current ratio of 1.02 between the *n*- and *p*-channel modes, which indicates a high potential for reconfigurable logic applications. The BT-LiM cell can perform YES, NOT, AND, OR, NAND, NOR, XNOR, and XOR logic functions in a single cell because of these reconfigurable characteristics. Further, binary and ternary logic functions are realized in the cell without a programming stage, and the cell maintains the results of the logic functions under zero-bias conditions. This study achieves multifunctional LiM that can operate all binary and ternary Boolean logics.

Keywords logic-in-memory, reconfigurable channel modes, ternary logic, triple-gated feedback field-effect transistors

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1 Introduction

Ternary logic has attracted significant attention in the fields of artificial intelligence and the Internet of Things. Big data can be handled more efficiently using trits in ternary logic compared to using bits in binary logics [1–5]. Ternary logic effectively reduces computing complexity by 63.1% compared to that using binary logics [6]. The logic gates with a small footprint and high tunability are highly desirable for efficient multifunctional hardware architectures. Binary- and ternary-compatible logic systems have been designed for a new computing paradigm given the rapidly growing demand for electronic devices with diverse functions [7–12]. In these systems, two-valued binary and three-valued ternary logics need to be matched so that conversion from the binary to ternary-logic systems, and vice versa, is necessary. However, conversion issues such as those requiring programming stages or changes in supply voltage (V_{SUP}) remain unresolved. Further, most binary and ternary multifunctionalities are applied to inverters alone, and their practical applications are limited.

Logic-in-memory (LiM) computing has been studied actively for data-intensive applications to overcome the von Neumann bottleneck [13–16], and integrating processing and memory units into the LiM can help significantly simplify the computing systems. Consequently, a system that can perform both binary- and ternary-compatible logic functions and LiMs offers substantial advantages in terms of computational efficiency and performance. Feedback field-effect transistors (FBFETs) are suitable for binary- and ternary-compatible logic functions and LiMs owing to their steep switching and memory characteristics [17–21]. In addition, FBFETs with two or three gate electrodes can be reconfigured into *n*- and *p*-channel modes, which makes them suitable for reconfigurable logic applications [22–25].

In this study, we designed a binary and ternary logic-in-memory (BT-LiM) cell with eight triple-gated (TG) FBFETs to demonstrate LiM operations for eight different basic Boolean logic gates (YES, NOT, AND, OR, NAND, NOR, XNOR, and XOR) using technology computer-aided design (TCAD) simulations. The ability to implement eight Boolean logic gates in a single cell is attributed to the

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reconfigurable characteristics of TG FBFETs. In addition, ternary-logic operations fully encompass binary-logic operations in the cell, and therefore, there is no need for programming steps or additional circuits to convert between binary and ternary logic.

2 Result and discussion

2.1 Design of TG FBFETs and BT-LiM cells

Figure 1(a) shows the schematic and circuit symbols of reconfigurable TG FBFETs. The TG FBFET has a p^+-i-n^+ Si nanowire structure with one control-gate (CG) and two program-gate (PG) electrodes in the channel region. The n- and p-channel modes in a transistor can be reconfigured by changing the polarity of the programmable gate voltage ($V_{\rm PG}$). The electrostatic doping occurs when the applied $V_{\rm PG}$ generates an electric field that induces charge carriers in the channel regions under PGs. The channel regions beneath the PGs are electrostatically doped as n-type (n^*) when a positive $V_{\rm PG}$ is applied, resulting in a p^+-n^*-i-n^*-n^+ structure for the n-channel mode. In this structure, the p^+ region is a drain region, the n^*-i region is a channel region, and the n^*-n^+ region is a source region. The TG FBFET with a positive $V_{\rm PG}$ operates in the n-channel mode. Herein, the control gate voltage ($V_{\rm CG}$) modulates the height of the potential barrier in the CG region, regulating the electron injection into the channel region to make the transistor in the n-channel mode be in the ON state or the OFF state. In contrast, the channel regions beneath the PGs are doped electrostatically as p-type (p^*) when a negative $V_{\rm PG}$ is applied; thus, the transistor has a p^+-p^*-i-p^*-n^+ structure for the p-channel mode. In this structure, the p^+-p^* region is a drain region, the i-p^* region is a channel region, and the n^+ region is a source region. The TG FBFET with a negative $V_{\rm PG}$ operates in the p-channel mode. $V_{\rm CG}$ regulates the hole injection into the channel region, enabling the transistor in the p-channel mode to be in the ON state or the OFF state.

A single BT-LiM cell can execute multiple Boolean logic operations because of the reconfigurable characteristics of TG FBFETs. Figure 1(b) shows a schematic of a BT-LiM cell. In the cell, eight TG FBFETs are connected in series and parallel and reconfigured into n- and p-channel modes depending on the logic gates; these transistors operating in n- or p-channel modes are represented as switches. The n- and p-channel modes exhibit symmetrical transfer characteristics, which can be classified into three zones (Figure 1(b), left). In zones ① and ③, the n- and p-channel modes are in opposite states. The cell performed a binary logic operation using $V_{\rm CG}$ values in zones ① and ③ as the input voltage ($V_{\rm IN}$). In binary logic, two different current paths in the cell are created depending on $V_{\rm IN}$s. Output logic "−1" is defined when a current path is created between the common source voltage ($V_{\rm SS}$) and output voltage ($V_{\rm OUT}$); output logic "+1" is defined when a current path is created between the common drain voltage ($V_{\rm DD}$) and $V_{\rm OUT}$. However, in zone ②, both n- and p-channel modes were in the ON state. $V_{\rm CG}$ is used in this zone as $V_{\rm IN}$ enables the connection between $V_{\rm DD}$ and $V_{\rm SS}$, and therefore, the intermediate state is defined as output logic "0". Here, both pull-up and pull-down networks have similar resistance, and therefore, the use of $V_{\rm CG}$ values corresponding to all three zones as $V_{\rm IN}$ enables ternary logic operations in the cell. Note that the component transistors of the cell reconfigured into the n- or p-channel modes by the $V_{\rm PG}$ can be in the ON states or the OFF states with different $V_{\rm CG}$ (or $V_{\rm IN}$) configurations.

2.2 Electrical characteristics and operation mechanism of TG FBFETs

In the BT-LiM cell, TG FBFETs can be positioned in pull-up or pull-down networks depending on the logic gate, and therefore, they operate under voltages applied at the drain ($V_{\rm D}$) or source ($V_{\rm S}$). Figure 2 shows the transfer characteristics of the n- and p-channel modes of a TG FBFET under various $V_{\rm S}$ and $V_{\rm D}$ values and the energy band diagrams describing the operation mechanisms. The transistor operated in the n-channel mode when a $V_{\rm PG}$ of 2.0 V was applied (Figure 2(a)). The drain-source current ($I_{\rm DS}$) increases abruptly as $V_{\rm CG}$ increases from −3.0 to 3.0 V, and the transistor switches from the OFF state to the ON state because of a positive feedback mechanism. The latch-up voltage ($V_{\text{latch-up}}$) shifts in the negative voltage direction from −1.2 to −1.6 V as $V_{\rm S}$ varies from −1.2 to −1.6 V. $V_{\text{latch-up}}$ increases to ∼−0.03 V when a positive $V_{\rm D}$ value is applied to the n-channel mode. In comparison, when a negative $V_{\rm S}$ is applied (Figure 2(b)), $V_{\text{latch-up}}$ exhibits nearly the same value regardless of the $V_{\rm D}$ variation.

In the energy band diagram (Figure 2(c)), potential barriers for electrons and holes are generated in the CG and drain-side PG regions, respectively, under a $V_{\rm PG}$, $V_{\rm CG}$, and $V_{\rm S}$ of 2.0, −3.0, and −1.6 V, re-

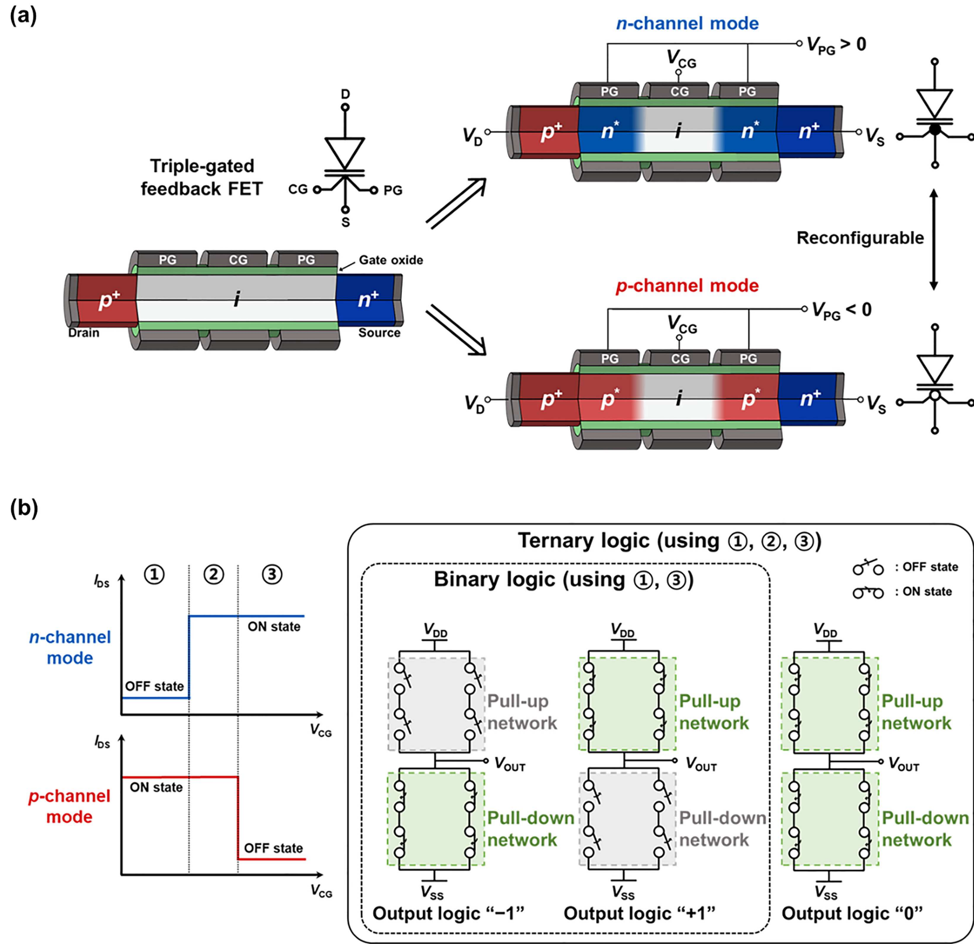

Figure 1 (Color online) Design of the TG FBFET and BT-LiM cell. (a) Schematics and circuit symbols of reconfigurable TG FBFETs; (b) schematics of BT-LiM cell.

spectively. Despite the continuous supply of electrons attributed to the negative V_S, the potential barrier in the CG region prevents electron injection into the channel, which results in the OFF state. However, the height of the potential barrier for electrons decreased with an increase in V_{CG} to 3.0 V. The electrons were injected into the channel region, and the latch-up phenomenon occurred through a positive feedback loop. Conversely, V_D was applied instead of V_S and holes were supplied from the drain (Figure 2(d)). The hole injection into the channel region is less affected by V_{CG} because it directly regulates the height of the potential barrier for electrons in the n-channel mode. Therefore, latch-up occurs at a higher V_{CG} when applying V_D than that when applying V_S.

For the p-channel mode with the positive V_D, the latch-up phenomenon occurs as V_{CG} decreases from 3.0 to -3.0 V, and $V_{\text{latch-up}}$ increases from 1.2 to 1.6 V as V_D increases from 1.2 to 1.6 V (Figure 2(e)). Conversely, with negative V_S, $V_{\text{latch-up}}$ is left-shifted to $\sim$0.04 V compared to the positive V_D (Figure 2(f)). Further, the variation in $V_{\text{latch-up}}$ for V_D is almost negligible. In the energy band diagram (Figure 2(g)), the potential barrier for holes (electrons) in the CG region (PG region near the source) is generated at a V_{PG}, V_{CG}, and V_D of -2.0, 3.0, and 1.6 V, respectively, and therefore, the transistor is in the OFF state. Then, the potential barrier for holes is lowered, and the injected holes trigger the positive feedback loop as V_{CG} decreases to -3.0 V. The V_{CG} cannot directly control the injection of electrons when electrons are supplied with a negative V_S because of the potential barrier for holes in the CG region in the p-channel mode (Figure 2(h)). Hence, $V_{\text{latch-up}}$ is left shifted when V_S is applied compared with V_D.

The TG FBFET exhibited symmetrical characteristics between the n- and p-channel modes with a symmetric $V_{\text{latch-up}}$ and on-current ratio of 1.02. In both the n- and p-channel modes, the transistor exhibited a high ON/OFF current ratio of $\sim 10^{12}$. These characteristics are crucial for universal logic

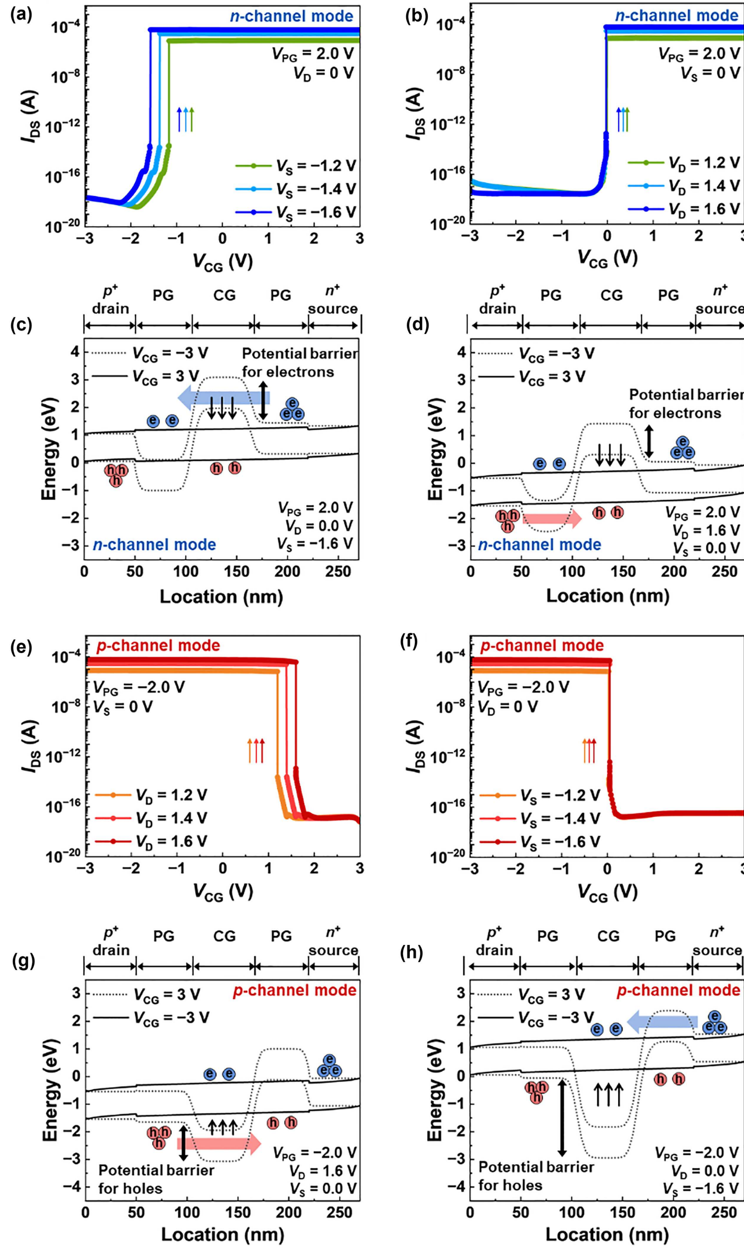

Figure 2 (Color online) Electrical characteristics and operation mechanism of the TG FBFET. Transfer characteristics of the n-channel mode TG FBFET under various (a) $V_{\rm S}$ and (b) $V_{\rm D}$; energy band diagrams of the n-channel mode TG FBFET at $V_{\rm CG}$ = −3 and 3 V under (c) $V_{\rm S}$ = −1.6 V and (d) $V_{\rm D}$ = 1.6 V; the transfer characteristics of the p-channel mode TG FBFET under various (e) $V_{\rm D}$ and (f) $V_{\rm S}$; energy band diagrams of the p-channel mode TG FBFET at $V_{\rm CG}$ = −3 and 3 V under (g) $V_{\rm D}$ = 1.6 V and (h) $V_{\rm S}$ = −1.6 V.

applications. Further, regardless of whether $V_{\rm D}$ or $V_{\rm S}$ is applied, a zone existed in which both the n- and p-channel modes were in the ON state. These are the essential characteristics to define the three states in ternary logic, which enables implementing binary-ternary compatible cells. Moreover, the transistor can be utilized in LiM applications because of its ability to store charge carriers in the channel region.

2.3 BT-LiM cell comprising eight TG FBFETs

Utilizing the switching and memory characteristics of the component TG FBFETs, the BT-LiM cell performed LiM operations under the following conditions. The $V_{\rm SUP}$, $V_{\rm PG}$, and two input voltages ($V_{\rm IN1}$ and $V_{\rm IN2}$) are applied with a pulse width of 1 ms. Throughout all logic operations, $V_{\rm DD}$ and $V_{\rm SS}$, which correspond to $V_{\rm SUP}$, are set to 1.95 and −1.95 V, respectively. The $V_{\rm PG}$ values required for the component

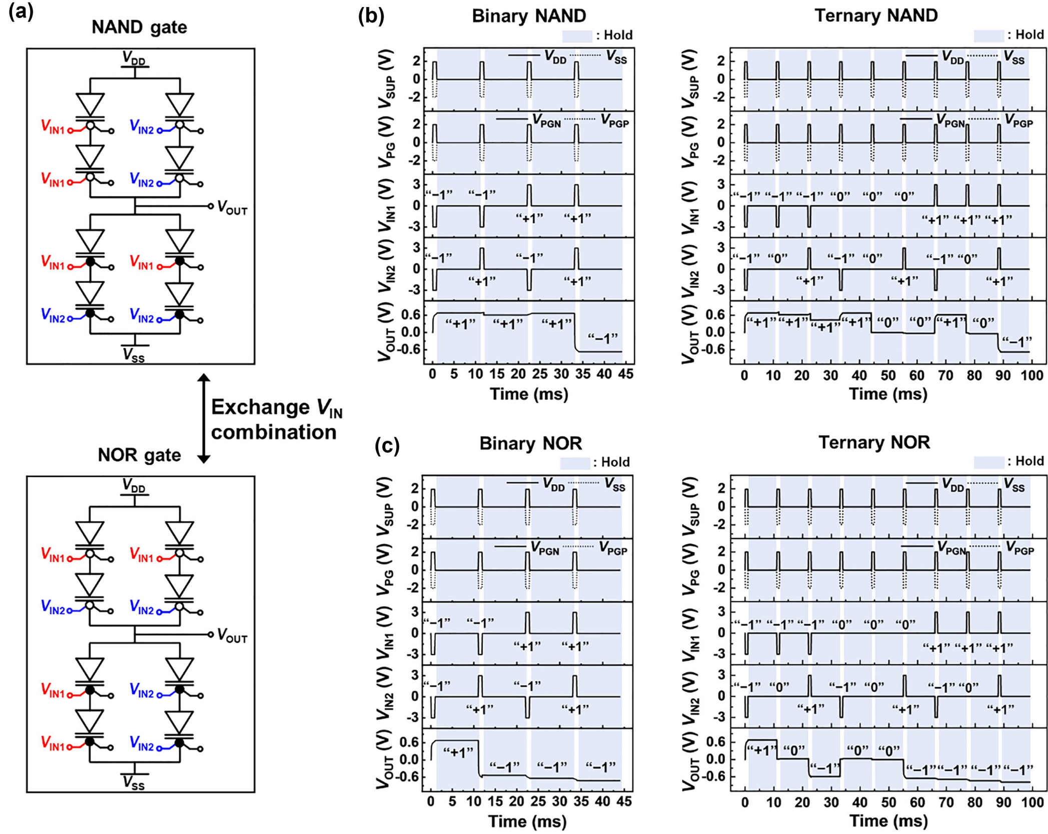

Figure 3 (Color online) BT-LiM cell operating as NAND and NOR gates. (a) Circuit diagrams for the NAND and NOR gates; (b) timing diagrams for the binary and ternary LiM operations of the NAND gate; (c) timing diagrams for the binary and ternary LiM operations of the NOR gate.

transistors operating in the n- ($V_{\rm PGN}$) and p-channel modes ($V_{\rm PGP}$) are 2.0 and −2.0 V, respectively. The $V_{\rm IN}$ values are applied to the CGs of the component transistors to determine the ON or OFF states of each transistor. In the binary logic operations, $V_{\rm IN1}$ and $V_{\rm IN2}$ are −3.0 and 3.0 V for the input logics "−1" and "+1", respectively. In the ternary logic operations, $V_{\rm IN1}$ and $V_{\rm IN2}$ values of 0 V are applied as the input logic "0", leading to the ON state in both the n- and p-channel modes. The ON or OFF states of each transistor determine $V_{\rm OUT}$ through voltage division. In the binary logic operation, the $V_{\rm OUT}$ appears as ∼−0.6 and 0.6 V, representing the output logic "−1" and "+1", respectively. In the ternary logic operations, there is an additional output logic "0" close to 0 V besides the two previous logic states. Immediately after each logic operation, the hold operation is performed for 10 ms. During the hold operation, all voltages applied during the logic pulse ($V_{\rm SUP}$, $V_{\rm PG}$, $V_{\rm IN1}$, and $V_{\rm IN2}$) are set to 0 V. The $V_{\rm OUT}$ values of the logic operations are maintained during the hold operation because of the memory characteristics of the transistors.

A BT-LiM cell executes various logical operations. This can be achieved by (1) varying $V_{\rm IN}$ to either $V_{\rm IN1}$ or $V_{\rm IN2}$ while maintaining the same cell configuration, and (2) reconfiguring the component transistors into either the n- or p-channel mode. Combining these two methods enables the cell to perform all eight Boolean logic operations.

2.4 NAND and NOR LiM operations or the BT-LiM cell

In a BT-LiM cell, the NAND and NOR logic operations are executed with the same cell configuration comprising four p-channel (n-channel) mode TG FBFETs in a pull-up (pull-down) network (Figure 3(a)). The $V_{\rm IN}$ combination takes the form in which the pull-ups and pull-downs are opposite for these two logic gates. Figure 3(b) shows that a single NAND gate performed both binary and ternary LiM operations. For the binary NAND operation, input logics (−1, −1), (−1, +1), (+1, −1), and (+1, +1) are successively applied. In the pull-up network, the same $V_{\rm IN}$ is applied to the p-channel mode transistors connected in series, applying input logic "−1" as $V_{\rm IN1}$ or $V_{\rm IN2}$ leads to output logic "+1". In contrast, in the pull-down

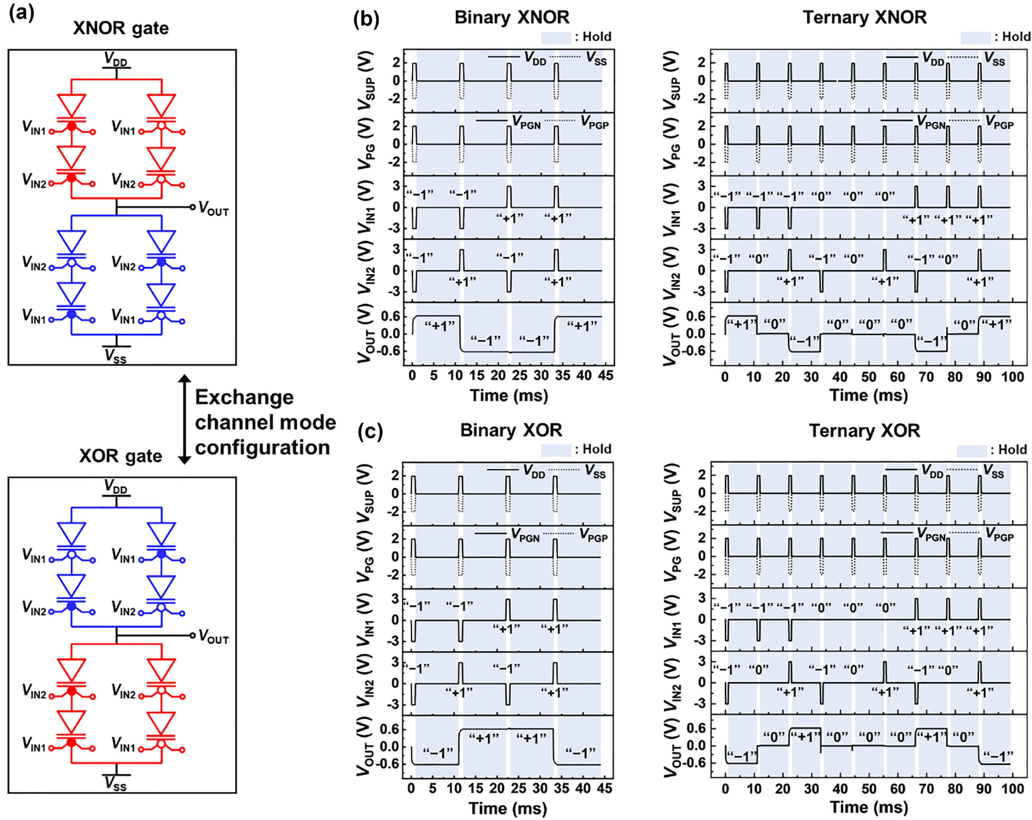

Figure 4 (Color online) BT-LiM cell operating as XNOR and XOR gates. (a) Circuit diagrams for the XNOR and XOR gates; (b) timing diagrams for binary and ternary LiM operations of the XNOR gate; (c) timing diagrams for the binary and ternary LiM operations of the XOR gate.

network, different $V_{\rm IN}$s are applied to the n-channel mode transistors connected in series, and output logic "−1" is obtained only when both $V_{\rm IN1}$ and $V_{\rm IN2}$ correspond to input logic "+1".

In the ternary NAND operation, input logics (−1, −1), (−1, 0), (−1, +1), (0, −1), (0, 0), (0, +1), (+1, −1), (+1, 0), and (+1, +1) are successively applied. When $V_{\rm IN} = 0$ V was applied, both the n- and p-channel mode TG FBFETs were in the ON state. Therefore, for input logics (0, 0), (0, +1), and (+1, 0), the transistors connected in series in both the pull-up and pull-down networks enter the ON state, thereby resulting in $V_{\rm OUT}$ close to 0 V. Binary and ternary LiM operations can be executed without any programming stage or changing $V_{\rm SUP}$. The ternary logic operations are performed by adding input logic "0". Thus, excluding the results for input logics (−1, 0), (0, −1), (0, 0), (0, +1), and (+1, 0) where 0 V is applied to $V_{\rm IN1}$ or $V_{\rm IN2}$ in ternary logic, the outcomes are identical to those of the binary logic operation.

In the binary NOR operation in Figure 3(c), output logic "−1" is obtained whenever input logic "+1" is applied to one or both inputs, and output logic "+1" is obtained only when all $V_{\rm IN1}$ and $V_{\rm IN2}$ correspond to input logic "−1". The ternary logic operation becomes feasible in the cell performing binary logic operations by adding input logic "0" to either $V_{\rm IN1}$ or $V_{\rm IN2}$. Moreover, the output values of the logic operations in both the NAND and NOR gates are retained without any external bias during the hold operation following each logic pulse. This can be attributed to the ability of the component transistors to maintain charge carriers in the channel region, even when $V_{\rm SUP}$ is not applied. In the hold operation, the $V_{\rm OUT}$ value is determined by charge carriers stored in the channel region of the transistors.

2.5 XNOR and XOR LiM operations or the BT-LiM cell

In the BT-LiM cell, the XNOR and XOR logic operations were implemented by changing the channel mode configuration (Figure 4(a)). The XNOR gate comprises two n- and p-channel mode TG FBFETs on both the pull-up and pull-down sides. Component transistors with the same channel mode were connected in series in the pull-up network, while the transistors with different channel modes were connected in series in the pull-down network. In contrast, the XOR gate exhibits pull-up and pull-down networks

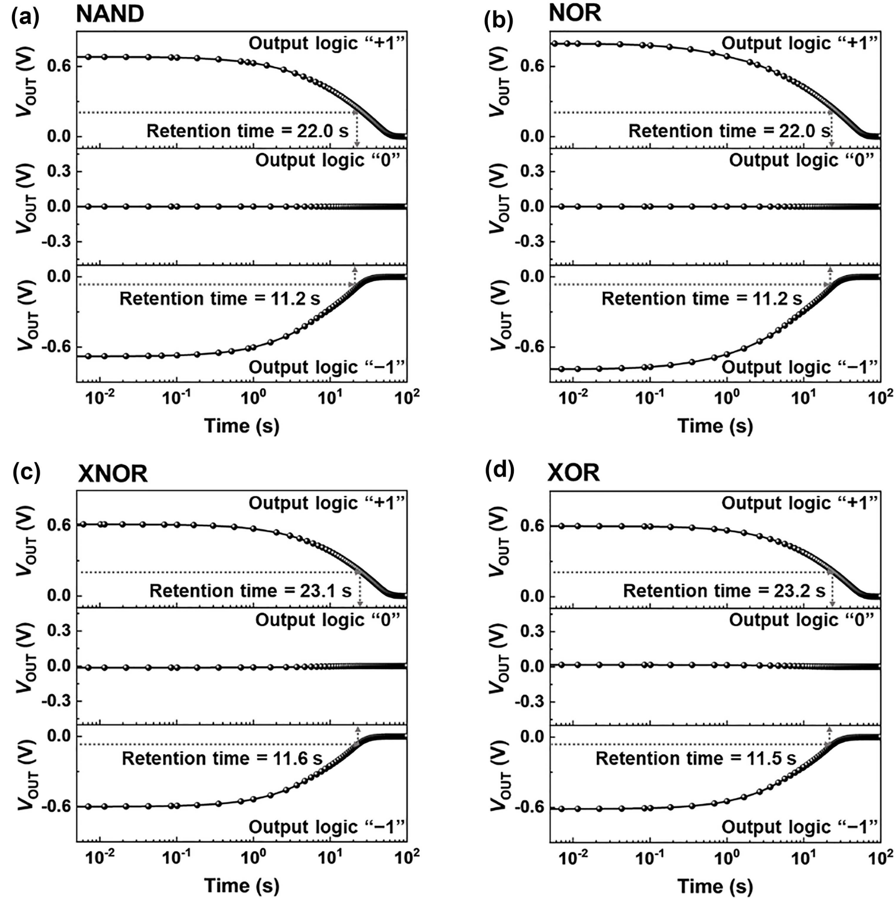

Figure 5 Logic retention characteristics of the BT-LiM cell. $V_{\rm OUT}$ as a function of the duration of the hold operation for (a) NAND, (b) NOR, (c) XNOR, and (d) XOR gate operations.

with channel-mode configurations that reverse those of the XNOR gate. The combinations of $V_{\rm IN}$ for the XNOR logic operation remained the same as those in the XOR gate operation. Binary and ternary XNOR LiM operations were conducted as shown in Figure 4(b). For the binary XNOR operation, the pull-up network consists of component transistors in the same channel mode connected in series, and thereby, output logic "+1" is obtained when $V_{\rm IN1}$ and $V_{\rm IN2}$ are the same. Output logic "−1" is attained when they have opposite values because of the series connection of the component transistors in the different channel modes. For the ternary XNOR operation, output logics "+1" and "−1" are obtained in the same manner as the binary operation, and output logic "0" is obtained when input logic "0" is applied to either or both $V_{\rm IN1}$ and $V_{\rm IN2}$. The XOR gate has opposite pull-up and pull-down configurations to those of the XNOR gate such that these two logic gates exhibit opposite output logic for the same input logic (Figure 4(c)). In the binary XOR operation, output logic "+1" is obtained when $V_{\rm IN1}$ and $V_{\rm IN2}$ are different, and output logic "−1" is obtained when both $V_{\rm IN1}$ and $V_{\rm IN2}$ are the same. In the ternary XOR logic operation, when either input is set to input logic "0", $V_{\rm OUT}$ is close to 0 V. Both the pull-up and pull-down networks exhibit similar resistances. The LiM operations of the other logic gates are shown in Figures S1 and S2.

2.6 Logic retention characteristics of the BT-LiM cell

As shown in Figure 5, the logic retention characteristics of NAND, NOR, XNOR, and XOR logic gates were analyzed to evaluate the LiM operation of the BT-LiM cell. The retention characteristics are confirmed as the change of the $V_{\rm OUT}$ values corresponding to output logics "+1", "0", and "−1" during the hold operation after a logic operation with a pulse width of 1 ms. In the hold operation, all external voltages including $V_{\rm SUP}$, $V_{\rm PG}$, $V_{\rm IN1}$, and $V_{\rm IN2}$ are set to 0 V. As time passes, charge carriers stored in the channel region of the TG FBFETs decrease because of recombination, which causes $V_{\rm OUT}$ to gradually

Table 1 Comparison between the logic gates of the BT-LiM cell and previously reported binary and ternary multifunctional logic gates.

Ref.	Device type	Logic functions		Logic conversion method (Binary ↔ Ternary)	Logic retention time
		Binary	Ternary		
[7] (Experiment)	MoS_2 FET	Inverter	Inverter	Changing top gate voltage (−3 V ↔ 2 V)	–
[8] (Experiment)	Organic-based heterojunction transistor	Inverter	Inverter	Changing programming voltage (18 V ↔ 15 V)	–
[9] (Experiment)	BP-MoS_2 heterojunction transistor	Inverter	Inverter	Changing V_{DD} (0.2 V ↔ 2.0 V)	–
[10] (Experiment)	BP-ReS_2 heterojunction transistor	Inverter	Inverter	Changing V_{DD} (0.4 V ↔ 2.0 V)	–
[11] (Experiment)	$MoTe_2$-MoS_2 heterojunction transistor	NOT/OR/XOR	OR	No need	–
[26] (Simulation)	Si Tunneling and drift-diffusion FET	Inverter	Inverter	Changing V_{DD} (0.9 V ↔ 1.2 V)	–
[27] (Simulation)	Si-Ge tunneling FET	Inverter	Inverter	Changing V_{DD} (0.7 V ↔ 1.0 V)	–
This work (Simulation)	Si FBFET	YES/NOT/AND, OR/NAND/NOR, XNOR/XOR	YES/NOT/AND, OR/NAND/NOR, XNOR/XOR	No need	23.2 s

approach 0 V. The logic retention time is defined as the time required for the $V_{\rm OUT}$ value to reach 37% of its initial value. The NAND and NOR gates demonstrate identical logic retention times (Figures 5(a) and (b)); the retention times are 22.0 and 11.2 s for output logics "+1" and "−1", respectively. The XNOR logic gate has logic retention times of 23.1 and 11.6 s for output logics "+1" and "−1", respectively (Figure 5(c)). The XOR gate exhibits logic retention times of 23.2 and 11.5 s for output logics "+1" and "−1", respectively (Figure 5(d)). For the output logic "0", the $V_{\rm OUT}$ value remains stable close to 0 V for a duration of 100 s for all four logic gates. The retention characteristics of the other Boolean logic gates showed similar tendencies (Figure S3). $V_{\rm OUT}$ remains stable as long as the resistance ratio between the pull-up and pull-down networks is maintained. In addition, the configuration of the BT-LiM cell with the TG FBFETs connected in series in both the pull-up and pull-down networks effectively reduced the leakage current, which demonstrates excellent retention characteristics.

It is crucial to implement various logic gates to enhance the logic performance per unit area. Table 1 [7–11, 26, 27] presents a comparison with previously reported binary and ternary multifunctional logic gates. Compared with experimental studies on binary and ternary multifunctional logic gates, there are not a lot of the simulation studies; the concept of logic conversion in a circuit has been applied in simulation techniques in recent years. In addition, there has been little research dealing with logic retention times of the BT-LiM cells. In terms of binary and ternary logic functions, the BT-LiM cell has advantages in area efficiency because all eight Boolean logic gates within a single cell can be achieved without the need for the additional circuit for each logic gate. Furthermore, it can be designed in a vertical structure with the expected cell size being $8F^2$, because the cell is composed of nanowire transistors [28]. Unlike most multifunctional logic circuits that require high voltage for programming or changing the external voltages for conversion between binary and ternary logic, our BT-LiM cell offers a significant advantage by performing both logics without the need for intermediate steps. In addition, the BT-LiM cell can store the outputs of logic operations for up to 23.2 s under zero-bias conditions, which helps reduce the bottleneck between memory and computing units, increasing operational efficiency and effectively reducing energy consumption during data transportation.

The energy consumptions are 12.6 and 12.4 fJ for output logics "+1" and "−1", respectively. For output logic "0", the energy consumption is estimated to be relatively high at 230 pJ; the transistors connected in series in both the pull-up and pull-down networks are in the ON states, resulting in a relatively high short-circuit current. On the other hand, the cell exhibits zero static energy consumption; all $V_{\rm SUP}$ values are set to 0 V during the hold operation. As for the operation speed, the BT-LiM cell shows an inherently limited speed due to the charge carrier storage ability; the cell retains the logic

results for up to 23.2 s by either accumulation or depletion of charge carriers within the channel region of TG FBFETs. According to our previous study [29], a reset pulse prior to the logic operations plays a role in the removal of charge carriers present in the channel region. Hence, the operation speed of the cell can be improved by introducing a reset pulse prior to the logic operations.

3 Conclusion

Our TCAD simulation demonstrated the binary and ternary LiM operations of a BT-LiM cell comprising eight TG FBFETs. The component transistors of the cell are reconfigured into n- or p-channel modes and show high symmetry, such as an on-current ratio of 1.02 and fully symmetric $V_{\text{latch-up}}$. The cell successfully performs LiM operations for the YES, NOT, AND, OR, NAND, NOR, XNOR, and XOR gates in a single cell by reconfiguring the channel modes of the transistors and V_{IN} configurations. All eight Boolean logic gates can execute both binary and ternary logic operations within the same cell. There is no need for logic conversion processes such as applying programming voltage or using additional circuits because the binary logic is fully encompassed by the ternary logic in our cell. Further, the cell exhibited logic retention characteristics of up to 23.2 s even when all external voltages were zero. Our results suggest the potential for using multifunctional cells in new computing systems.

4 Methods

4.1 Device structure

A Synopsys Sentaurus TCAD simulator (O_2018.06) was used to simulate the TG FBFET with a two-dimensional device structure, which was created using the Sentaurus Device Editor module. The three gates were separated by 10 nm, and each gate had a length of 50 nm. The drain and source lengths were both 50 nm, and the thickness of the Si channel was 10 nm. The channel region was covered with an SiO_2 gate oxide layer with a thickness of 2 nm. The drain region was heavily p-doped (boron) with a doping concentration of 1×10^{20} cm^{-3}, and the source region was heavily n-doped (phosphorus) with a doping concentration of 1×10^{20} cm^{-3}. The intrinsic Si channel region was lightly boron-doped with a doping concentration of 1×10^{15} cm^{-3}. Because the channel was lightly p-doped, the TG FBFET can operate in the n- or p-channel modes by changing the polarity of V_{PG}. The work function for all gate metals was 4.65 eV.

4.2 Device and circuit simulation

All simulations of the BT-LiM cells comprising TG FBFETs were performed using the commercial device simulator Synopsys Sentaurus (O_2018.06). The transfer characteristics and energy band diagrams of a single TG FBFET were numerically investigated using a Sentaurus device. Our cell simulations were conducted using mixed-mode simulations that support multidevice simulations. To ensure the accuracy of the simulation results and to account for non-idealities, we applied a variety of physical models in which Fermi-Dirac statistics and Slotboom bandgap narrowing were included to model carrier distribution and to consider the effects of high doping concentrations, respectively. In addition, we used doping-dependent mobility, inversion and accumulation layer mobility, and high-field saturation mobility models to consider changes in mobility under high electric fields. Moreover, we considered Auger recombination and Shockley–Read–Hall (SRH) to capture various recombination mechanisms. Specifically, surface SRH recombination was included to account for the carrier recombination near the surface; it has a crucial impact on short-channel and nanowire structures.

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Supporting information Figures S1–S3. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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