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Substrate bias effects in p-channel GaN-on-Si transistors

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The drain current (I_D) of the n-channel GaN field-effect-transistor (n-FET) is influenced by the substrate-to-source bias voltage (V_{BS}) (substrate bias effect) [1]. Actually, non-zero V_{BS} is also likely to occur in p-FET in real application, because the source electrode of p-FET is usually connected to high voltage. This study reports the dependency between I_D and V_{BS} in p-FET for the first time, and analyzes the underlying mechanisms from the perspective of vertical electric field (EF) distribution.

Device structure and measurement setup. The schematic cross section and photograph of the devices under test are shown in Figures 1(a) and (b). The devices are standard GaN CMOS structure, with 50-nm p^{++}-GaN layer (Mg: 1×10^{20} cm^{-3} with 2% to 3% ionization rates), 30-nm p^{+}-GaN cap layer (Mg: 1×10^{18} cm^{-3}), 20-nm $Al_{0.22}Ga_{0.78}N$ barrier layer and 2-μm GaN buffer layer on P-Si substrate. The depth of gate recess in p-FET is 70 nm. The p^{++}-GaN layer and the p^{+}-GaN layer are collectively referred to as p-GaN. The drain to source distance (L_{DS}), gate length (L_G) and gate width (W_G) is $L_{DS}/L_G/W_G$ = 8 μm/1 μm/20 μm for n-FET and 4 μm/1 μm/200 μm for p-FET.

There are two kinds of measurement setups based on Agilent B1500A in this study. (1) Quasi-static measurement: I_D-V_{DS} measurements are conducted at various V_{BS}, where the drain current in the fresh device at V_{BS} = 0 V is referred to as I_0. (2) Transient measurement: the substrate was first biased at V_{BS} = ± 80 V for 10 min. After removing V_{BS} stress, I_D is sampled at V_{DS} = −10 V, V_{GS} = −4 V and V_{BS} = 0 V, until I_D returns to I_0.

Quasi-static measurement. The quasi-static measurement results of p-FET are shown in Figure 1(c), in which the curve at V_{BS} = 0 V is marked with red circles. The relationship between normalized I_D and V_{BS} of both p-FET and n-FET is further plotted in Figure 1(d), where normalized I_D is the ratio of I_D to I_0. Normalized I_D of n-FET remains constant under positive V_{BS}, and decreases under negative V_{BS}, which is in accordance with the report in [1]. Nevertheless, in p-FET, I_D shows a reduction of 21.7% at V_{BS} = 80 V compared to I_0, and exhibits an increment of 17.5% at V_{BS} = −80 V. This monotonic dependency has not been reported in literature yet.

It is proposed that the change of I_D is related to the vertical EF in the channel [2]. According to classical electrostatics, EF lines start from positive charges and terminate at negative charges. That means, when vertical EF lines point into the channel, there will be more electrons (i.e., fewer holes) in the channel. When EF lines point out from the channel, there will be fewer electrons (i.e., more holes). V_{BS} impacts vertical EF distribution through two mechanisms: (1) V_{BS} acts as a back gate which directly generates vertical EF lines via field effect; (2) V_{BS} induces carrier injection and space charge (Q_{space}) formation in the buffer layer, which further modulates EF distribution (Figures 1(e) and (f)).

Under positive V_{BS}, the back gate generates upward vertical EF pointing from the substrate to the channel, and electrons are injected from 2DEG and/or ohmic contacts into the buffer layer to form negative space charges ($Q_{space} < 0$). For n-FET (the left of Figure 1(g)), the negative Q_{space} can absorb all the upward electric EF lines and screen 2DEG from being influenced, resulting in a nearly constant I_D [1]. In terms of p-FET (the right of Figure 1(g)), electron injection is significantly weaker than in n-FET for two reasons: first, 2DEG outside the gate region is depleted by p-GaN; second, ohmic contacts cannot provide electrons, as they are separated from 2DEG by p-GaN. As a result, the negative Q_{space} can merely absorb part of the upward EF lines. The rest of the upward electric EF lines enter the p-GaN channel and decrease the hole density. Hence, I_D of p-FET is lower than I_0 under positive V_{BS}.

Under negative V_{BS}, both electrons and holes contribute

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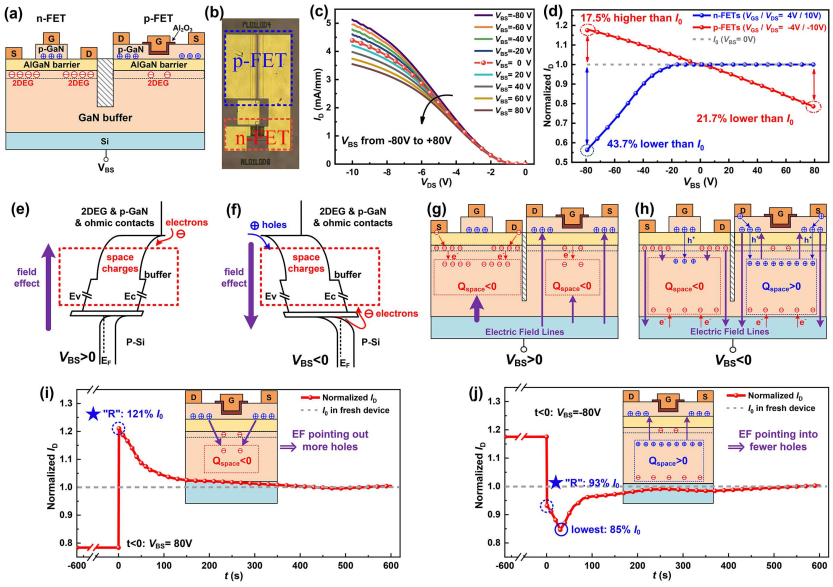

Figure 1 (Color online) Schematic and measurement results. (a) Schematic cross section and (b) photograph of fabricated GaN-on-Si n-FET and p-FET. (c) Quasi-static I_D-V_{DS} measurement of p-FET at $V_{GS} = -4$ V. (d) Normalized I_D-V_{BS} of n-FET and p-FET. Schematic energy band diagram under (e) positive and (f) negative V_{BS}. Schematic space charge and vertical EF lines under (g) positive and (h) negative V_{BS}. Transient measurement after removing (i) positive and (j) negative V_{BS}, where "R" responds to the moment of V_{BS} removal.

to the formation of space charges. However, the energy barrier at the GaN/Si interface hinders the electron injection [3], and the low hole mobility in bulk GaN also leads to inefficient hole injection. In the case of n-FET (the left of Figure 1(h)), hole injection only occurs under the gate region, so the total Q_{space} is still negative. Both the back gate and negative Q_{space} attract EF lines to point out from 2DEG, which leads to lower electron density and smaller I_D. When it comes to p-FET (the right of Figure 1(h)), hole injection becomes stronger than in n-FET because there is a larger area of p-GaN. The later transient measurements validate that Q_{space} of p-FET under negative V_{BS} is positive. The positive Q_{space} and the back gate create EF lines in opposite directions. Since p-FET exhibits a larger I_D under negative V_{BS}, it is inferred that the impact of the back gate is more predominant, which creates downward EF lines to point out from the channel.

Transient measurement. It has been mentioned that V_{BS} modulates channel carrier densities through the back gate and space charges, and the quasi-static measurement results are a combination of the two factors. If a long-term V_{BS} stress is suddenly removed, the back gate will also disappear instantaneously, but the space charges will continue impacting I_D because part of the injected carriers are captured by the traps in the buffer layer. We can conduct transient measurements and monitor the recovery trend of I_D after removing V_{BS} to verify the existence about the space charges.

In this study, the origin of space charges is assumed to be the ionization of traps, which means electrons and holes are respectively captured by acceptor-like and donor-like traps. The de-ionization of traps is not taken into account because it only occurs at high V_{BS} (over 100 V) [4].

When a positive V_{BS} is switched back to 0 V ("R" in Figure 1(i)), trapped electrons (negative Q_{space}) attract downward EF lines to point out from the channel, so that I_D at "R" is about 21% higher than I_0. After about 400 s, I_D gradually recovers to I_0, along with the release of trapped electrons.

On the other hand, upon the removal of negative V_{BS}, I_D is 7% lower than I_0 at "R" in Figure 1(j), which validates a positive Q_{space} at this moment. I_D first drops to a minimum value (15% lower than I_0), and then recovers to I_0 over 600 s. The non-monotonic recovery process of I_D after "R" indicates the involvement of both electrons and holes, with trapped electrons being released earlier than holes.

Conclusion. This work studies the substrate bias effect in p-channel GaN transistors for the first time. The drain current is observed to decrease under positive V_{BS} and increase under negative V_{BS}. Such a phenomenon is explained through the effect of the back gate and space charges.

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