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Analysis and solution of streak effect in high dynamic range CMOS image sensors

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The high dynamic range (HDR) CMOS image sensor has been widely used in many fields, such as autonomous driving and security guarding [1]. The dual conversion gain (DCG) structure, which adjusts the conversion gain (CG) by changing the capacitors connected to the floating diffusion (FD) nodes in the pixel, is an effective and prevalent method for realizing HDR imaging [2]. While the DCG structure can extend the dynamic range, in the practical HDR imaging process, the substantial number of photo-generated electrons in bright areas can cause significant voltage variations in the pixel output. These variations affect the gray values in darker areas of the same image, leading to the streak effect [3]. This study primarily investigates the streak effect caused by forward conduction current of the PN junction in DCG pixels, and proposes a circuit to suppress this effect.

HDR pixel structure. The HDR pixel structure and timing diagram are shown in Figure 1(a). The photodiode (PD) collects the photons and then generates the photoelectrons. The transistor M_{RST} empties the photoelectrons accumulated in C_{FD} before a new exposure period. The transistor M_{TX} transfers the photoelectrons from PD to C_{FD} when the signal V_{TX} is high. The transistor M_{CAP} is a MOS capacitor in a pixel that the gate connected to the source of M_{RST} is the top plate and the source and drain connected to the ground are the bottom plates. The transistor M_{SF} is a source-follower that is used to buffer the voltage on C_{FD} and the transistor M_{SEL} is a switch that decides whether V_{pixel} is connected to the column bus. The transistor M_{HDR} is used to change the C_{FD}. Through switching the M_{HDR}, the C_{FD} can be adjusted to realize HDR imaging:

$$C_{\mathrm{FD}} = \begin{cases} C_{\mathrm{SF}}, & \text{when } V_{\mathrm{HDR}} \text{ is low}, \\ C_{\mathrm{SF}} + C_{\mathrm{HDR}}, & \text{when } V_{\mathrm{HDR}} \text{ is high}, \end{cases} \tag{1}$$

where C_{SF} is the gate parasitic capacitor of M_{SF} and C_{HDR} is the gate parasitic capacitor of M_{CAP}.

Streak effect. During the HDR imaging process, the transistor M_{HDR} is switched on to allow C_{FD} to collect more electrons. After V_{TX} becomes high, the photoelectrons generated in PD are transferred to C_{FD} and the voltage of FD decreases by

$$\Delta V_{\mathrm{FD}} = \frac{Q_{\mathrm{PD}}}{C_{\mathrm{SF}} + C_{\mathrm{HDR}}}, \tag{2}$$

where Q_{PD} is the number of photoelectrons. And the voltage at the top plate of M_{CAP} decreases the same voltage

$$\Delta V_{\mathrm{MOS}} = \Delta V_{\mathrm{FD}}. \tag{3}$$

Because the influence of C_{GS} and C_{GD} of M_{CAP}, a transient voltage drop appears at the bottom plate of M_{CAP} and it can be derived as

$$\Delta V_{\mathrm{drop}} = \Delta V_{\mathrm{MOS}} \cdot \frac{C_{\mathrm{GS},M_{\mathrm{CAP}}}}{C_{\mathrm{GS},M_{\mathrm{CAP}}} + C_{\mathrm{SB},M_{\mathrm{CAP}}}}. \tag{4}$$

ΔV_{drop} will make V_{D} and V_{S} drop below V_{B} instantaneously. The PN junction in M_{CAP} between the source/drain and the substrate transitions from reverse biased to forward biased. Therefore, the heavily doped N-type source/drain, the P-type substrate, and the lightly doped N-type PD form a structure similar to an N-P-N bipolar transistor in the amplification state, as shown in Figure 1(c). The forward-biased PN junction between the substrate and the source/drain will generate a drift current $I_{\mathrm{M\text{-}S}}$, causing a large number of electrons flowing from the source/drain to the substrate. After recombining with holes in the low-doped substrate, the remaining electrons will be influenced by the diffusion electric field between the substrate and the PD, forming a diffusion current $I_{\mathrm{S\text{-}P}}$ and thus entering the PD. $I_{\mathrm{S\text{-}P}}$ can be derived from the collector current of bipolar junction transistor as follows:

$$I_{\mathrm{S\text{-}P}} = i_{\mathrm{s}} \cdot \exp\left(\frac{|V_{\mathrm{DS/BS}}(t)|}{V_{\mathrm{t}}}\right), \tag{5}$$

where V_{t} is the thermal voltage and i_{s} is the reverse saturation current of the PN junction. Due to V_{D} and V_{S} of M_{CAP} recovering from ΔV_{drop} to 0 V over time, the number of electrons entering the PD can be derived as

$$Q_{\mathrm{PD\_leak}} = \int_0^{+\infty} i_{\mathrm{s}} \cdot \exp\left(\frac{|V_{\mathrm{DS/BS}}(t)|}{V_{\mathrm{t}}}\right) \cdot t_{\mathrm{rec}} \cdot \mathrm{d}t, \tag{6}$$

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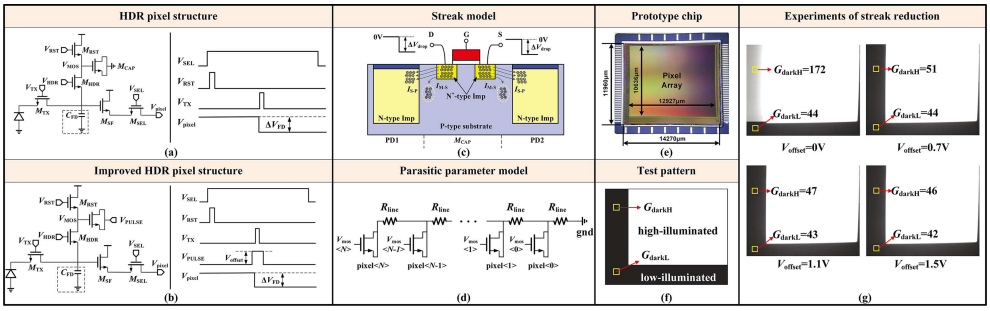

Figure 1 (Color online) Principle of the streak effect and reduction method. (a) HDR pixel structure; (b) improved HDR pixel structure; (c) streak model; (d) parasitic parameter model; (e) prototype chip; (f) test pattern; (g) experiments of streak reduction.

where $t_{\rm rec}$ is the recovery time. It depends on the load capacitance and resistance on source and drain of $M_{\rm CAP}$. To figure out $t_{\rm rec}$ and $|V_{\rm DS/BS}(t)|$, the parasitic parameter model of $M_{\rm CAP}$ is shown in Figure 1(d). There are N pixels in a row that share the metal connection of the ground. The ground is connected from the right side of the pixel array. $R_{\rm line}$ is the parasitic resistance of the metal line in each pixel. The recovery time of $V_{\rm D}$ and $V_{\rm S}$ depends on the specific position of the pixel. $t_{\rm rec}$ of pixel $\langle i\rangle$ can be derived as

$$t_{\rm rec}(i) = (i+1)\cdot R_{\rm line}\cdot C_{\rm HDR}. \tag{7}$$

If M pixels are under high illumination that will cause large $V_{\rm drop}$ and $(N-M)$ pixels are under low illumination that $V_{\rm drop}\approx 0$. $|V_{\rm DS/BS}(t)|$ of pixel$\langle i\rangle$ can be derived as

$$|V_{\rm DS/BS}(t)_i| = \Delta V_{\rm drop}\cdot\frac{M}{N}\cdot\exp\left(-\frac{t}{t_{\rm rec}(i)}\right). \tag{8}$$

By substituting (7) and (8) into (6), the additional charges in pixel$\langle i\rangle$ due to $I_{\rm S\text{-}P}$ can be derived as

$$Q_{\rm PD\_leak}(i) = \int_0^{+\infty} i_{\rm s}\cdot\exp\left(\frac{|V_{\rm DS/BS}(t)_i|}{V_{\rm t}}\right)\cdot t_{\rm rec}(i)\cdot{\rm d}t. \tag{9}$$

According to (9), in pixels located further away from the ground port, $V_{\rm D}$ and $V_{\rm S}$ require a longer recovery time and more electrons will enter the PD. Besides, if more pixels are under high-illuminated condition, the streak effect in dark areas will become more severe.

Reduction method and experiments. In order to reduce the streak effect mentioned above, a control signal $V_{\rm PULSE}$ is applied to $V_{\rm D}/V_{\rm S}$ of $M_{\rm CAP}$. The proposed structure and timing diagram are shown in Figure 1(b). Before the signal $V_{\rm TX}$ becomes high, $V_{\rm PULSE}$ becomes high first to pull $V_{\rm D}/V_{\rm S}$ of $M_{\rm CAP}$ to $V_{\rm offset}$. After the $V_{\rm TX}$ becomes high and $V_{\rm drop}$ appears, $V_{\rm D}$ and $V_{\rm S}$ can be calculated as

$$V_{\rm S/D} = V_{\rm offset} - \Delta V_{\rm drop}. \tag{10}$$

According to (10), we can ensure $V_{\rm S/D} > 0$ V by adjusting $V_{\rm offset}$ at all times. The PN junction between the substrate and the source/drain of $M_{\rm CAP}$ remains reverse biased, thereby preventing electrons drifting into the substrate and suppressing the streak effect.

In order to validate the method proposed in this study for suppressing the streak effect, a 1280 × 1024 CMOS image sensor is fabricated in a 110 nm 1P4M process as shown in Figure 1(e). The size of the pixel array is 12927 μm × 10636 μm and the size of the chip is 14270 μm × 11960 μm. The driver circuits are implemented on the right side of the pixel array. The test pattern is shown in Figure 1(f). In the constructed HDR scene, the upper-right corner of the frame is illuminated by high light, while the remaining parts are kept dark to emphasize the streak effect. The grayscale value of pixel darkH, located in a low-illuminated area within the same row as the high-illuminated area, is denoted as $G_{\rm darkH}$. The grayscale value of pixel darkL, in the same column as darkH but entirely in the low-illuminated area, is denoted as $G_{\rm darkL}$. The difference ΔG between $G_{\rm darkH}$ and $G_{\rm darkL}$ represents the magnitude of the streak effect. The sample picture and suppression results of the streak effect are shown in Figure 1(g). When $V_{\rm offset} = 0$ V, the status of $M_{\rm CAP}$ is the same as that in Figure 1(a) and the typical streak effect appears in the darkH region. Under this condition, $G_{\rm darkH} = 172$ and $G_{\rm darkL} = 44$. Their difference ΔG is 128 due to the streak effect. When $V_{\rm offset} = 0.7$ V, ΔG is reduced to 7. The steak effect is suppressed apparently compared with $V_{\rm offset} = 0$ V. When $V_{\rm offset}$ is raised up to 1.1 V, ΔG is reduced to 4. When $V_{\rm offset} = 1.5$ V, ΔG is the same as that in $V_{\rm offset} = 1.1$ V. The streak effect caused by the PN junction current of $M_{\rm CAP}$ is suppressed effectively. The remaining difference in grayscale between darkH and darkL is caused by other ideal effects in the pixel array and readout circuits.

Conclusion. The streak effect caused by the forward-biased PN junction current of MOS capacitors in HDR pixels is analyzed and a method to suppress it is proposed in this study. In HDR pixels, the voltage of the MOS capacitor's top and bottom plates is affected by the voltage drop at the FD, causing the PN junction between the substrate and the source/drain to become forward biased, which leads to electrons flowing from the source/drain regions to the PD and causes streak effect. In order to suppress the steak effect, a positive pulse is applied to the bottom plate of the MOS capacitor to compensate for the voltage drop. According to the experiment results, the difference of grayscale value representing the steak effect is reduced from 128 to 4.

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References

1 Nishimura K, Sato Y, Hirase J, et al. An over 120dB simultaneous-capture wide-dynamic-range 1.6e− ultra-low-reset-noise organic-photoconductive-film CMOS image sensor. In: Proceedings of IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, 2016
2 Ma C, Liu Y, Li Y, et al. A 4-M pixel high dynamic range, low-noise CMOS image sensor with low-power counting ADC. IEEE Trans Electron Dev, 2017, 64: 3199–3205
3 Purcell M, Storm G, Elliott R, et al. Image artifacts caused by pixel bias cells in CMOS imagers targeted for mobile applications. In: Proceedings of International Image Sensor Workshop, Bergen, 2009