SCIENCE CHINA
Information Sciences

• LETTER •

January 2025, Vol. 68, Iss. 1, 119401:1–119401:2
https://doi.org/10.1007/s11432-024-4190-4

# Physics based circuit compatible model for hybrid antiferroelectric random access memory

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Received 12 June 2024/Revised 13 September 2024/Accepted 14 October 2024/Published online 29 November 2024

**Citation** Wu Q X, Peng Y, Xiao W W, et al. Physics based circuit compatible model for hybrid antiferroelectric random access memory. Sci China Inf Sci, 2025, 68(1): 119401, https://doi.org/10.1007/s11432-024-4190-4

Since the discovery of $HfO_2$-based ferroelectric (FE) materials in 2011, considerable advancements have been made in material preparation, mechanism research, and device realization [1]. Consequently, these materials are now regarded as leading candidates for embedded non-volatile memory (eNVM). Beyond eNVM applications, recent studies have demonstrated that memory devices with antiferroelectric (AFE) films can achieve high response speeds, low latency, and reduced power consumption while maintaining excellent endurance characteristics [2, 3]. Additionally, the typical double hysteresis loops and multiple non-overlapping polarization current peaks of AFE films offer a novel approach to designing multistate memories. However, in order to further promote the application of high storage density AFE, an AFRAM electronic design automation (EDA) model must be developed, and it has yet to be proposed.

In this study, a physics-based AFRAM EDA circuit model is developed. Two logic operation functions are realized in parallel within a single AFRAM cell.

*Methods.* Figure 1(a) shows the schematic diagram of the AFRAM EDA model proposed in this study, which comprises two sublattice equivalent circuits (sublattice EC models I and II) and voltage-controlled switches ($SW_1$ and $SW_2$). Each sublattice EC model includes resistors $R_1(R_2)$ and capacitors $C_1(C_2)$ connected in series at the input of nonlinear voltage-controlled voltage sources ($kv_1$ and $kv_2$) to simulate linear properties. At the output, the voltage-controlled current sources ($gv_1$ and $gv_2$) with transconductances equal to 1 are in parallel with $R_3$, $C_3$, and $R_4$, $C_4$. The nonlinear characteristics of the AFE are mainly determined by $kv_1$ and $kv_2$. To replicate full AFE behavior, sublattice EC I is configured with a positive input voltage ($V_{in} > 0$) to simulate operation in the positive polarization domain, while sublattice EC II is set with $V_{in} < 0$ to represent the negative polarization domain. Figure 1(b) depicts the specific modeling details and parameters. The results in Figure 1(c) show a high degree of consistency with experimental data, indicating that the AFRAM EDA model exhibits strong accuracy and reliability.

Figure 1(d) illustrates the timing diagram for the "write" and "read" operations of the AFRAM, enabling four-state storage ('00', '01', '10', and '11'). Here, the word line (WL), bit line (BL), and plate line (PL) are defined, with $V_F$ representing the reference voltage for the PL. The write and read operations for data '00' and '01' are activated by pulsing $BL_{neg}$ and $PL_{neg}$, corresponding to the negative polarization region shown in Figure 1(e). Specifically, when data '00' is written, $PL_{neg}$ rises to $V_{DD}$ and the polarization state of the AFE capacitor switches to $-P_s$ (@ 'E') while $BL_{neg}$ remains zero. Then the WL is turned off, and the $PL_{neg}$ is kept at the $V_F$. After that, the polarization state changes from point 'E' to 'D', and the data '00' is written. Then, data '00' is read through raising $PL_{neg}$ to $V_{DD}$ while $BL_{neg}$ is pre-discharged to zero voltage and then kept floating. The voltage across the AFE capacitor is $-V_{DD}$ and the polarization state is switched to $-P_s$ (@'E'). The process of polarization state change during write/read operation follows the dashed trajectory (1) in Figure 1(e).

When data '01' is written, $BL_{neg}$ is raised to $V_F$ and $PL_{neg}$ is kept at $V_F$. After that, the polarization state of the AFE capacitor is written to the point 'O'. The $BL_{neg}$ drops to zero before WL is turned off. The polarization state turns from point 'O' to 'G' and the data '01' is written. Further, the data '01' can be read through raising $PL_{neg}$ to $V_{DD}$ while $BL_{neg}$ is pre-discharged to zero and then remains floating. The voltage across the AFE capacitor is $-V_{DD}$ and then the polarization state is switched to $-P_s$ (@'E'). The process of polarization state change during write/read operation follows the solid trajectory (2) in Figure 1(e). Additionally, Figure 1(e) implies that the average capacitance for reading '01' ($C_{01}$) is larger than that of reading '00' ($C_{00}$), that is $C_{01} > C_{00}$, which corresponds to the '01' read operation causing a larger increase in $BL_{neg}$ than '00'. Similarly, in the case of AFRAM write/read data '10' and '11', the $BL_{pos}$ and $PL_{pos}$ are carried out, corresponding to the positive polarization part in Figure 1(e), with their polarization state

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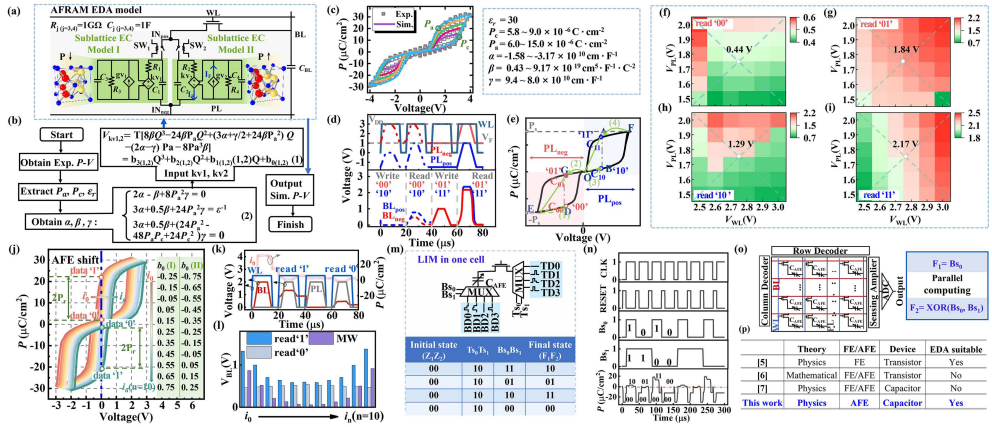

**Figure 1** (Color online) (a) Schematic of the AFRAM EDA model; (b) fitting process and parameter extraction; (c) experimental and simulation fitting results for the AFE capacitor; (d) time diagram of write/read operations; (e) corresponding polarization change trajectories for four-state storage; BL readout voltage for (f) '00', (g) '01', (h) '10', and (i) '11' at different $V_{\mathrm{WL}}$ and $V_{\mathrm{PL}}$; (j) non-centrosymmetric $P$-$V$ hysteresis of the AFRAM capacitor; (k) applied $V_{\mathrm{WL}}$, and $V_{\mathrm{PL}}$ pulses; (l) BL readout voltage in non-volatile AFRAM mode at different inputs; (m) single-cell LIM circuit schematic and truth table based on four-state AFRAM; (n) waveforms for the parallel computation scheme realizing two logic functions: $F_1 = B_{s0}$ and $F_2 = B_{s0}$ XOR $B_{s1}$; (o) application of LIM in an array; (p) performance benchmarking of the AFRAM EDA model in this work against reported FE/AFE models.

changes following tracks (3) and (4), respectively.

*Results and discussion.* The AFRAM EDA model can effectively support both volatile and non-volatile hybrid operating modes. Figures 1(f)–(i) illustrate the storage status of '00', '01', '10', and '11' read by BL at different WL and PL operating voltages ($V_{\mathrm{WL}}$ and $V_{\mathrm{PL}}$). The range of $V_{\mathrm{DD}}$ varies from 2.5 to 3.5 V. Notably, center values of BL readout voltage of '00', '01', '10', and '11' states are 0.44, 1.84, 1.29, and 2.17 V, respectively, thus achieving a memory window for negative part ($\mathrm{MW_{neg}}$) and a memory window for positive part ($\mathrm{MW_{pos}}$) of 1.40 and 0.88 V, respectively. It perfectly satisfies the practical memory array application requirements [4].

In addition to its application as a four-state volatile memory, the AFRAM EDA model's applicability in non-volatile mode is also explored. As shown in Figure 1(j), when AFRAM operates in the non-volatile state, it corresponds to the situation of the internal electric field introduced in the AFE film, thus achieving a non-centrosymmetric hysteresis and non-zero remanent polarization ($2P_{\mathrm{r}}$), resulting in two stable non-volatile states ('0' and '1'). In this work, the shifts of $P$-$V$ loop of the AFRAM capacitance are realized by adjusting the parameter $b_0$. Here, $b_0$(I) and $b_0$(II) are set to change from $i_0$ to $i_n$ ($n = 10$), and their specific parameter lists are shown in Figure 1(j). Similarly, the timing diagram of AFRAM EDA model operating in non-volatile mode is depicted in Figure 1(k). The $P$ extracted in the BL write/read operation signifies the successful integration of non-volatile functionality. The MWs for AFRAM operating in non-volatile mode with different $i_n$ values are illustrated in Figure 1(l).

Based on the AFRAM EDA model, we simultaneously implement two logic functions $F_1 = B_{\mathrm{s0}}$ and $F_2 = B_{\mathrm{s0}}$ XOR $B_{\mathrm{s1}}$. Figure 1(m) presents the circuit scheme and truth table for LIM in a single AFRAM cell. The waveforms in Figure 1(n) demonstrate the parallel computation process. As shown in Figure 1(o), the advantage of AFRAM in storage array applications is its ability to store 2 bits/cell and implement two logic functions in parallel by encoding polarization state as '00', '01', '10', and '11', thereby improving both storage density and computing efficiency. Figure 1(p) benchmarks the AFRAM EDA model developed in this study against previously reported ferroelectric and antiferroelectric models [5–7]. Notably, the physics-based AFRAM model proposed here not only enables flexible switching between volatile and non-volatile hybrid modes but is also suitable for EDA circuit simulations.

*Conclusion.* This study introduces a novel AFRAM EDA model capable of flexible implementation of four volatile states ('00', '01', '10', and '11') as well as non-volatile states ('0' and '1'). Additionally, leveraging the unique four-state storage characteristic of AFRAM, two logic functions $F_1 = B_{\mathrm{s0}}$, and $F_2 = B_{\mathrm{s0}}$ XOR $B_{\mathrm{s1}}$ are realized in parallel in a single AFRAM cell. This work presents a new AFRAM model employed in the EDA tool for designing high-speed, low-power embedded memory systems.

**Acknowledgements** This work was supported by National Natural Science Foundation of China (Grant Nos. 9236410005, 61534004), National Natural Science Foundation of Shaanxi Province (Grant No. 2023-JC-YB-497), Fundamental Research Funds for the Central Universities (Grant No. QTZX23080), and Young Elite Scientists Sponsorship Program by CAST (Grant No. 2022QNRC001).

**Supporting information** Appendixes A–C. The supporting information is available online at info.scichina.com and link.springer.com. The supporting materials are published as submitted, without typesetting or editing. The responsibility for scientific accuracy and content remains entirely with the authors.

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