

• Supplementary File •

MoS₂ synaptic transistor with one-step manufacture

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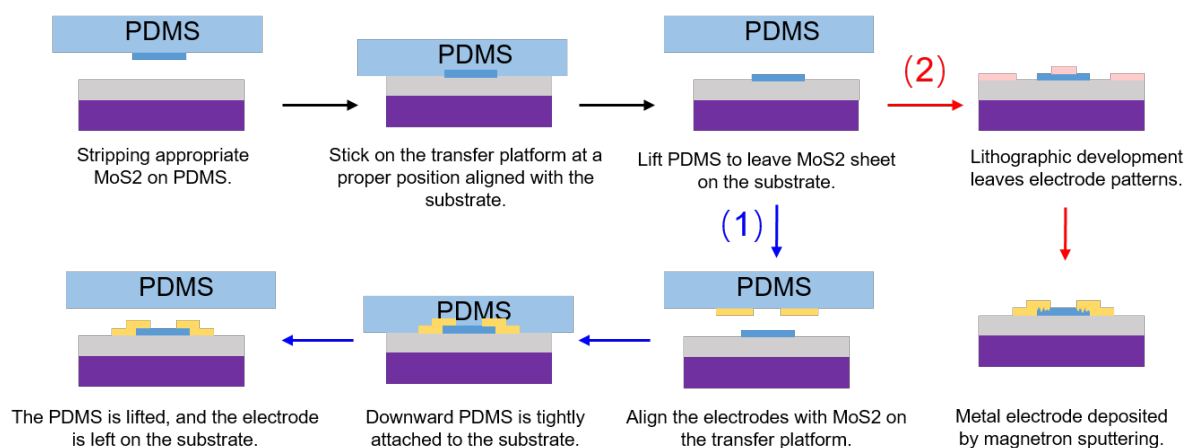


Figure S1 Transfer (1) and magnetron sputtering (2) schematic diagram of preparing mos₂ transistor by depositing electrodes.

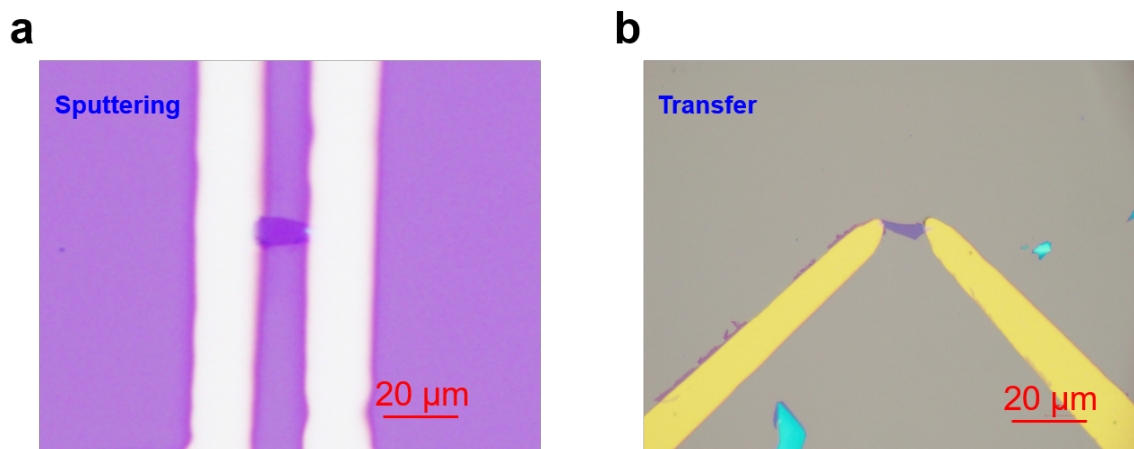


Figure S2 Optical microscope images of sputtering device (a) and transfer device (b).

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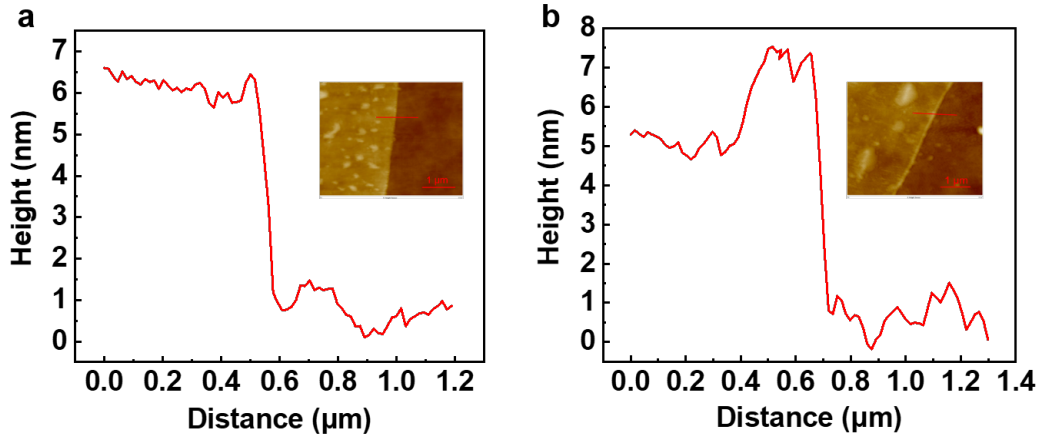


Figure S3 AFM images of channel of (a) transfer device and (b) sputtering device.

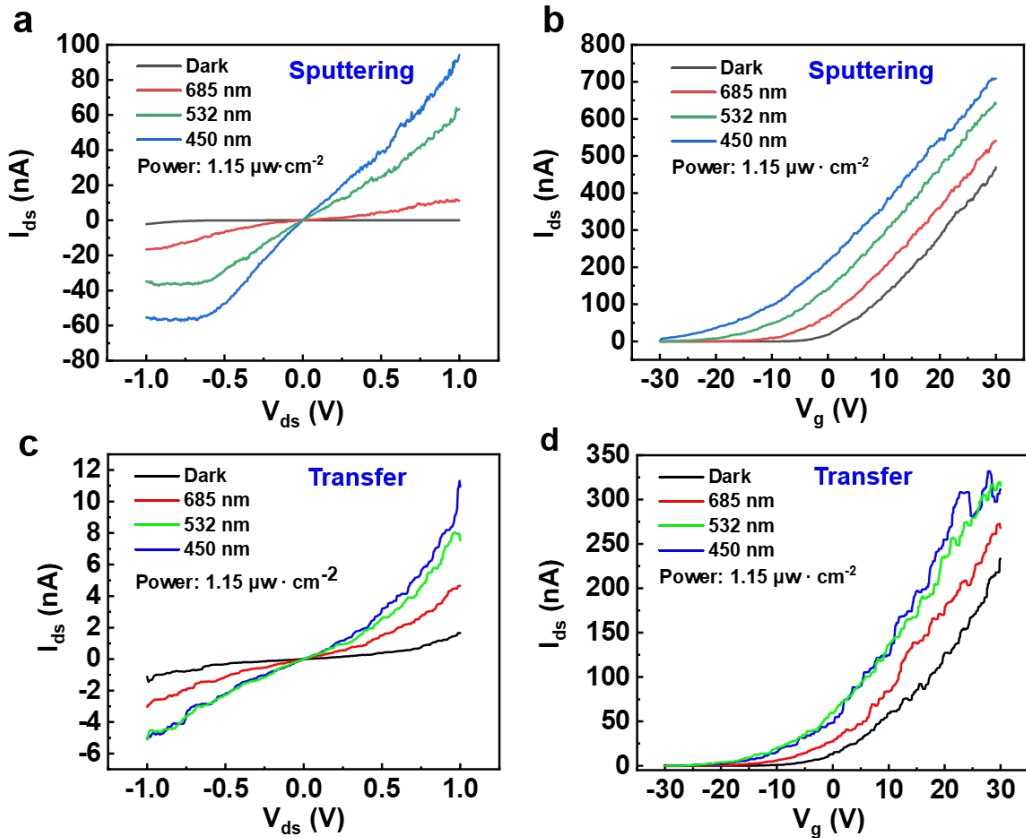


Figure S4 Basic photoelectric performance. The output characteristic curve (a) and transfer characteristic curve (b) of sputtering device. The output characteristic curve (c) and the transfer characteristic curve (d) of the transfer method device.

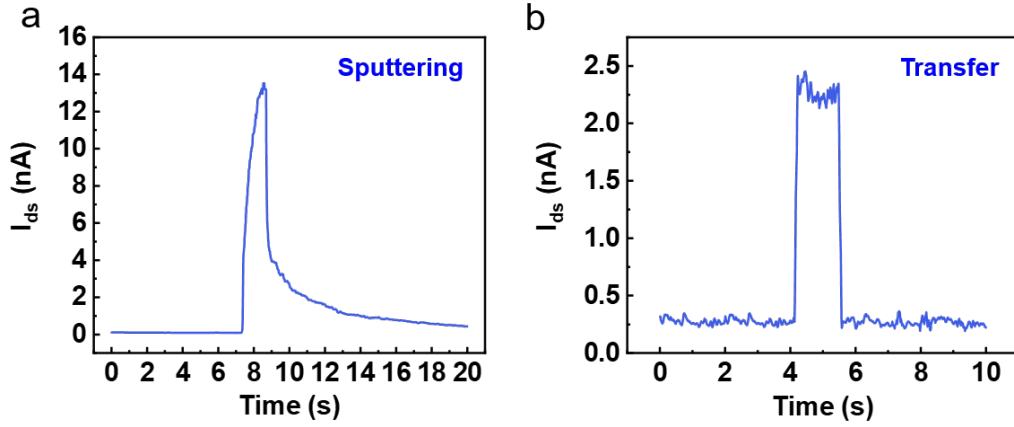


Figure S5 EPSC test of (a) sputtering device and (b) transfer device.

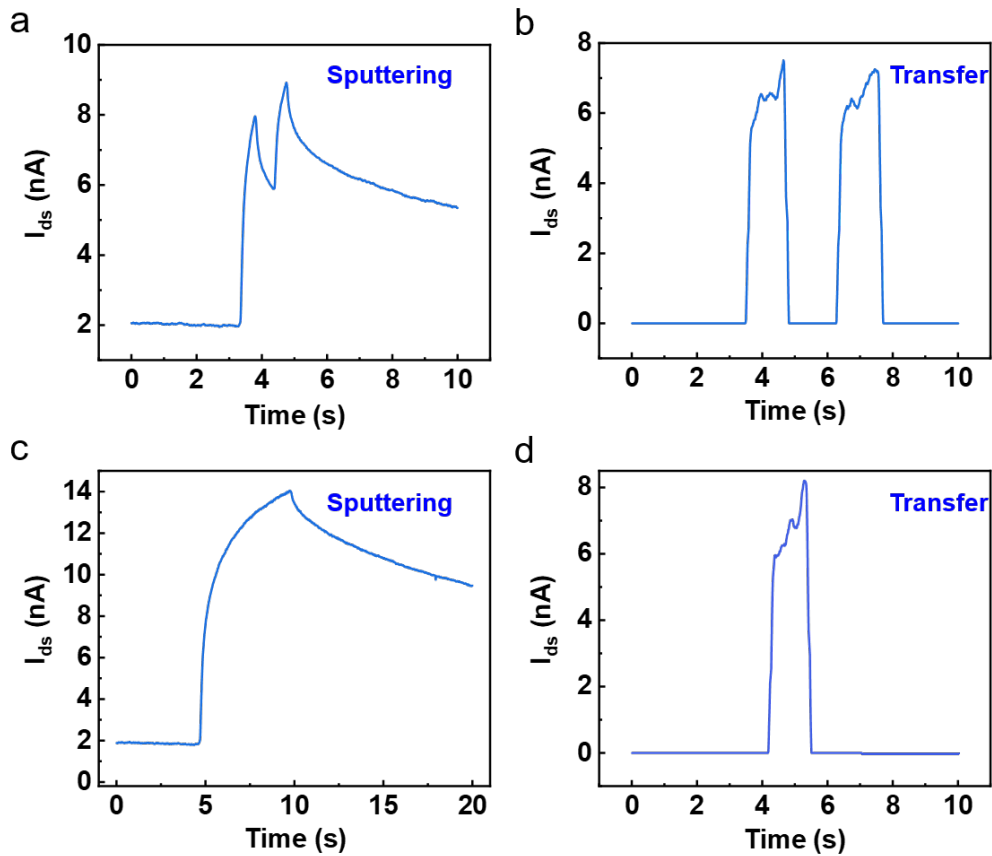


Figure S6 Repeatability of the method: Two devices are prepared by the same method, and the synaptic weight is adjusted and EPSC is tested again(685 nm, $1.4 \mu\text{W}\cdot\text{cm}^{-2}$). (a, c) New sputtering device. (b, d) New transfer device.

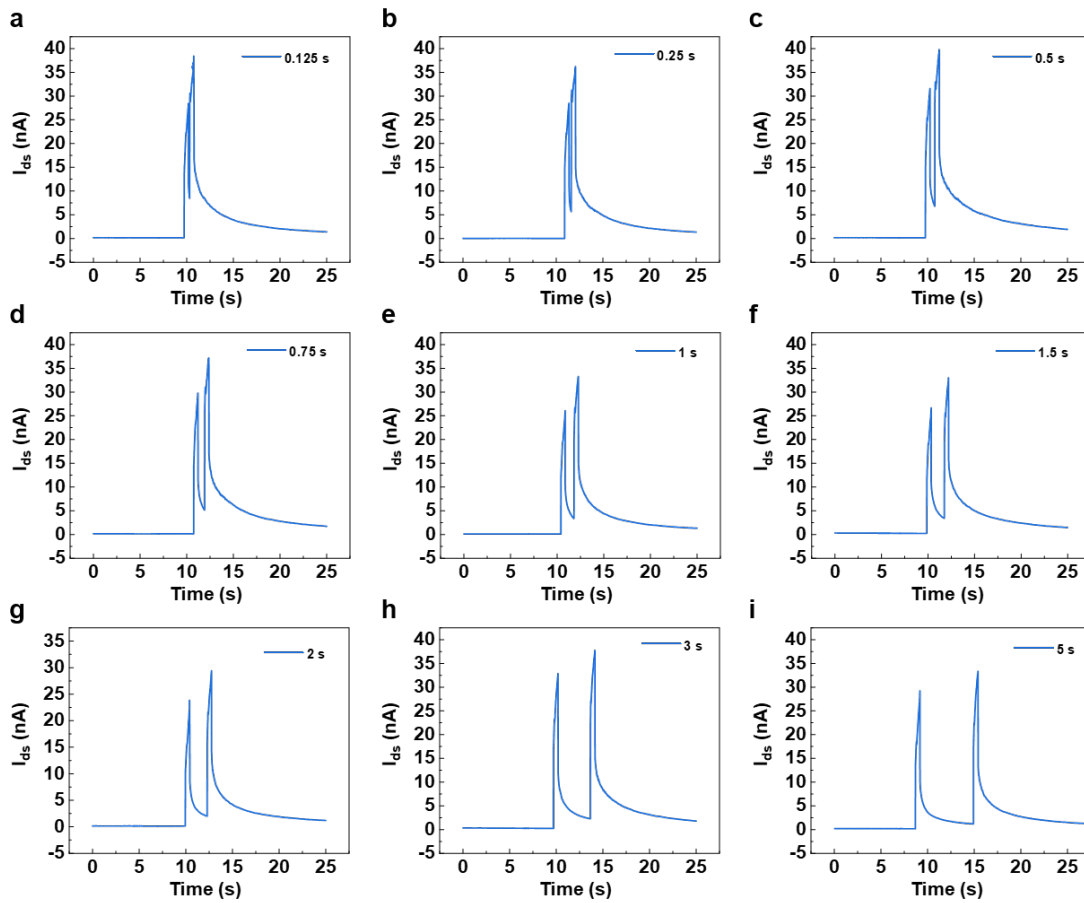


Figure S7 PPF test at different pulse intervals.

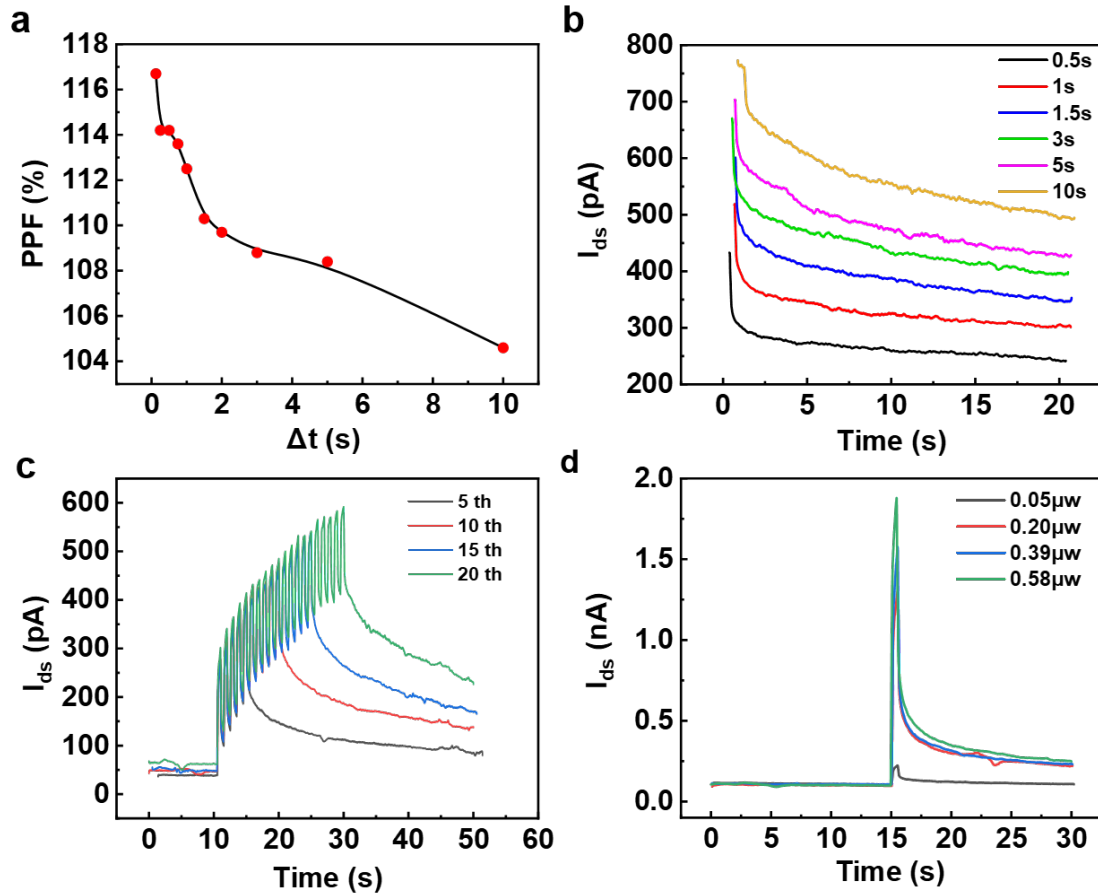


Figure S8 Synaptic plasticity of new devices. (a) PPF of the device. The STM to LTM transformation behavior of the device is observed under (b) different pulse width, (c) different pulse number and (d) different light intensity.

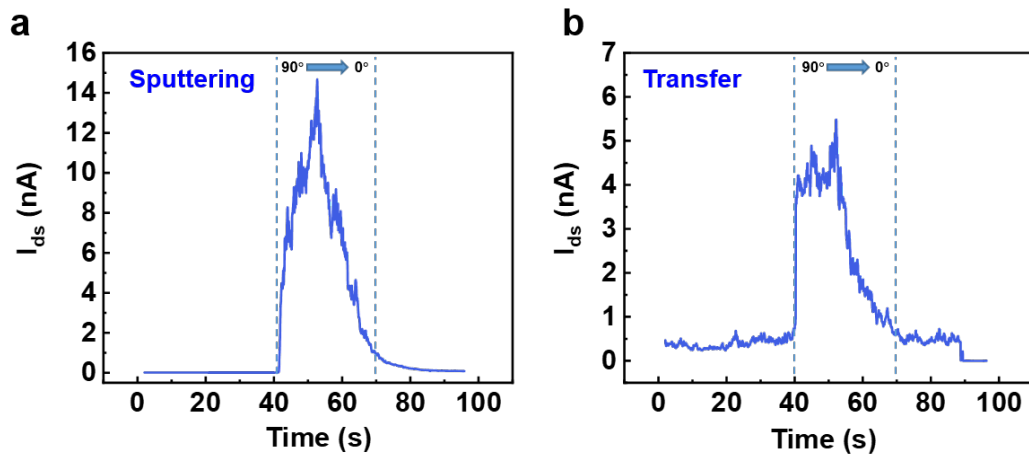


Figure S9 (a) The continuous change of the current of the sputtering device and (b) the transfer device under the condition that the incidence Angle from 90° to 0° gradually.

1	2	3
4	5	6
7	8	9

Figure S10 Schematic diagram of 3×3 synaptic transistor array.

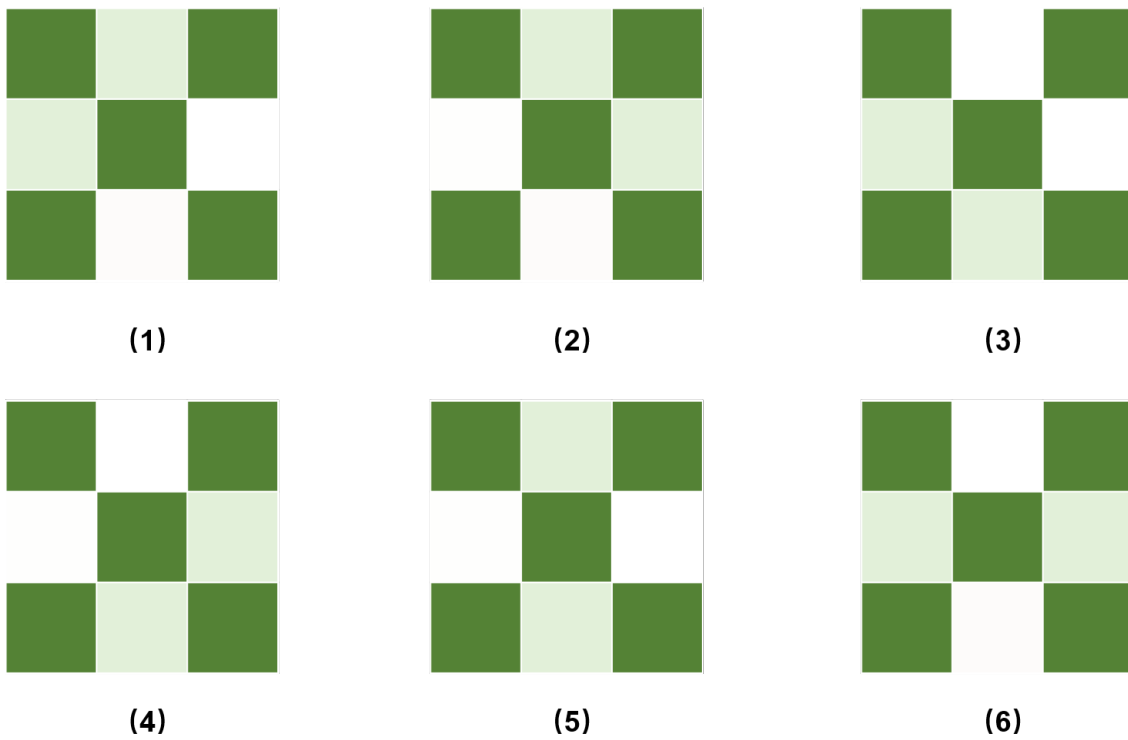


Figure S11 Six noisy images with a common feature “X”, each image has two noise points that are different from the other images.

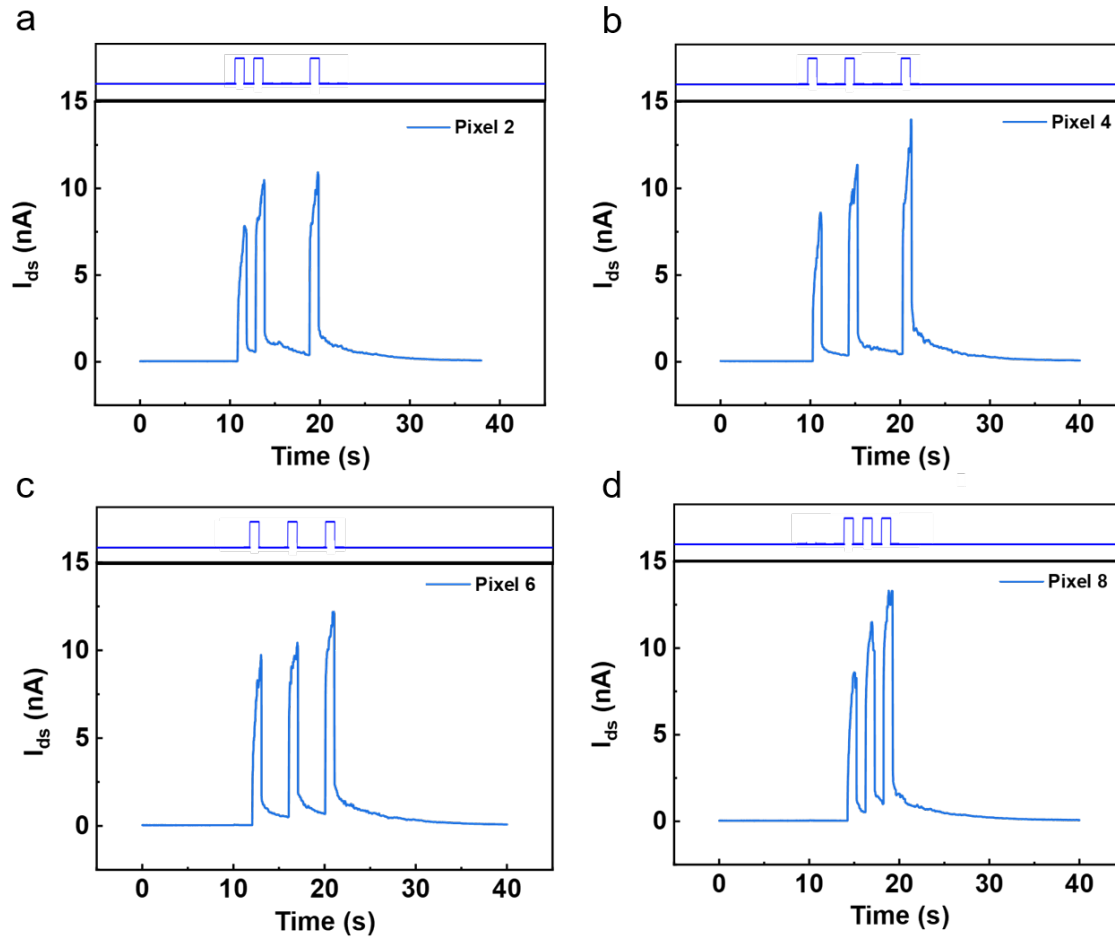


Figure S12 Changes of current in pixels 2, 4, 6 and 8 with pulse stimulation.